15

Gate Oscillators

15.1 INTRODUCTION

This and Chapter 16 treat the use of integrated circuits in oscillator design. Integrated circuits cannot be modified at will and therefore the performance characteristics of the integrated circuit oscillators cannot be tailored for the specific application as is possible in oscillators composed of discrete components. However, there are many applications wherein lesser and a wide range of performance can be tolerated, and for these applications the integrated circuit offers the advantage of economy because of the smaller part count as compared with that of the equivalent discrete element circuits.

The foregoing is not meant to imply that integrated circuits play no role in the design of high-performance oscillators. For example, Section 13.5.3 discusses a high-performance oscillator, wherein linear integrated circuits are combined with discrete active and passive elements. Furthermore, Ref. 15.1 shows a special purpose high-performance oscillator, wherein a digital integrated circuit supplies all the active elements.

This chapter discusses the use of a class of digital integrated circuits, called gates, in oscillators. The gates are primarily intended for digital use; that is, in logic, data processing, and computing systems, and are therefore rated, specified, and characterized for these applications. Digital integrated circuits, characterized for oscillator use, are discussed in Chapter 16.

Oscillators, using these gates for all the active elements, are of low to moderate quality and generally have outputs, such as TTL, suitable for driving other digital circuits. Often, the gates are spares forming part of a larger digital system, and therefore no additional cost is incurred for the oscillator active elements and many of the passive elements. Provided the performance is adequate, the cost of a gate oscillator is considerably less than that of the equivalent discrete element oscillator.

Because the gates are characterized only for digital use, there are many problems in using them for oscillators. These problems are admirably discussed by Holmbeck in Ref. 15.2. The problems are primarily due to two device characteristics: the spread of triggering levels and the propagation delay, t_{PR}, through the device. It is important to note that both of these characteristics vary with environmental conditions, power supply voltage, and with individual units. Due to the triggering characteristics of digital elements within an integrated circuit device, each individual circuit may require its individual adjustment of bias in the oscillator circuit to insure that the oscillator will always start. Also, when the digital element is biased for linear operation, the oscillator will oscillate readily at frequencies determined by the propagation delay of the element and time constants external to the element. For correct oscillator design it is necessary that the unwanted modes of operation be suppressed, a task difficult to accomplish reliably because of the variation between individual units.

15.2 CLASSIFICATION OF GATE ELEMENTS

There are many groups in which the elements may be classified. Among the important groups are as follows:

1 By type and input and output voltage levels

CMOS
TTL (bipolar)
ECL (bipolar)

Note: Under certain conditions, the CMOS and TTL gates are compatible.

2 By magnitude of t_{PR}

Approx. t_{PR} (ns)	
1	ECL III
2	ECL 10,000
3	STTL (Schottky)
5	LSTTL (low-power Schottky)
10	Standard TTL
70	CMOS

3 By magnitude of power consumption

Approx. power consumption per gate (mW)	
1.3/MHz at 5 V	CMOS
2	LSTTL (low-power Schottky)
10	Standard TTL
22	STTL (Schottky)
25	ECL 10,000
60	ECL III

4 By function

BUFFER (noninverting)
BUFFER (inverting)
AND gate (noninverting)
AND gate (inverting)
OR gate (noninverting)
NOR gate (inverting)
EXCLUSIVE OR gate (inverting and noninverting)
EXCLUSIVE NOR gate (inverting and noninverting)
LINE RECEIVER (inverting and noninverting)

Notes:

1 Above 2 MHz, the CMOS power consumption is greater than that of the LSTTL.
2 The standard TTL above is the 5400/7400 series. There are other series which may have a lower or higher power consumption and smaller or larger t_{PR}.
3 Not all functions are available in all element types.
4 Two inverting elements in cascade are equivalent to a noninverting element.
5 Manufacturers' catalogues should be consulted for the latest performance data, nomenclature, and symbols.

15.3 APPLICATION OF THE VARIOUS GATE TYPES

The CMOS gate is used below about 2 MHz, the TTL up to about 50 MHz, and the ECL above 50 MHz. The LSTTL gate is now used in many applications where STTL was formerly used.

Because of the greater ease of biasing (see Section 15.4) and because of the effects of propagation delay, circuits using inverting gates have been found to be more practical than circuits using noninverting gates and are therefore in much greater use.

15.4 BIASING

As previously repeatedly stated, the oscillator small signal or the starting loop gain should be much greater than the equilibrium loop gain. Because of the noise immunity properties of the gates, the initial small-signal gain is zero, and therefore the oscillator will never start. It must therefore be biased into the quasi-linear region of operation.

15.4.1 Biasing TTL gates

Figure 15.1 shows the input output voltage characteristics for the typical TTL inverting gate. It will be noted that the desired operating point is where $V_{OUT} \approx 2$ V. This point may be obtained by connecting r_b as shown in Fig. 15.2*a*. Because of the variation between gates from unit to unit, r_b may have to be selected for each unit.

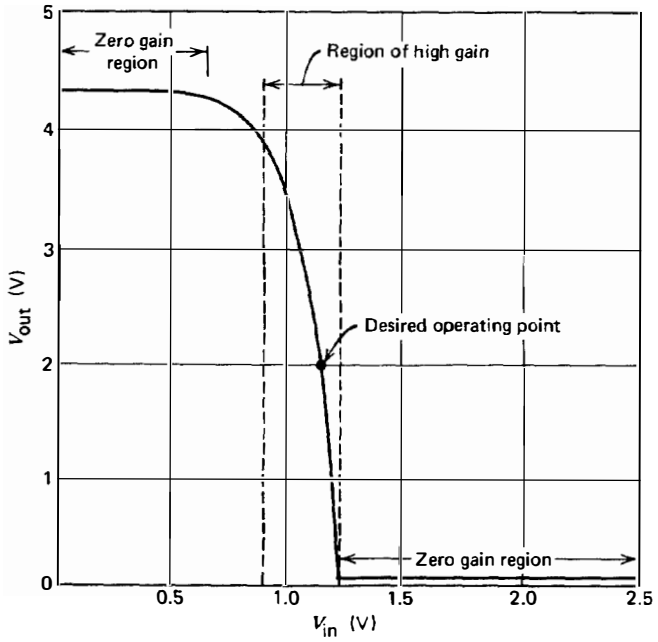

Figure 15.1 Typical TTL gate output versus input voltage characteristic.

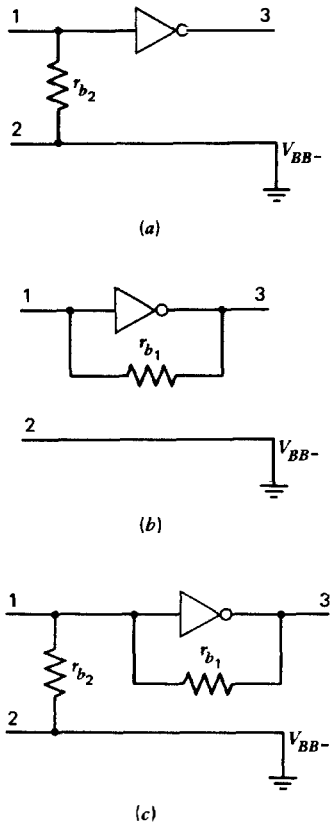

Figure 15.2 Methods of biasing TTL gates. (*a*) Method whereby the bias component does not load the resonator. (*b*) Preferred method for gate stabilization. (*c*) Combination of (*a*) and (*b*).

A more satisfactory biasing method is shown in Fig. 15.2*b*, wherein r_b is connected to provide negative feedback and will also provide a measure of stabilization for temperature variations.

Figure 15.2*c* shows the combination of Figs. 15.2*a* and 15.2*b*. In this case r_{b_1} supplies most of the bias and r_{b_2} is used to adjust the output voltage symmetry.

Often, in oscillator circuits, a resonator may be connected to points 1 and 3. r_{b_1} may then cause a serious deterioration of the resonator performance. This may be corrected by either of the two methods shown in Fig. 15.3. In Fig. 15.3*a*, L_b is inserted to make Z_b large compared to the resonator impedance. In Fig. 15.3*b*, r_{b_1} is split into r'_{b_1} and r''_{b_1} and the connecting point ac grounded by the capacitor. The result is to connect r'_{b_1} across points 3 and 2 and r''_{b_1} across points 1 and 2 which presumably already have low impedances, so that the effect of r''_{b_1} and r'_{b_1} become negligible.

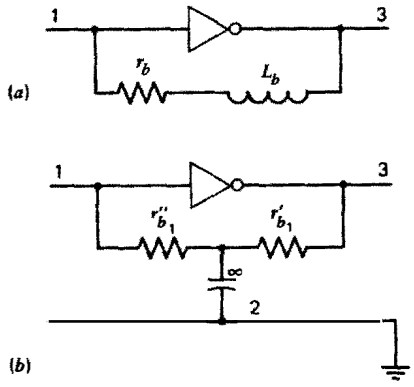

Figure 15.3 Means of eliminating the loading effect of r_{b_1}. (*a*) By inductor in series with r_{b_1}. (*b*) By partition and ac grounding.

15.4.2 Biasing CMOS Gates

Figure 15.2*a* is not applicable because of the internal configuration. However, Fig. 15.2*b* is applicable.

15.4.3 Biasing ECL Gates

Figure 15.4 shows that the proper bias is -1.3 V.

The ECL III gate is provided with a -1.3 V bias generating circuit. All that is necessary is to connect this circuit to point 1 in Fig. 15.2 via the proper ac isolating means.

The ECL 10,000 series gates must be provided with the power supply voltage divider necessary to generate the -1.3 V which is then applied to point 1 in Fig. 15.2 via the required ac isolating means.

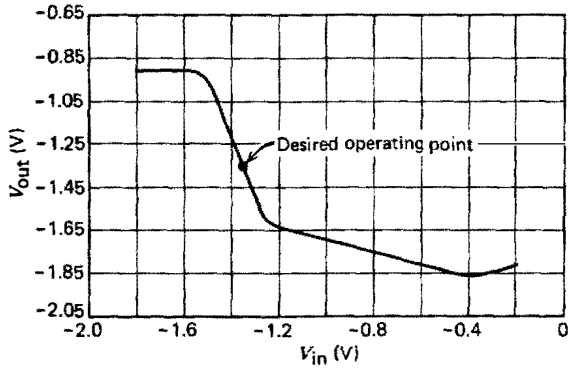

Figure 15.4 Typical ECL gate output versus input voltage characteristic.

15.5 CONVERSION OF GATES HAVING DIFFERENT FUNCTIONS INTO EQUIVALENT INVERTERS

Usually the simple inverter function is all that is required for an oscillator design. Often, other types of spare gates are available. This section demonstrates how to convert these other types into inverters.

Figure 15.5 shows how to convert NANDs, NORs, EXCLUSIVE ORs, and NORs into the equivalent inverter shown in Fig. 15.2. The inverter of Fig. 15.5*a* has a higher input impedance and is therefore suitable for an antiresonant oscillator circuit. The inverter of Fig. 15.5*b* has a lower input impedance and is therefore more suitable for series resonant oscillator circuits.

After having been converted, they are biased and otherwise treated as the inverters of Figs. 15.2 and 15.3.

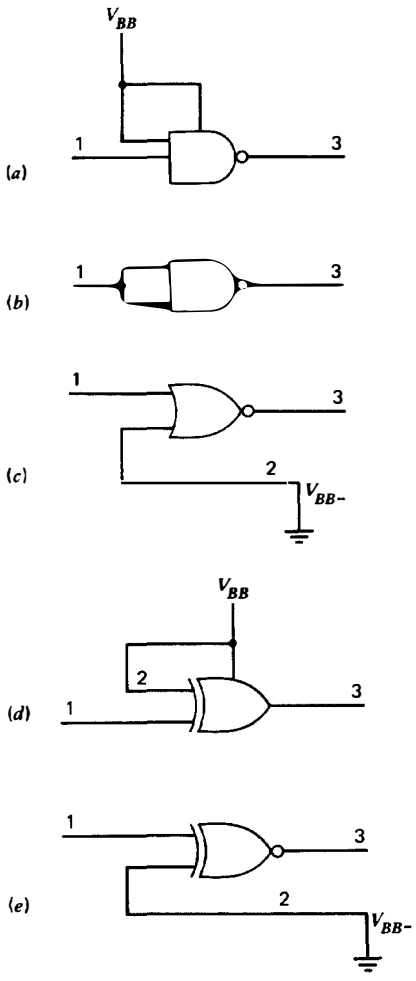

Figure 15.5 Connections for converting NAND and NOR gates into inverters. (*a*) NAND gate. (*b*) NAND gate for lower input impedance. (*c*) NOR gate. (*d*) Exclusive OR gate. (*e*) Exclusive NOR gate.

15.6 THE INVERTER APPROXIMATE EQUIVALENT CIRCUIT

Figure 15.6a shows the equivalent circuit of the inverter. In this circuit A is the gain between points 4 and 1 and is a function of frequency. It is seen from Figs. 15.1 and 15.4 that at low frequencies

$$A \approx 16 \qquad \text{for the TTL gate}$$

$$A \approx 4 \qquad \text{for the ECL gate}$$

In general

$$A = |a| \angle \theta \tag{15.1}$$

where both $|A|$ and θ are functions of f, and

$$\theta \approx -360° t_{PR} f \tag{15.2}$$

t_{PR} is in μs and f is in MHz.

From Eq. (15.2) it is seen that the gate becomes noninverting when

$$f_{NI} \approx \frac{1}{2t_{PR}} \tag{15.3}$$

No information is given in the normal gate description to evaluate the variation of A with f, but it can be stated that A decreases as f increases.

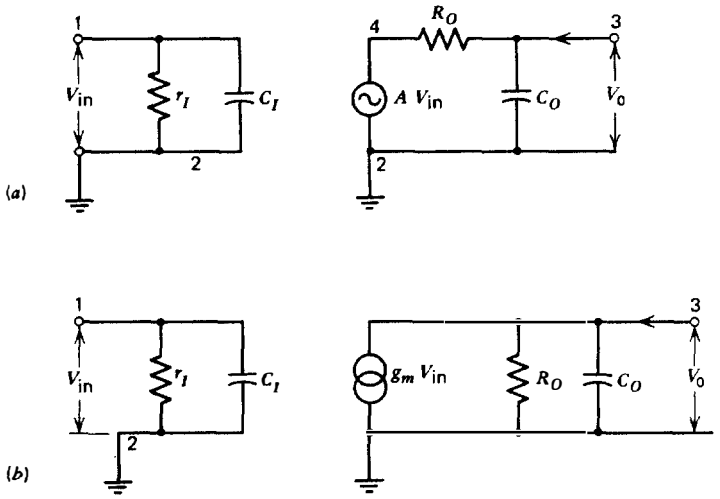

Figure 15.6 Inverter equivalent circuits. (a) Basic circuit. (b) Norton's equivalent of (a).

R_O has a low value and is approximately 5 Ω for the MEC III gate and 30 Ω for the standard TTL gate.

These values are at low frequencies and will increase and become complex as the frequency increases.

C_O is approximately 30 pF

C_I is approximately 7 pF

r_I is approximately 1200 Ω

All at low frequencies for standard TTL gates.

It should be noted that the input portion of the equivalent circuit is only valid where the effect of r_b is rendered negligible as in Fig. 15.3*a*. Otherwise,

1 r_I is in parallel with r_{b_2} in Fig. 5.2*a*.
2 r_I is in parallel with r_{b_1}/A in Fig. 15.2*b* by virtue of the Miller effect.
3 r_I is in parallel with r_b'' in Fig. 15.3*b*.

Upon applying Norton's theorem to the circuit of Fig. 15.6*a*, the circuit of Fig. 15.6*b* results. It will be noted that it is quite similar to the equivalent circuit of the transistor of Figs. 2.6*a* and 2.11. In Fig. 15.6*b*,

$$g_m = \frac{A}{R_O} \tag{15.4}$$

Therefore much of the theory developed in Chapters 5 through 10 can be applied to the gate oscillator, at least qualitatively.

It is important to be aware of the important differences between the transistor and gate equivalent circuits:

1 The gate has a much larger g_m.
2 The gate θ_{g_m} is much larger.
3 R_O is much smaller than the equivalent r_{ce} of the transistor.
4 C_O is much larger than the equivalent C_{ce} of the transistor.

These differences cause major changes in the respective oscillator design procedures.

15.7 TYPE OF LIMITING USED IN GATE OSCILLATORS

The limiting means is analogous to the collector base voltage limiter described in Section 6.2.4. As a result, the output is relatively independent of the resonator resistance, and the frequency is relatively voltage sensitive.

15.8 GATE OSCILLATORS WITH CRYSTALS OPERATING IN THE INDUCTIVE REGION

This type of oscillator is more useful than that in which the crystal operates at series resonance. This is because the circuit tuning elements tend to suppress the spurious oscillations described in Section 15.1.1. However, it requires more external components than the series resonant oscillator.

Figure 15.7*a* shows the basic model for this class of oscillators and Fig. 15.7*b* shows a typical realization. It will be recognized as the Pierce oscillator described in Chapters 5 and 7. The major difference is that the load resistance R_L is quite small, which produces a slightly smaller operating Q.

It is interesting to compute the approximate frequency shift due to the gate propagation delay.

Consider the following example:

$$f = 10 \text{ MHz}$$

$$Q_{op} \approx 25{,}000$$

the gate is the standard TTL type, and

$$t_{PR} = 10 \text{ ns}$$

Therefore

$$\theta_{g_m} = -36°$$

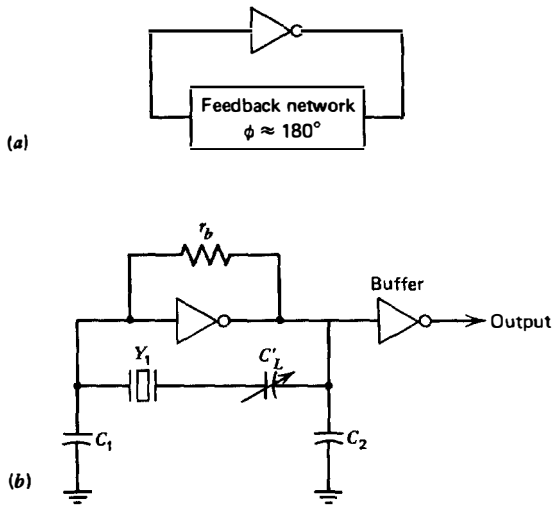

Figure 15.7 Oscillators with the crystal operating in the inductive region. (*a*) Basic model. (*b*) Typical realization of (*a*).

from Eq. (15.2) and

$$\frac{\Delta f_{\theta_{g_m}}}{f} \approx \frac{\tan(-36°)}{2(25{,}000)} = -15 \times 10^{-6}$$

from Eq. (5.18).

It should be remembered that t_{PR} is variable for many reasons; therefore its contribution to the frequency becomes a cause of frequency instability. Usually C_L' can be adjusted to compensate for the mean value of $\Delta f_{\theta_{g_m}}/f$.

An equivalent circuit can be substituted for the actual circuit. In the equivalent circuit, $\theta_{g_m} = 0$ and an inductor L_{eq} is connected in series with the crystal (see Section 19.8 and Ref. 15.2, Fig. 8) where

$$L_{eq} \approx \frac{2 \times 10^6 \Delta f_{\theta_{g_m}}/f}{(2\pi f)^2 C_1} \quad (\mu H) \tag{15.5}$$

where C_1 is the crystal motional capacitance. L_{eq} is often considered a figure of merit of the circuit although it obviously is also a strong function of the crystal characteristics.

If the crystal is an overtone, then C_1 or C_2 can be replaced by one of the networks described in Section 5.6.4 to select the desired overtone.

Figure 15.8 shows the gate oscillator version of the isolated Pierce oscillator described in Chapter 8. R_s has the following functions.

1. It provides a means of setting the crystal drive.
2. It serves to isolate the gate properties from the oscillator, so that much of the theory developed in Chapter 7 is applicable. However, the θ_{g_m} of the gate must be taken into consideration in the calculations.

At high frequencies, R_s may be replaced by a capacitor C_s to compensate for the gate propagation delay.

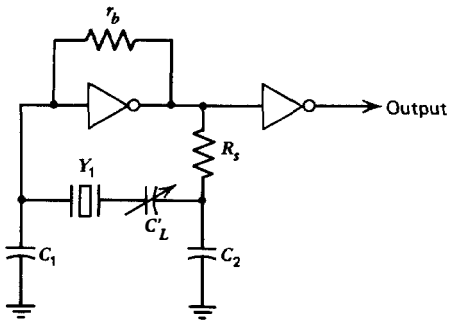

Figure 15.8 Gate oscillator version of the isolated Pierce oscillator.

15.9 GATE OSCILLATORS WITH CRYSTALS OPERATING NEAR SERIES RESONANCE

Figure 15.9*a* shows the basic model for this class of oscillators, and Fig. 15.9*b* shows a practical realization.

These oscillators, under the most favorable conditions, have the least part count, excluding the active elements, and are therefore considered desirable. However, in general their long-term frequency performance is inferior to those of Section 15.8 in which C_1 and C_2 tend to swamp the contribution of the gate to the frequency. Furthermore, they are even more prone to spurious oscillation than the oscillators of Section 15.8 because of the absence of C_1 and C_2, which limit the frequency regions of possible oscillation, and because of the higher gain due to the two gates in cascade.

In this circuit the gate inputs are connected in parallel to reduce the input impedance to better match the crystal.

Because of the two gates in cascade

$$\theta_{g_m} = 2(0.36 f t_{\mathrm{PR}}) \tag{15.6}$$

and, therefore,

$$\theta_{g_m} = -72°$$

and

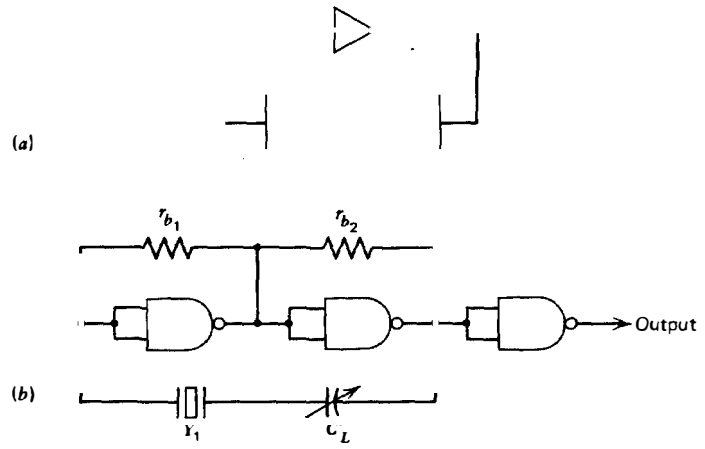

Figure 15.9 Gate oscillator with the crystal operating near series resonance. (*a*) Basic model. (*b*) Typical realization of (*a*).

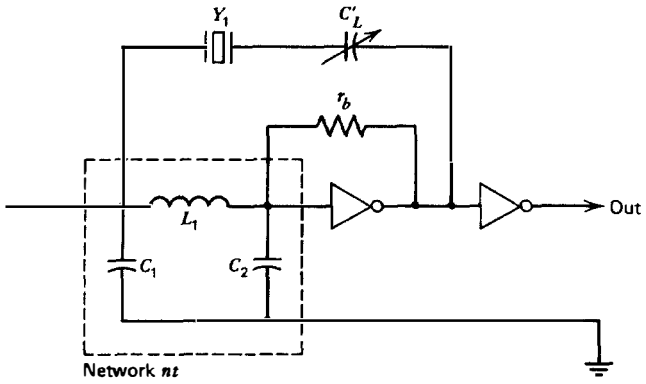

Figure 15.10 Typical high-frequency oscillator for crystal network operating near series resonance.

which is over four times that in the example in Section 15.8. Also, L_{eq} will be four times as large and C'_L will therefore become much smaller.

The oscillator of Fig. 15.9 is useful only up to moderately high frequencies as at higher frequencies the gate phase shift becomes excessive.

The oscillator of Fig. 15.10 is more suitable for high-frequency operation. In that oscillator, the required phase shift, θ, is made up of $180° + \theta_{g_m} + \theta_{nt}$.

The network, nt, performs the following functions:

1 Provides the phase shift $180° - \theta_{g_m}$.
2 Matches the gate input impedance to the crystal.
3 Selects the desired crystal overtone.

15.10 CLOSING REMARKS

The material has been presented to provide the reader with some basic theory dealing with gate oscillators. The theory, in general, will yield only qualitative results and will offer little help toward solving the problems of spurious oscillators which can only be accomplished experimentally. Accordingly, when designing gate oscillators for production it is necessary to conduct extensive experimentation to ensure the absence of spurious effects. It is quite difficult to completely eliminate the tendency for these spurious effects and a great deal of component modification may be necessary, as well as layout changes, addition of components for the sole purpose of spurious elimination, and improvements in the supply voltage bypassing. Even the choice of which gate on the chip is used may have an impact in the performance. In many cases, when spare gates are not available, it is found that the component count, using more gates for the active elements, may exceed the parts count for the more reliable discrete element circuitry or equivalent.

Those interested in the measurement of the approximate circuit equivalent parameters are referred to Chapter 19, particularly Section 19.8.

In view of the rapid development of integrated circuitry, it is possible and highly probable that much of the material on specific devices in this chapter, as well as in Chapter 16, may be rendered obsolete with the passage of time, and much improved performance may become obtainable. However, the general theory and comments will always be applicable.