8

Isolated Pierce Oscillator

8.1 INTRODUCTION

The Pierce oscillator discussed in the previous chapter has the following serious disadvantages.

1 The power output for stable oscillator design is only a small fraction of the loss in Z_3. (In crystal oscillators, Z_3 is the crystal.)
2 The isolation, meaning the effect of variation in load upon the frequency, is quite poor.

The isolated Pierce oscillator is a modification of the normal Pierce oscillator which does not have the above disadvantages. It does possess the disadvantage of being relatively difficult to design. This chapter adapts the design procedure of the previous chapter to be applicable to the isolated Pierce oscillator.

8.2 OSCILLATOR CIRCUIT ANALYSIS

8.2.1 Introduction

The *isolated Pierce oscillator* means the oscillator, the circuit schematic diagram of which is shown in Fig. 8.1. It will be noted that it is the same as that for the normal Pierce oscillator of Chapter 7 except for resistor R_s.

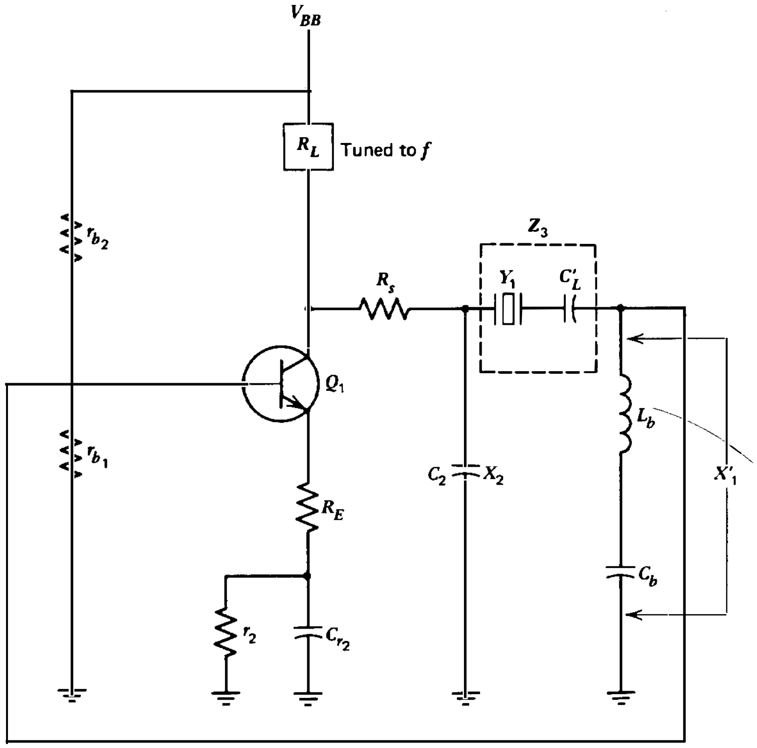


Figure 8.1 Isolated Pierce oscillator.

Figure 8.2a shows the ac equivalent circuit of Fig. 8.1. In this circuit, the transistor has been replaced by a current generator having transconductance g_m. Also the ac loading of the transistor input and bias circuits is shown as the equivalent resistances R_b and R_{in}, respectively, which have the same significance as that for the normal Pierce oscillator.

In this circuit

$$I_c = g_m V_b \tag{8.1}$$

If it is assumed that the Q of the PI circuit to the right of the dashed line exceeds 5, then

$$X_3 \approx -(X_1 + X_2) \tag{8.2}$$

$$R_n \simeq \frac{X_2^2}{R_3 + R_{\text{in}} + R_b} \tag{8.3}$$

$$I_3 \simeq I_s \frac{X_2}{R_3 + R_{\text{in}} + R_b} \tag{8.4}$$

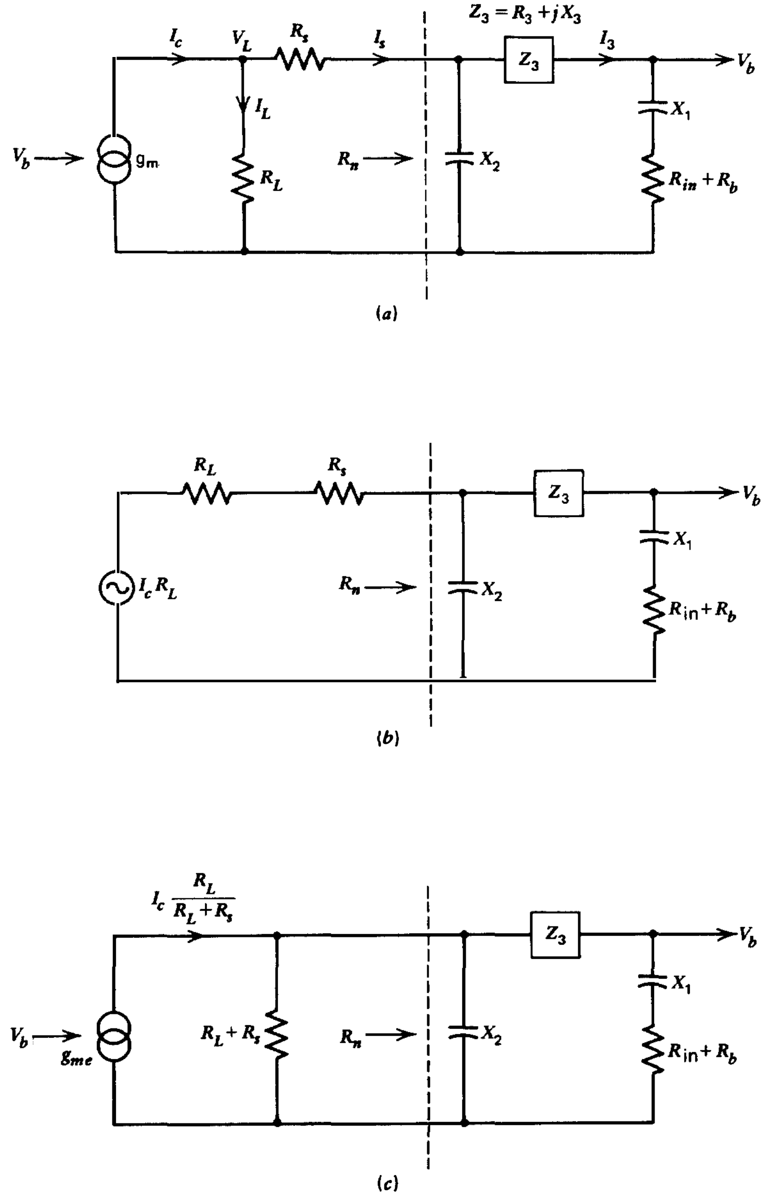


Figure 8.2 Equivalent ac circuits of isolated Pierce oscillator. (a) Equivalent circuit of Fig. 8.1. (b) Thévenin's equivalent of (a). (c) Norton's equivalent of (b).

$$I_s \simeq \frac{V_L}{R_s + R_n} \tag{8.5}$$

$$I_c = \left(1 + \frac{R_L}{R_s + R_n}\right) I_L \tag{8.6}$$

$$\simeq \left(1 + \frac{1}{m_r}\right) I_L \tag{8.6a}$$

assuming $R_s \gg R_n$ and

$$m_r \equiv \frac{R_s}{R_L} \tag{8.7}$$

$$V_b \simeq I_3 X_1 \tag{8.8}$$

$$g_m = \frac{I_c}{V_b} \simeq \frac{I_c}{I_3 X_1} \tag{8.9}$$

or

$$g_m X_1 \simeq \frac{I_c}{I_3} \tag{8.9a}$$

The conditions existing in that part of the circuit to the left of the dotted line are now known. It is very desirable to be able to use the theory developed for the Pierce oscillator in Chapters 5 and 7 to determine the conditions in the rest of the circuit.

To do so, the circuit of Fig. 8.2*a* is converted into the circuit of Fig. 8.2*c*, which is the normal Pierce oscillator circuit. This is accomplished as follows: The circuit of Fig. 8.2*a* is first converted into the Thévenin equivalent circuit of Fig. 8.2*b* by replacing the current generator with the equivalent voltage generator. Norton's theorem is then used to convert the circuit of Fig. 8.2*b* into the equivalent circuit of Fig. 8.2*c*.

8.2.2 Additional Design Equations

By definition of g_m, from Fig. 8.2*c*,

$$g_{me} = \frac{I_c R_L}{V_b(R_L + R_s)} = \frac{R_L}{R_L + R_s} g_m \tag{8.10}$$

$$= \frac{1}{1 + m_r} g_m \tag{8.10a}$$

Assuming

$$R_3 + R_{in} + R_2 \gg R_b \tag{8.11}$$

then

$$R_T \simeq R_2 + R_{in} + R_3 \tag{8.12}$$

Let

$$R_t = R_3 + R_{in} \tag{8.13}$$

and let

$$X_2 = nR_t \tag{8.14}$$

It is recommended that

$$n \geqq 5 \tag{8.14a}$$

then

$$R_n \simeq \frac{X_2^2}{R_t} \tag{8.15}$$

$$= 25R_t \qquad \text{for } n = 5 \tag{8.15a}$$

From Eq. (8.5),

$$I_s = \frac{V_L}{R_s + 25R_t} \qquad \text{for } n = 5 \tag{8.16}$$

From Eq. (8.4)

$$I_3 \simeq \frac{V_L}{R_s + R_n} \frac{X_2}{R_t} \tag{8.17}$$

$$\simeq \frac{I_L R_L}{R_s + R_n} \frac{X_2}{R_t} \tag{8.17a}$$

$$\approx \frac{I_L R_L}{R_s} \frac{X_2}{R_t} \qquad \text{when } R_n \ll R_s \tag{8.17b}$$

The last equation may be written, from Eqs. (8.6) and (8.9), as

$$I_3 \equiv \frac{1}{1 + m_r} I_c \frac{X_2}{R_t} \tag{8.17c}$$

It is interesting to formulate the relations for

$$\eta = \frac{P_L}{p_3} \tag{8.18}$$

$$\eta = \frac{V_L^2}{R_L}\left(I_3^2 R_3\right)^{-1} \tag{8.18a}$$

$$= \frac{(R_s + R_n)^2}{R_L R_3 (X_2/R_t)^2} \qquad \text{from Eq. (8.17)} \tag{8.18b}$$

$$= \frac{R_s^2}{25 R_L R_3} \qquad \text{for } n = 5 \text{ and } R_s \gg R_n \tag{8.18c}$$

Equation (8.18b) is very useful for determining the power ratio for given values of R_s and R_L. It is very interesting that large values of R_n and large values of R_s/R_L yield large η. However, the maximum value of R_s is limited to the largest *practical* value of R_s which at high frequencies is not very large.

If Eq. (8.18b) is solved for R_s, then

$$R_s = \frac{X_2}{R_t}\sqrt{\eta R_3 R_L} - R_n \tag{8.19}$$

$$\approx \frac{X_2}{R_t}\sqrt{\eta R_3 R_L} \qquad \text{when } R_s \gg R_n \tag{8.19a}$$

Equation (8.19) may be used for determining R_s for a given η.

Equation (8.9a) states that

$$g_m X_1 = \frac{I_c}{I_3}$$

which, from Eqs. (8.6) and (8.17a), is

$$= \frac{R_s + R_n + R_L}{R_L X_2/R_t} \tag{8.20}$$

$$\simeq \frac{1 + m_r}{X_2/R_t} \tag{8.20a}$$

when $R_s + R_L \gg R_n$.

The general basic oscillatory equation discussed at great length in Chapters 5 and 7 states that

$$g_{me} X_1 X_2 = R_T \tag{8.21}$$

It will be found after calculating the values of the components that Eq. (8.21) will not be completely satisfied because of the approximations made during the derivations. For example, R_T, from Eq. (8.21), using the values for X_1, X_2, and g_{me} calculated in the algorithm, is always less than that given by Step 17 in the algorithm.

The relationship between the two can be shown to be

$$\frac{R_T(\text{of Step 17})}{R_T(\text{of Eq. (8.21)})} \approx \frac{R_s + R_n}{R_s} \tag{8.22}$$

This discrepancy can be corrected by replacing X_2 by X_2' where

$$X_2' = nR_T \tag{8.23}$$

Therefore, Eq. (8.21) becomes

$$g_{me}X_1X_2' = R_T \tag{8.24}$$

and

$$C_2 = \frac{159{,}000}{fX_2'} \tag{8.25}$$

8.2.3 Practical Values of R_s

Section 1.2.1.7 states that the maximum realizable resistor value is

$$R_{\text{max}} = \frac{32{,}000}{f}$$

This is based upon $X_{C_p} > 10R$.

In this application, it is sufficient to make

$$X_{C_p} > 5R;$$

therefore,

$$R_{\text{max}} = 64{,}000/f \tag{8.26}$$

8.2.4 Oscillator Design for Minimum Power Consumption

It is obvious that, for minimum power consumption, R_L should be maximum. R_L is determined by the following:

1 The BV_{CE} of the transistor.
2 The maximum physically realizable R_L.
3 The value of $\eta = P_L/P_x$.

Items 1 and 2 are fully treated in Section 7.2.4. Item 3 will now be discussed.

Equation (8.18b) may be rewritten

$$R_L = \frac{R_s^2}{n^2 R_3 \eta} \qquad \text{for } R_s \gg R_n \tag{8.27}$$

It is seen that, for R_L to be maximum, R_s must be maximum, which however is limited as stated in Eq. (8.26). Therefore, from Eqs. (8.27) and (8.26)

$$R_{L_{\max}} = \frac{(64{,}000)^2}{f^2 n^2 R_3 \eta} \tag{8.28}$$

The value of R_L to be used is the smaller of the values as determined by item 1, item 2, and/or Eq. (8.28).

8.3 LIMITING

Since it is desirable to maintain the output power independent of the resistance, R_3, and since the isolating characteristic of this oscillator renders the frequency much less sensitive to changes in supply voltage than in the normal Pierce oscillator, it is in order to use collector base limiting. Accordingly, the material in Section 7.2.4.1 is applicable to this design. However, for very small output power, Section 7.2.4.2 is applicable, as base emitter cutoff limiting is then in order. Often, the algorithm will alert the user that a different type of limiting is called for by calculating a negative value for r_{b_2}. The preparation of the algorithm for base emitter cutoff limiting is left to the reader as an exercise, using the other algorithms as a guide.

8.4 THE DESIGN PROCEDURE

The design procedure is similar to that for the normal Pierce oscillator described in Section 7.4, except for the modification demanded by the conversion from the isolated Pierce oscillation to the normal Pierce oscillation as described in Section 8.2. The procedure is surprisingly straightforward for the relatively complex oscillator circuit.

8.5 ALGORITHM AND DESIGN EXAMPLES

8.5.1 The Design Algorithm for the Isolated Pierce Oscillator (Algorithm 12.3)

See Section 7.5.1 for some pertinent remarks which are also applicable to this algorithm.

The algorithm has been prepared for maximum conversion efficiency consistent with the transistor characteristics, maximum practical load resistance, and the desired $\eta = P_L/P_x$.

The algorithm has been prepared on the basis that the g_m design procedure is the same as that for the normal Pierce oscillator. This basis allows the operating Q to vary widely depending on P_L/P_x. Another basis could have been to attempt to make the ratio of Q_{op}/Q_x a predetermined value, as is done in the normal Pierce oscillator, but this often results in unrealizable circuits; that is, some of the components are calculated to be negative. The basis used renders the algorithm very simple and always results in realizable circuits.

8.5.2 Design Examples for Algorithm 12.3

Design Examples 8.1 and 8.2 are the design examples for this algorithm. They have been chosen to illustrate the effects of large frequency differences and large crystal resistance differences. Both examples have the same P_L and η.

R_L in Design Example 8.1 was fixed by the maximum realizable value of R_s, while R_L in Design Example 8.2 was fixed by the BV_{CE} of the transistor. It will be noted that the conversion efficiency of Design Example 8.2 is considerably greater than that of Design Example 8.1. This is due to the larger R_L.

C_2 in Design Example 8.2 is rather small for an oscillator at 0.8 MHz. This is due to the very large crystal resistance. R_{df}/R_T, cited in the tables, equals Q_{op}/Q_x.

In both examples, η is 100, which is much larger than that in the normal Pierce circuit, typically $\frac{1}{3}$. The major advantage of this oscillator is thereby demonstrated.

8.5.3 Trimming for Algorithm 12.3

8.5.3.1 Introduction

See Section 7.5.3.1.

8.5.3.2 Basis of the Trimming Procedure

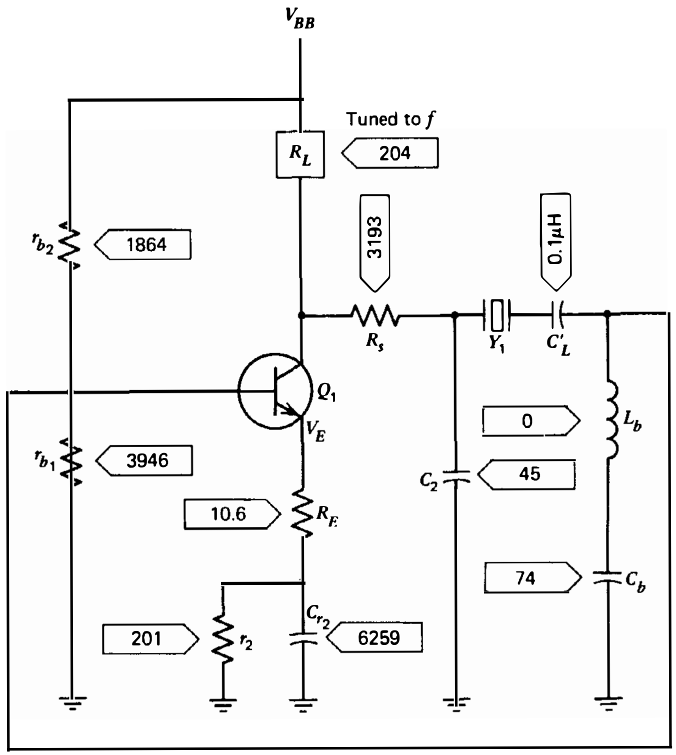
The trimming is based upon the following approximate relations, many of which are similar to those for the normal Pierce oscillator, but are repeated here for convenience.

1 $$|V_L| \propto V_{CE} \tag{7.47}$$

2 $$P_L \propto \frac{V_L^2}{R_L} \tag{7.50}$$

3 $$|V_b| \approx |I_3||X_1| \tag{7.49}$$

4 $$P_x \approx P_L \frac{25 R_L R_x}{R_s^2} \qquad \text{from Eq. (8.18c)} \tag{8.29}$$

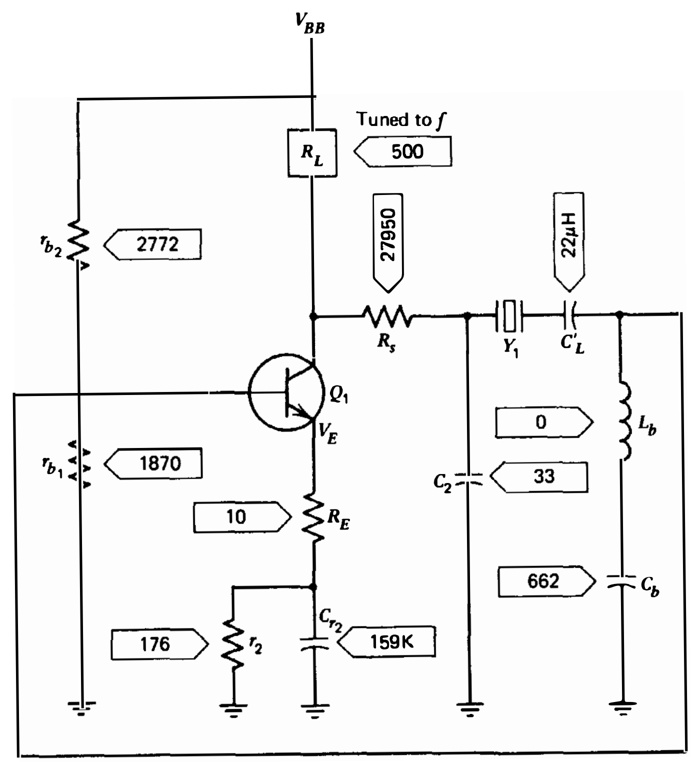


Design Example 8.1 Isolated Pierce oscillator.

All units in

℧ MHz Ω mW pF μH
mA, mV dc or rms

	Item	Value
Oscillator Performance	f	20
	P_L	50
	P_x	0.5
	V_{BB}	10,000
Principal Crystal Data	R_{df}	20
	I_x	5
	Cut	AT
	N	1
Transistor Data	β_o	30
	f_T	700
	BV_{CE}	15,000
	C_{cb}	1
	C_{bet}	2
	C_{ce}	2
	P_{dis}	
	Type	2N918
Circuit Parameters	A_{Lo}	2
	n	5
	η	100
Calculated Data	I_{BB}	25.6
	g_m	0.039
	V_E	4937
	R_{df}/R_T	0.56



Design Example 8.2 Isolated Pierce oscillator.

All units in

℧ MHz Ω mW pF μH
mA, mV dc or rms

	Item	Value
Oscillator Performance	f	0.8
	P_L	50
	P_x	0.5
	V_{BB}	10,000
Principal Crystal Data	R_{df}	625
	I_x	.89
	Cut	AT
	N	1
Transistor Data	β_o	30
	f_T	700
	BV_{CE}	15,000
	C_{cb}	1
	C_{bei}	2
	C_{ce}	2
	P_{dis}	
	Type	2N918
Circuit Parameters	A_{L_0}	2
	n	5
	η	100
Calculated Data	I_{BB}	16.5
	g_m	0.04
	V_E	2644
	R_{df}/R_T	0.518

8.5.3.3 Typical Trimming Steps

The following describes the action required to increase a given characteristic. Obviously, the opposite action decreases the same characteristic.

8.5.3.3.1 Output Power P_L

Equation (7.50) states that increasing V_L or decreasing R_L will increase the power. V_L, in turn, can be increased by increasing V_{CE}, as required by Eq. (7.47), by adjusting r_{b_1} and r_{b_2}. At the same time, it may be necessary to decrease r_2 for proper limiting action. Similarly, decreasing R_L may require adjustments of the dc biasing.

8.5.3.3.2 Crystal Power P_x

Equation (8.27) states that decreasing R_s will increase P_x. Also, any action that will increase P_L will also increase P_x. Decreasing R_x will also tend to decrease P_x, as stated in the same equation.

8.5.4 Frequency Instability Due to Variation in Components Other than Z_3

Obviously, variations in components due to time, environment, and component defects will produce variations in frequency. What is particularly interesting is the effect of variations caused by the operator such as changes in R_L and tuning of the output circuit.

Changes in R_L will produce frequency changes smaller than those in the equivalent normal Pierce oscillator because of the isolation provided by R_s as is evident from Fig. 8.2*c*. The isolation increases as the ratio R_s/R_L increases and as the ratio R_s/X_2 increases.

A problem not present in the normal Pierce oscillator is the tuning of the load R_L. The entire analysis assumes that R_L is resistive, but if it is improperly tuned, R_L becomes Z_L, which is a complex impedance of magnitude and phase angle, depending upon the tuning. Equation (8.10) more correctly should be

$$g_{me} = \frac{Z_L}{Z_L + R_s} g_m \tag{8.30}$$

which in turn is a complex transconductance, even when g_m is real. Therefore, one would expect a change in frequency as Z_L is tuned. The extent of this change can be computed as described in Section 5.4 and may be substantial. This effect can be used constructively as a fine frequency tuning adjustment.