7

The Normal Pierce Oscillator

7.1 INTRODUCTION

This chapter develops the additional and/or modified relations of Chapter 5 required to design this type of oscillator. It also contains comments about the practical aspects of the design. Finally, it formulates two design algorithms—one for each of the major types of limiting of Section 6.2. The algorithms are specifically applicable to the self-limiting types of crystal oscillator, but they are also useful for non-self-limiting types and oscillators with other two-terminal resonators.

By the normal Pierce oscillator is meant the oscillator first shown in Fig. 5.1*a* and now repeated in a modified form in Fig. 7.1. All the components in this figure are physical; that is, they are all installed components. However, there are additional resistors and capacitors which form part of the transistor. This chapter will show how to compute the values of the physical components which when combined with the transistor properties will produce a prespecified oscillator performance.

7.2 OSCILLATOR CIRCUIT ANALYSIS

7.2.1 Introduction

As stated in Section 5.5.1, the Pierce circuit is basically the same as the Colpitts oscillator and all the theory developed in Chapter 5 for the Colpitts oscillator

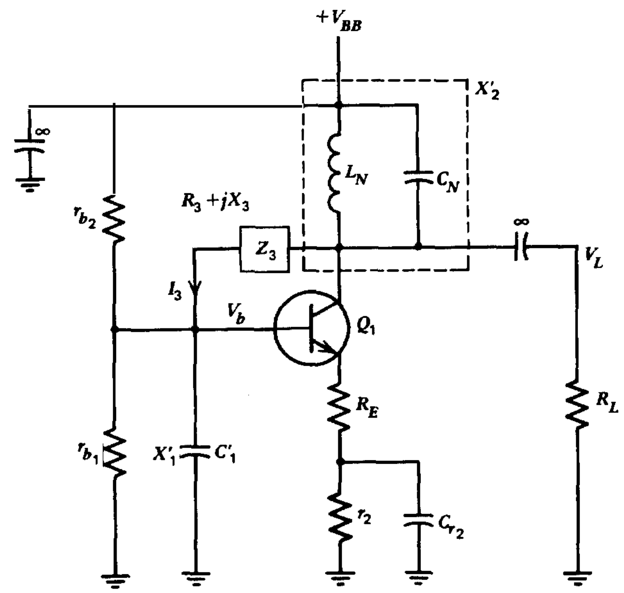


Figure 7.1 Pierce oscillator detailed schematic.

applies, with slight simplifications, to the Pierce oscillator. Since the analysis of the Colpitts oscillator was based upon the detailed ac circuit schematics of Fig. 5.9, it is instructive to show similar schematics for the Pierce oscillator.

Figures 7.2*a*, 7.2*b*, and 7.2*c* are analogous schematics for the Pierce oscillator corresponding to Figs. 5.9*a*, 5.9*b*, and 5.9*c* for the Colpitts oscillator, and Section 5.5 should be consulted for the derivation of these schematics. It will be noted that the only difference is, apart from the change of datum point (ground), that r_b is across X_1 in the Pierce oscillator, while r_b is across $X_1 + X_2$ in the Colpitts oscillator. This seemingly trivial difference has the following important effects:

1 r_b has a considerably smaller loading effect and results in a higher operating Q in the Pierce oscillator.
2 The Pierce oscillator is easier to design.

7.2.2 Modified Equations

Some of the equations derived in Chapter 5 have to be modified as follows:

Equation (5.40) now becomes

$$R_T = R_3 + \frac{X_1^2}{r_{be'}} + \frac{X_1^2}{r_b} + \frac{X_2^2}{R_L} = g_m X_1 X_2 \qquad (7.1)$$

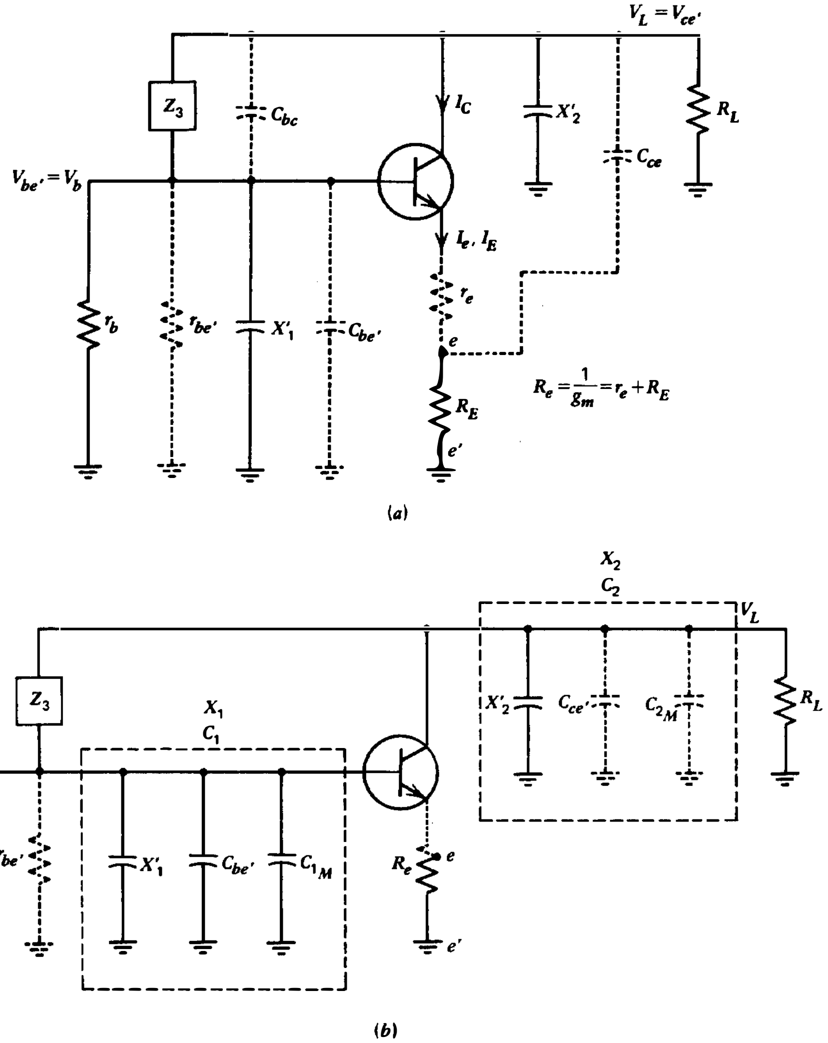


Figure 7.2 Pierce oscillator. (*a*) Detailed schematic of the ac circuitry. *Note*: $i_C \approx i_E$. (*b*) Modified schematic, Step 1. (*c*) Modified schematic, Step 2.

where by definition (see Section 5.5.3) and Eq. (5.40)

$$\frac{X_1^2 g_m}{\beta_o} = \frac{X_1^2}{r_{be'}} \equiv R_{\text{in}} \tag{7.2}$$

$$\frac{X_1^2}{} = R \tag{7.3}$$

$$\frac{X_2^2}{R_L} \equiv R_2 \tag{7.4}$$

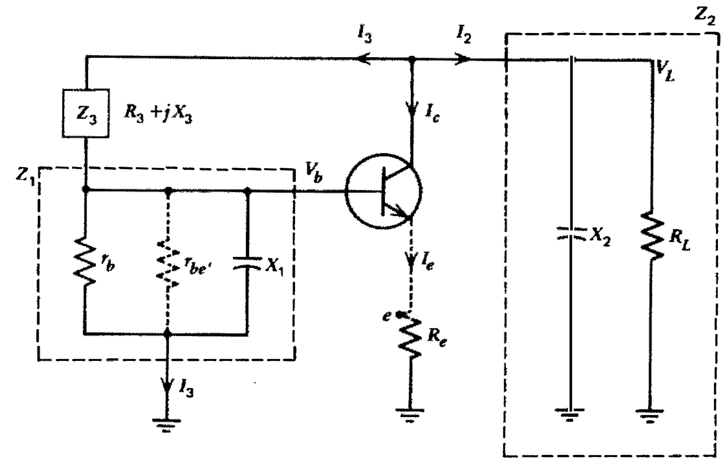


Figure 7.2 (*Continued*).

Also,

$$V_b = I_3 Z_1 \approx -jI_3 X_1 \tag{7.5}$$

and

$$|V_b| \approx |I_3||X_1| \tag{7.5a}$$

Equation (5.59) becomes

$$\frac{|I_3|}{|I_e|} = \frac{|X_2|}{R_T} \tag{7.6}$$

where R_T is defined in Eq. (7.1). Equation (5.65) becomes

$$V_L = I_3[R_3 + R_{\text{in}} + R_b + jX_2] \tag{7.7}$$

or

$$|V_L| = |I_3|\sqrt{(R_3 + R_{\text{in}} + R_b)^2 + X_2^2} \tag{7.8}$$

The relationships presented in this chapter deserve greater elaboration, but an adequate presentation is prohibited by space limitations. Equations (7.1) to (7.7) particularly merit close examination, as their significance changes substantially with the type of limiting. Some of these aspects will be treated in the following sections.

7.2.3 Fundamental Design Equations

By definition

$$|I_c| = g_m|V_b| = g_m|I_3|X_1 \tag{7.8}$$

from Eq. (7.:

$$1000P_L = \frac{V_L^2}{R_L} \tag{7.9}$$

$$1000P_{Z_3} = I_3^2 R_3 \tag{7.9a}$$

Let

$$\eta \equiv \frac{P_L}{P_{Z_3}} = \frac{V_L^2}{I_3^2 R_3 R_L} \tag{7.10}$$

or

$$\eta = \frac{(R_3 + R_{\text{in}} + Rb)^2 + X_2^2}{R_3 R_L} \qquad \text{'rom Eq. (7.7)} \tag{7.11}$$

$$= \frac{\qquad}{R_L R_3} \qquad \text{:rom Eq. (7.4)} \tag{7.12}$$

solving for R_2

$$R_2 = \frac{\eta R_L R_3 - (R_3 + R_{\text{in}} + R_b)^2}{R_L} \tag{7.13}$$

$$= \eta R_3 - \frac{(R_3 + R_{\text{in}} + R_b)^2}{R_L} \tag{7.14}$$

When a design is first started, the values of R_{in} and R_b are unknown. If it is assumed that

$$R_3 \gg R_{\text{in}} + R_b \tag{7.15}$$

then Eq. (7.14a) becomes

$$R_2 \approx \eta R_3 - \frac{R_3^2}{R_L} \tag{7.16}$$

and from Eq. (7.1),

$$R_T \approx R_3 + R_2 \tag{7.17}$$

Also from Eq. (5.77),

$$Q_{op} \approx \frac{Q_{Z_3}R_3}{R_3 + R_2} = \frac{Q_{Z_3}}{1 + (R_2/R_3)} \tag{7.18}$$

which becomes, from

$$Q_{op} \approx \frac{Q_{Z_3}}{1 + \eta - R_3/R_L} \tag{7.19}$$

Usually,

$$1 + \eta \gg \frac{R_3}{R_L} \tag{7.20}$$

therefore

$$Q_{op} \approx \frac{Q_{Z_3}}{1 + \eta} \tag{7.21}$$

which states that for small degradations of Q, η must be small.

If a degradation of Q_{Z_3}, of approximately 25% is allowed, then

$$\eta \approx 0.33$$

which is a recommended value.

Equations (7.10) and (7.21) state that for small Q degradation, the output power is much smaller than the Z_3 power.

Equation (7.16) should be further investigated. This equation states

$$R_2 \approx \eta R_3 - \frac{R_3^2}{R_L}$$

Occasionally, R_2 calculates as being a negative quantity, which is obviously physically impossible. What it does mean is that the design is unsound. The only way of correcting this defect is to increase R_L, which in turn requires increasing V_L, which in turn requires increasing the BV_{CE} of the transistor and, possibly, V_{BB}.

7.2.4 Discussion of $V_{L_{max}}$ and R_L

Obviously, the larger V_L is, the greater is the power output, but $V_{L_{max}}$ is limited by the BV_{CE} of the transistor; and the relationship of BV_{CE} to $V_{L_{max}}$ will now be explored. BV_{CE} is emphasized over BV_{CB} because in every silicon transistor BV_{CB} is considerably larger than BV_{CE}.

The relationships are different for the collector limited and the *be* cutoff oscillators. This difference is caused by the fact that in the collector base voltage limited oscillator, V_L is relatively independent of R_3 for a given oscillator. However, Eqs. (2.79), (7.1), and (7.5) state that as R_3 decreases in an oscillator designed for *be* cutoff limiting, I_3 increases. Equation (7.7), in turn, states that V_L increases, although not as fast as I_3 increases. Particularly, when Z_3 is a crystal, R_3, of necessity, varies from unit to unit and provision must be made in the circuit to allow for the variation.

7.2.4.1 Calculation of $V_{L_{max}}$ for the Collector Base Limiting Oscillator

Figure 7.3 shows the voltage relationships in this type of limiting. V_e is shown approximately equal to V_b to provide a factor of safety, although V_e is appreciably smaller than V_b.

By inspection it is seen that

$$v_{CE_{max}} = v_{C\max} - v_{E_{min}}$$

$$\approx 2.8\left(V_{L_{max}} + V_b\right) \tag{7.22}$$

assuming $V_b = V_e$.

But $$v_{CE_{max}} \leqq BV_{CB}$$

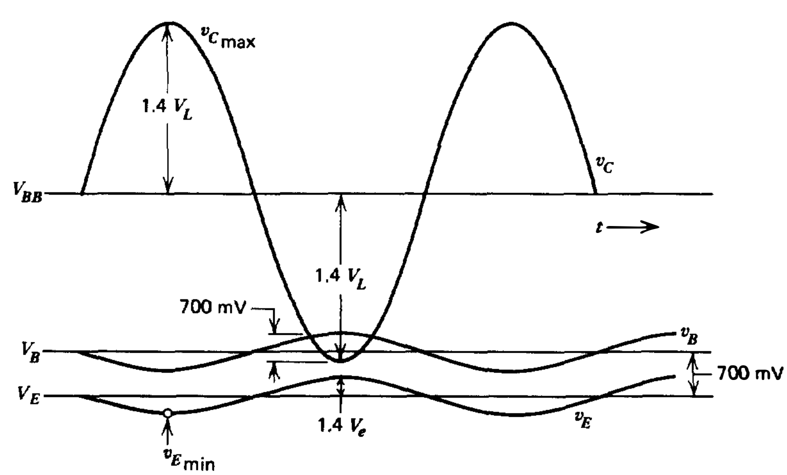


Figure 7.3 Voltage relationships for collector base limiting in the Pierce oscillator.

therefore,

$$V_{L_{max}} \leqq \frac{BV_{CE} - 2.8V_b}{2.8}$$

$$\leqq 0.357BV_{CE} - V_b \tag{7.23}$$

To compensate for $-V_b$,

$$V_{L_{max}} \approx 0.33BV_{CE} \tag{7.23a}$$

7.2.4.2 Calculation of $V_{L_{max}}$ for the be Cutoff Limiting Oscillator

Figure 7.4 shows the voltage relationships in this type of limiting. In this oscillator $v_{B_{max}}$ must be less than $v_{C_{min}}$ for Z_3 having the minimum R_3. Since the oscillator is designed for $R_{3_{max}}$, when V_L is minimum, provision must be made for the increase of V_L as R_3 decreases. Let

$$\frac{R_{3_{max}}}{R_{3_{min}}} = 2 \tag{7.24}$$

then

$$\frac{V_{L_{max}}}{V_{L_{min}}} \approx 1.5 \tag{7.25}$$

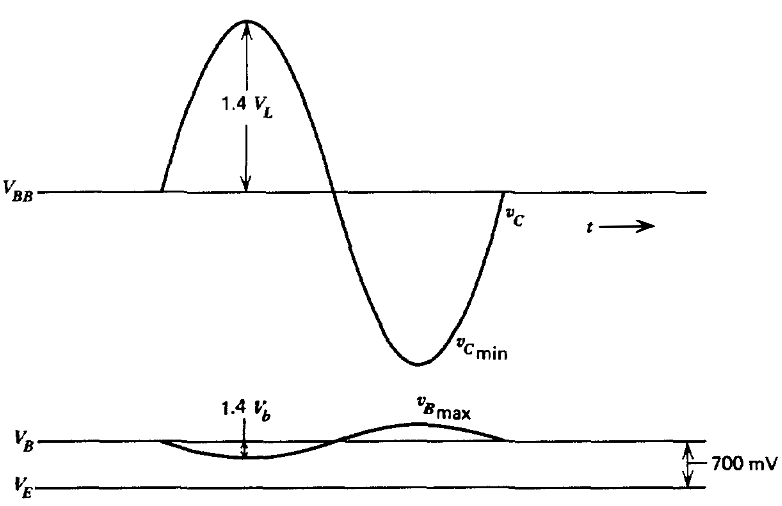


Figure 7.4 Voltage relationships for base emitter cutoff limiting in the Pierce oscillator.

and from Eq. (7.23a)

$$V_{L_{\max}} = \frac{0.33}{1.5} BV_{CE} = 0.22 BV_{CE} \tag{7.26}$$

7.2.4.3 Calculation of V_E, Which Should Be Greater Than 2 V

7.2.4.3.1

It is evident from Fig. 7.3 that for collector limiting,

$$V_E = V_{BB} - 1.4(V_L + V_b) \tag{7.27}$$

7.2.4.3.2

Similarly, from Fig. 7.4, for *be* cutoff limiting,

$$V_E = V_{BB} - (\geqq 2.1)(V_L + V_B) \tag{7.28}$$

It is very desirable that $v_{CE_{\min}} = v_{C_{\min}} - v_{E_{\max}}$ in Fig. 7.4 exceed 1700 mV to ensure proper operation of the transistor at high frequencies. Therefore, Eq. (7.28) becomes

$$V_E = V_{BB} - (\geqq 2.1)(V_L + V_B) - 1700 \tag{7.28a}$$

Equation (7.28a) sets a value of 1700 mV for $v_{CE_{\min}}$. However, it is desirable that $v_{CE_{\min}}$ be larger than 1700 mV. This is usually possible for the common values of V_{BB} and for small V_L.

Consider the following example (all units in mV):

$$V_{BB} = 10{,}000, \qquad V_L = 200, \qquad V_b = 113$$

Then, from Eq. (7.28a), $V_E = 7642$.

This results in the following situation:

1 $v_{CE_{\min}}$ is calculated to be 1700.
2 r_2 will dissipate an excessive part of the available V_{BB}.
3 V_{CE} will be difficult to maintain because of the tolerances and available standard values of components.

This situation is not tolerable because it can be remedied. It is therefore recommended that the procedure below be followed:

1 Calculate V_{E_1} by Eq. (7.28a).
2 If $V_{E_1} > V_{BB}/2$, make

$$V_E = \frac{V_{BB}}{2} \tag{7.28b}$$

3 If $V_{E_1} \leqq V_{BB}/2$, make

$$V_E = V_{E_1} \tag{7.28c}$$

In the above example, $V_E = 5000$, which now makes $v_{CE_{\min}} = 4342$, a preferable value.

7.2.4.4 Calculation of R_L and Its Effect upon V_L

Once $V_{L_{\max}}$ is known, R_L is found from

$$R_L = \frac{V_{L_{\max}}^2}{1000P_L} \tag{7.29}$$

Often, R_L computed from Eq. (7.29) is too large and cannot be physically realized at the operating frequency f.

Equation (1.16) states that

$$R_L \leqq \frac{10{,}000}{\sqrt{f}}\ \Omega$$

If this value of R_L is substituted into Eq. (7.29),

$$V_L = \sqrt{\frac{10^7 P_L}{\sqrt{f}}} \tag{7.30}$$

for P_L in mW, V_L in mV, and f in MHz. Obviously, V_L must then be made the smaller of the values obtained from Eq. (7.30) and Eqs. (7.23a) or (7.26) as applicable.

7.2.5 Calculation of the Approximate g_m When R_2, X_1, and X_2 Have Already Been Computed

From Eq. (7.1),

$$R_T = R_3 + R_2 + R_{\text{in}} + R_b = g_m X_1 X_2$$

and neglecting R_b because it is unknown:

$$R_T \approx R_3 + R_2 + R_{\text{in}} \tag{7.31}$$

From Eq. (7.2),

$$R_{\text{in}} = \frac{X_1^2}{r_{be'}} \tag{7.32}$$

and from Eq. (5.114)

$$r_{be'} = \frac{\beta_o}{g_m}$$

Therefore,

$$R_T = R_3 + R_2 + \frac{X_1^2 g_m}{\beta_o} = g_m X_1 X_2 \tag{7.33}$$

Solving for g_m

$$g_m = \frac{(R_3 + R_2)}{X_1(X_2 - X_1/\beta_o)} \tag{7.34}$$

7.2.6 Some Miscellaneous Reactance Formulas

7.2.6.1

$$C = \frac{1}{2\pi f X_C} \quad \text{(general formula)} \tag{7.35}$$

or

$$C = \frac{159{,}000}{f X_C} \tag{7.36}$$

where C is in pF, f is in MHz, and X_C is in Ω.

7.2.6.2

$$L = \frac{X_L}{2\pi f} \tag{7.37}$$

where L is in μH, f is in MHz, and X_L is in Ω.

7.2.6.3

$$X_{C_{r_2}} = \frac{0.05}{g_m} \tag{7.38}$$

$X_{C_{r_2}}$ is made very small compared to $1/g_m$, the dynamic emitter resistance.

7.2.6.4 Calculation of C_L'

A crystal resonator rated at antiresonance is required to work into a load capacitance $C_{L_{df}}$ to be at its rated frequency f. Normally the capacitance equivalent of $X_1 + X_2$ is much larger than $C_{L_{df}}$. Therefore a capacitance C_L' has to be connected in series, and it is

$$X_{C_L'} = \left[\frac{159{,}000}{C_{L_{df}} f} - (X_1 + X_2)\right] \tag{7.39}$$

and

$$C_L' = \frac{159{,}000}{X_{C_L'} f} \tag{7.40}$$

7.3 FREQUENCY VARIATIONS DUE TO EXTERNAL FACTORS

The frequency variation, caused by changes in load impedance and power supply voltages, is treated in this section.

7.3.1 Frequency Variation Due to Changes in the Load R_L

The treatment will consider changes only of the magnitude of R_L and will assume that the load remains resistive. Extension of the treatment to other types of load variation will be obvious to the reader.

In Fig. 7.2*c*, the load R_L is across the reactance X_2. Normally, since $R_L \gg X_2$, Z_2 can be written

$$Z_2 = \frac{X_2^2}{R_L} + jX_2 \tag{7.41}$$

but, in this case, the small changes in X_2 are important, so the complete impedance expression must be used.

$$Z_{2_n} = R_{2_n} + jX_2 = \frac{R_{L_n}(jX_2)}{R_{L_n} + jX_2} = \frac{R_{L_n} X_2^2}{R_{L_n}^2 + X_2^2} + j\frac{R_{L_n}^2 X_2}{R_{L_n}^2 + X_2^2} \tag{7.42}$$

It is seen that when R_L is changed to R_{L_2} from R_{L_1}, then

$$\Delta X_2 = \frac{R_{L_2}^2 X_2}{R_{L_2}^2 + X_2^2} - \frac{R_{L_1}^2 X_2}{R_{L_1}^2 + X_2^2} \tag{7.43}$$

Then the fractional frequency shift due to the change in R_L will be

$$\frac{\Delta f}{f} = \frac{\Delta X_2}{\left(\Delta X_3 (\Delta f/f)^{-1}\right)} \tag{7.44}$$

where $(\Delta X_3(\Delta f/f)^{-1})$ is defined in Step b10 of the algorithms.

Example

$$X_2 = 120, \qquad R_{L_1} = 2000, \qquad R_{L_2} = \infty \text{ (open circuit)},$$

$$\left(\Delta X_3(\Delta f/f)^{-1}\right)_{\text{crystal}} = 2 \times 10^6\ \Omega$$

then

$$\frac{\Delta f}{f} = \frac{120 - 119.57}{2 \times 10^6} = 2.1 \times 10^{-7}$$

7.3.2 Frequency and Amplitude Variation Due to Change in the Supply Voltage V_{BB}

The frequency variation is very difficult to calculate since it is influenced mainly by minute variations in the transistor characteristics with supply voltage change. However, some useful qualitative conclusions can be obtained.

7.3.2.1 Frequency Variations Independent of Type of Limiting

In general, when the voltage V_{BB} is increased, C_{bet} C_{ce}, and C_{cb} decrease and f_T increases. All of these changes produce an increase in frequency.

7.3.2.2 Frequency and Amplitude Variations in Oscillators with Emitter Base Cutoff Limiting

The oscillation equation (7.1) is rewritten here with some slight change in notation applicable to the Pierce oscillator.

$$R_T = \frac{X_2^2}{R_L} + R_3 + \frac{X_1^2}{r_b} = g_m\left[X_1X_2 - \frac{X_1^2}{\beta_o}\right] \tag{7.45}$$

Examination of the terms, X_2^2/R_L, R_3, X_1^2/r_b, X_1, and X_2 discloses that they are independent of signal amplitudes. If it is assumed that β_o is also independent of signal amplitude, then it follows from Eq. (7.45) that g_m is also independent of signal amplitude. If g_m is independent of signal amplitude, all effects, excluding those that are listed in Section 7.3.2.1, that may influence the frequency are also independent of signal amplitude. Therefore, there is no frequency change due to change of V_{BB}.

Equation (7.1) gives no information on the amplitude change due to the change in V_{BB}. To calculate the new signal strength V_L the following procedure is followed:

1 Calculate the new I_E using the equations in Section 2.5.
2 Calculate $I_e = 1.4I_E$. This is because $\gamma_1 = 1.4$.
3 Calculate $|V_L| = |I_2|X_2$ from Eq. (5.59a).

When the above steps are followed, it will be found that V_L is proportional to I_E, which in turn is proportional to V_{BB}, when V_E is much larger than 700 mV.

7.3.2.3 Frequency and Amplitude Variation with Collector Base Voltage Limiting

As V_{BB} increases, the output increases almost proportionally since V_{CB} increases proportionally and $V_{CB} \approx 1.4(V_L + V_b)$.

The tendency at the same time is for g_{mL} to increase. This produces the following effects:

1 C_{bed} increases.
2 r_{be} decreases.
3 r_{ce} decreases.

The effect of point 1 is to decrease the frequency, while the effects of points 2 and 3 are to increase the frequency, so that it is difficult to be certain whether the frequency will increase or decrease. However, these effects, combined with that of Section 7.3.2.1, usually will cause the frequency to increase as the voltage supply is increased.

7.4 THE DESIGN PROCEDURE

The design procedure can best be described as a series of levels of successive approximations. At each approximation level, the known information is used to calculate additional quantities which are then incorporated into the original information to form the basis for the next approximation level.

The rather arbitrary criterion, for termination of the design procedure, is that it is terminated at the end of the level where

$$R_T < 1.1R'_T \tag{7.46}$$

where R'_T is the value of R_T at the beginning of the level and R_T is the value at the end. R_T is defined in Eq. (7.1).

The number of levels never exceeds two, so that the design procedure is not excessively long and tedious. In general, the Pierce oscillator design requires only one level of approximation. After the levels of approximation described above have been completed, the resulting quantities are translated into the real physical components which make up the oscillator. This translation is performed taking into account the mode of operation of the resonator.

The procedures described above have been applied to several specific single transistor self-limiting crystal oscillators and are presented in the form of algorithms to render the complete design a formal, logical, and readily executable process (see Chapter 12).

7.5 THE PIERCE OSCILLATOR, COLLECTOR BASE LIMITING

7.5.1 The Design Algorithm for This Oscillator (Algorithm 12.1)

Algorithm 12.1 is contained in Chapter 12. It is recommended that Section 12.2 be read before using the algorithm.

The user has to supply the information requested in Sections a, b, c, and d. It will be noted that items c7, c9, c10, and c11 are not used in the algorithm but checks should be made, after completion of the design, to make sure that these values are not exceeded.

As noted in Eq. (6.18)

$$A_{L_0} = \frac{g_{m_{L0}}}{g_m}$$

Since the loop gain is proportional to g_m and the loop gain, at stable oscillation, equals 1, it follows that A_{L_0} is the *small-signal* loop gain.

The algorithm has been prepared for oscillators with crystal networks operating in the inductive mode; however, it is easily adaptable for replacement of the crystal network by another two-terminal network, such as an inductor of reactance value $\approx -(X_1 + X_2)$ at the desired frequency.

Section 1.2.1.6 states that the algorithms have been prepared on the basis of maximum practical conversion efficiency. This means that the load resistances are the maximum practical. If for any reason a smaller load resistance, R_L, is desired in the normal Pierce and Colpitts oscillators, it is necessary to

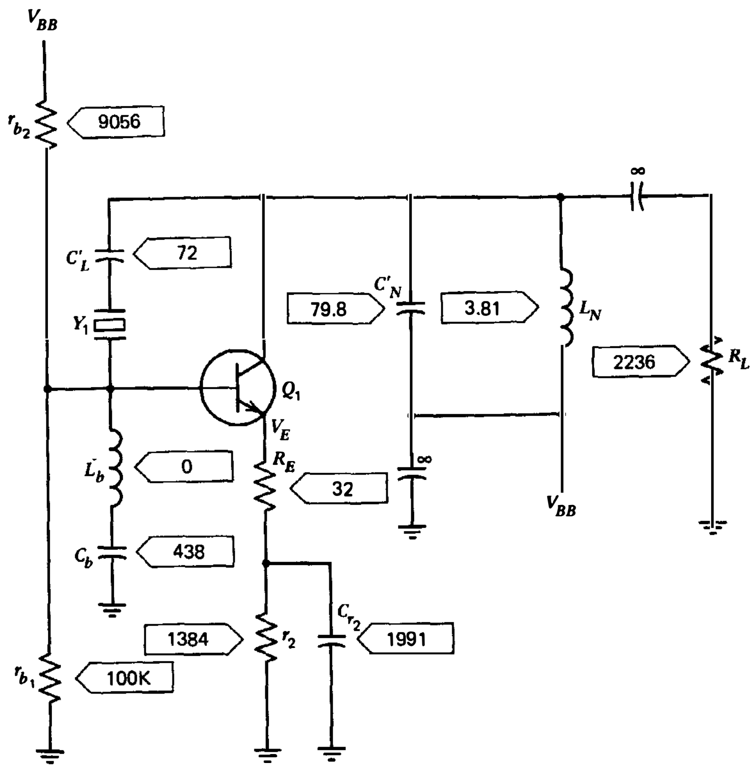
1 Insert the desired R_L in Step 3.
2 Calculate the new V_L corresponding to the new P_L and R_L.
3 Insert the new V_L in Step 2.
4 Continue with the execution of the algorithm.

The algorithms in general, although there are some obvious exceptions, include the design of an SC crystal mode selector making up X_1 (see Section 5.6.5.3). For very small I_x, the physical realization of the mode selector becomes impractical; for example, C_b becomes too small. In that case, X_1 should be the equivalent C_1' and the mode selector should be one of the types shown in Fig. 5.13 (see Section 5.6.5.4).

7.5.2 Design Examples for Algorithm 12.1

Design Examples 7.1 and 7.2 are included as examples of designs calculated from the algorithm. The important data is stated in the table and the calculated circuit components values are those on the circuit diagram.

Examples are given for 2 frequencies. Examination of the data on Design Example 7.1 shows that the design is unsatisfactory in that V_{CE} is too small to

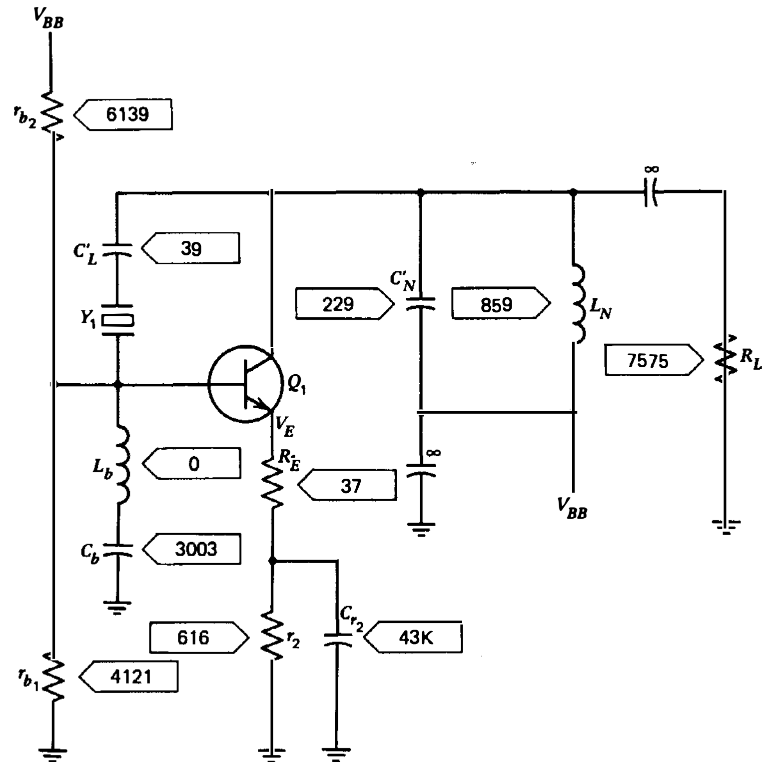


Design Example 7.1 Pierce oscillator, collector base voltage limiting.

All units in

℧ MHz Ω mW pF μH
mA, mV dc or rms

	Item	Value
Oscillator Performance	f	20
	P_L	1.66
	P_x	5
	V_{BB}	10,000
Principal Crystal Data	R_{dj}	20
	I_x	15.8
	Cut	AT
	N	1
	C_L	32
Transistor Data	β_o	30
	f_T	700
	BV_{CE}	15,000
	C_{cb}	1
	C_{bet}	2
	C_{ce}	2
	P_{dis}	
	Type	2N918
Circuit Parameters	A_{L_0}	2
	η	0.33
Calculated Data	I_{BB}	5.14
	g_m	0.0125
	V_E	6914



Design Example 7.2 Pierce oscillator, collector base voltage limiting.

All units in

℧ MHz Ω mW pF μH
mA, mV dc or rms

	Item	Value
Oscillator Performance	f	0.8
	P_L	3.3
	P_x	10
	V_{BB}	10,000
Principal Crystal Data	R_{df}	625
	I_x	4
	Cut	AT
	N	1
	C_L	32
Transistor Data	β_o	20
	f_T	300
	BV_{CE}	15,000
	C_{cb}	1
	C_{bet}	2
	C_{ce}	2
	P_{dis}	
	Type	2N2369A
Circuit Parameters	A_{L_0}	2
	η	0.33
Calculated Data	I_{BB}	5.11
	g_m	.011
	V_E	2634

be closely controlled and excessive variation in output will result due to variations in transistor characteristics and component values. It may be stated, in general, that this type of design is unsatisfactory for low P_x and/or very high frequencies.

Normally,

$$\frac{R_2^2}{R_L} \approx \eta R_{df}$$

but Design Example 7.2 is a case where this is not true. This is because R_{df}^2/R_L is not negligible compared to ηR_{df}.

Line c3 of the algorithm requires that $f_{T_{min}}$ be 150 and 5.3 MHz, and line c2 requires $\beta_{o_{min}}$ be 15 and 13 for Design Examples 7.1 and 7.2, respectively. It will be noted that these requirements are met by the transistors specified. Also, at the same frequency, the required $f_{T_{min}}$ is approximately proportional to the square root of the output power.

7.5.3 Trimming for Algorithm 12.1 (see Fig. 7.1)

7.5.3.1 Introduction

After the prototype is constructed, using the nearest standard values for the components, it is tested. Some adjustment may then be found necessary to make the measured performance identical to the specification performance. The adjustment process is called *trimming* and this section discusses the trimming procedure.

7.5.3.2 Basis of the Trimming Procedure

The trimming is based upon the following approximate relations:

1. $$|V_L| \propto V_{CE} \tag{7.47}$$
   from Eq. (7.23a).
2. $$|I|_3 \approx V_L/\sqrt{R_3^2 + X_2^2} \tag{7.48}$$
   from Eq. (7.8).
3. $$|V_b| \approx |I_3||X_1| \tag{7.49}$$
   from Eq. (7.5a).
4. $$P_L \propto V_L^2/R_L \tag{7.50}$$
5. $|V_b|$ and I_E must be maintained so that the proper type of limiting is in effect. This is a rather broad requirement and will permit a large range of $|V_b|$ and I_E, the values of which must be optimized for lowest X_1 and highest conversion efficiency consistent with the variations in transistor properties. This may involve changes in the values of r_2, R_E, r_{b1}, and r_{b2}.

Note: For a crystal resonator $I_3 \equiv I_x$.

7.5.3.3 Typical Trimming Steps

The following describes the action required to increase a given characteristic. Obviously, the opposite action decreases the same characteristic.

7.5.3.3.1 Output Power P_L

Equation (7.50) states that increasing V_L or decreasing R_L increases the power. V_L, in turn, can be increased by increasing V_{CE}, as required by Eq. (7.47), by adjusting r_{b1} and r_{b2}. At the same time, it may be necessary to decrease r_2 for proper limiting action. Similarly, decreasing R_L may require adjustments of the dc biasing.

7.5.3.3.2 Current I_3 (I_X in Crystal Oscillators)

Equation (7.48) states that I_3 can be increased by increasing V_L and/or decreasing X_2. Any action that will increase V_L also increases I_3 (see Section 7.5.3.3.1). Decreasing X_2 is accomplished by increasing C'_N. Of course, adjusting V_L will also affect the power output.

It is interesting to note that Eq. (7.48) also implies that changing C'_1 will have little effect on I_3. The same equation states that the current increases slightly as R_3 decreases so that if a new crystal with lower $R_{df} \equiv R_3$ is used, the current increases but at a slow rate, so that in the case where $X_2 > R_3$, I_3 may be considered constant as R_3 varies.

7.5.4 Frequency Instability due to Variations in Components, Other Than Z_3

Section 5.9 presents a stability analysis of this type of oscillator. Study of this analysis discloses that for maximum stability, X_1 and X_2 should be minimized. However, the requirements of power output, Z_3 power loss, operating Q, and conversion efficiency dictate the values of X_1 and X_2 as outlined in the algorithms. Accordingly, not much can be done for increasing the stability without changing the other performance characteristics. For example, increasing the power input substantially will permit a reduction in X_2. Also, increasing the power supply voltage will permit greater stabilization of the dc bias circuit and thus increase the oscillator stability.

7.6 THE PIERCE OSCILLATOR, *be* CUTOFF LIMITING

7.6.1 The Design Algorithm for This Oscillator (Algorithm 12.2)

The user has to supply the information requested in Sections a, b, and c. It will be noted that items c7, c9, c10, and c11 are not in the algorithm but checks should be made after completion of the design to make sure that these values are not exceeded.

In Section d, 0.3 has been chosen as the recommended value of α because it is comfortably within the straight-line portion of Fig. 2.12*b*. This value of α also corresponds to the saturation value of γ_1 and to relatively small values of γ_2 and γ_3 as shown in Fig. 2.12*c*. This value of α also produces a small-signal loop gain of 3.3 which is considered satisfactory.

The comments in Section 7.5.1 about replacement of the crystal networks by another network, about replacing the calculated R_L by another R_L, and about the crystal mode selector apply equally well here.

7.6.2 Design Examples for Algorithm 12.2

Design Examples 7.3, 7.4, 7.5, and 7.6 are included as examples of designs calculated from this algorithm. The input data is stated in the table and the calculated circuit component values are shown on the circuit diagram.

Examples are given for two frequencies and two power levels.

Examination of Design Example 7.4 shows the design is satisfactory for low power. The conversion efficiency is very poor and can be improved by increasing the power supply voltage.

Design Example 7.5 and 7.6 are the same design except for power supply voltage. It will be noted that the higher voltage yields the higher efficiency. This is due to the fact that the higher voltage permits a higher load impedance. Design Example 7.5 is defective in that it requires a β_o min of 55, which means that a higher β transistor is necessary.

Comparison of these examples with Design Examples 7.1 and 7.2 discloses that the *be* limiting designs are more efficient than the collector voltage limiting designs. Also the values of C_1' are considerably different in the two designs. This again confirms the fact that satisfactory designs are possible over a wide range of values.

7.6.3 Trimming for Algorithm 12.2

See Fig. 7.1.

7.6.3.1 Introduction

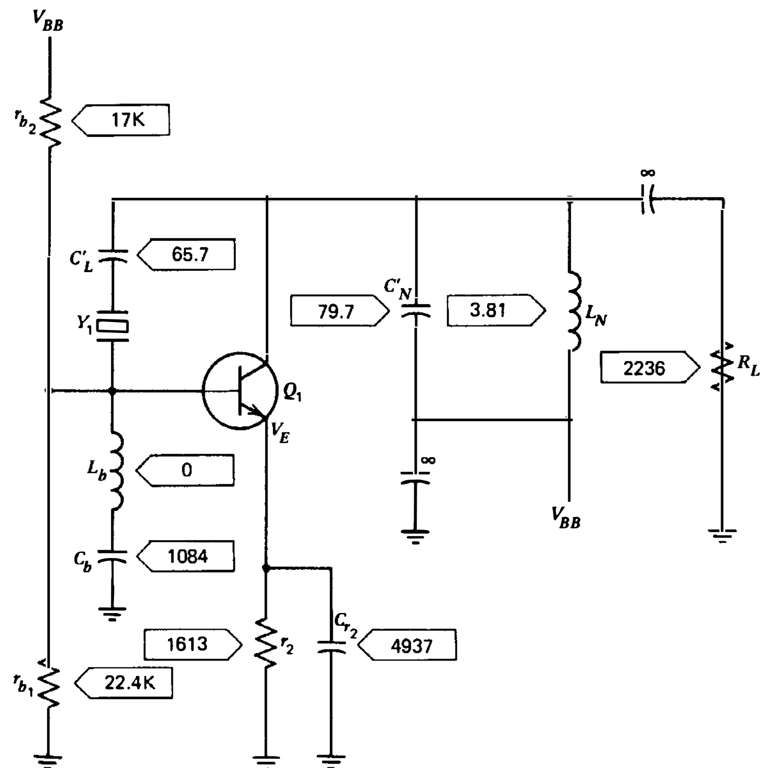
See Section 7.5.3.1.

7.6.3.2 Basis of the Trimming Procedure

The trimming is based upon the following relations:

1
$$I_e \approx 1.4 I_E \tag{7.51}$$
from Fig. 2.12*b*.

2
$$|V_L| \approx |I_3|\sqrt{R_T^2 + X_2^2} \tag{7.52}$$
from Eq. (7.8)
$$\approx |I_e|\frac{|X_2|}{R_T}\sqrt{R_T^2 + X_2^2} \tag{7.53}$$

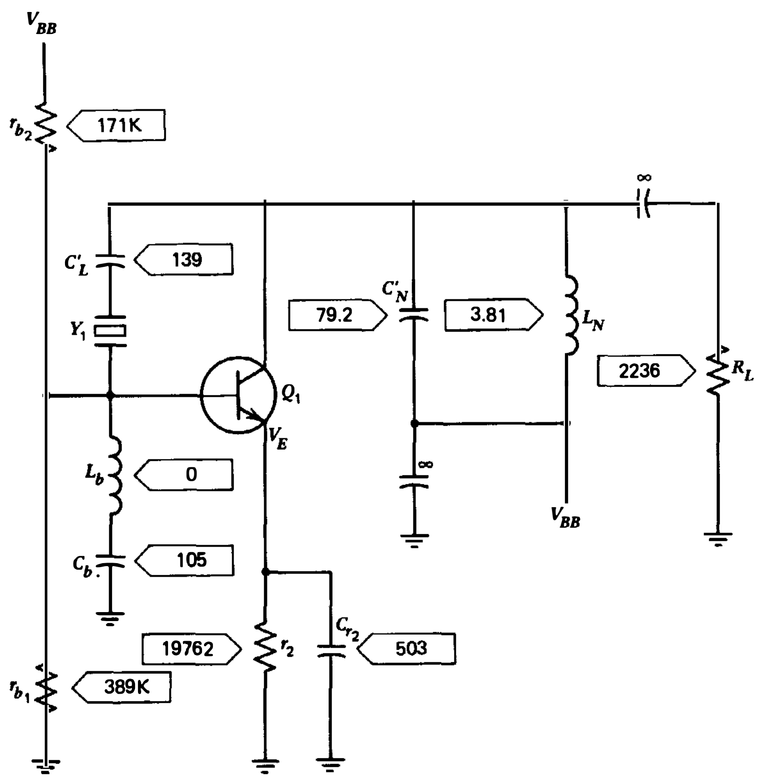


Design Example 7.3 Pierce oscillator, base emitter cutoff limiting.

All units in

℧ MHz Ω mW pF μH
mA, mV dc or rms

	Item	Value
Oscillator Performance	f	20
	P_L	1.66
	P_x	5
	V_{BB}	10,000
Principal Crystal Data	R_{df}	20
	I_x	15.8
	Cut	AT
	N	1
Transistor Data	β_o	30
	f_T	700
	BV_{CE}	15,000
	C_{cb}	1
	C_{bei}	2
	C_{ce}	2
	P_{dis}	
	Type	2N918
Circuit Parameters	α	0.3
	γ_1	1.4
	V_{be}	113
	η	0.33
Calculated Data	I_{BB}	2.84
	g_m	0.030
	V_E	4018

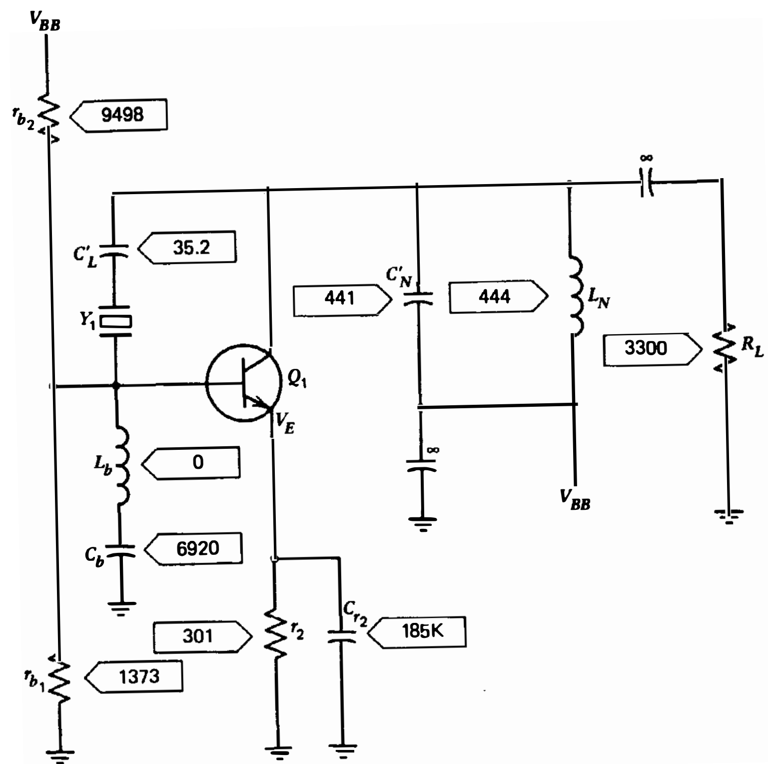


Design Example 7.4 Pierce oscillator, base emitter cutoff limiting.

All units in

℧ MHz Ω mW pF μH
mA, mV dc or rms

	Item	Value
Oscillator Performance	f	20
	P_L	0.0166
	P_x	0.05
	V_{BB}	10,000
Principal Crystal Data	R_{df}	20
	I_x	1.58
	Cut	N
	N	1
Transistor Data	β_o	30
	f_T	700
	BV_{CE}	15,000
	C_{cb}	1
	C_{bet}	2
	C_{ce}	2
	P_{dis}	
	Type	2N918
Circuit Parameters	α	0.3
	γ_1	1.4
	V_{be}	113
	η	0.33
Calculated Data	I_{BB}	0.28
	g_m	0.003
	V_E	5000

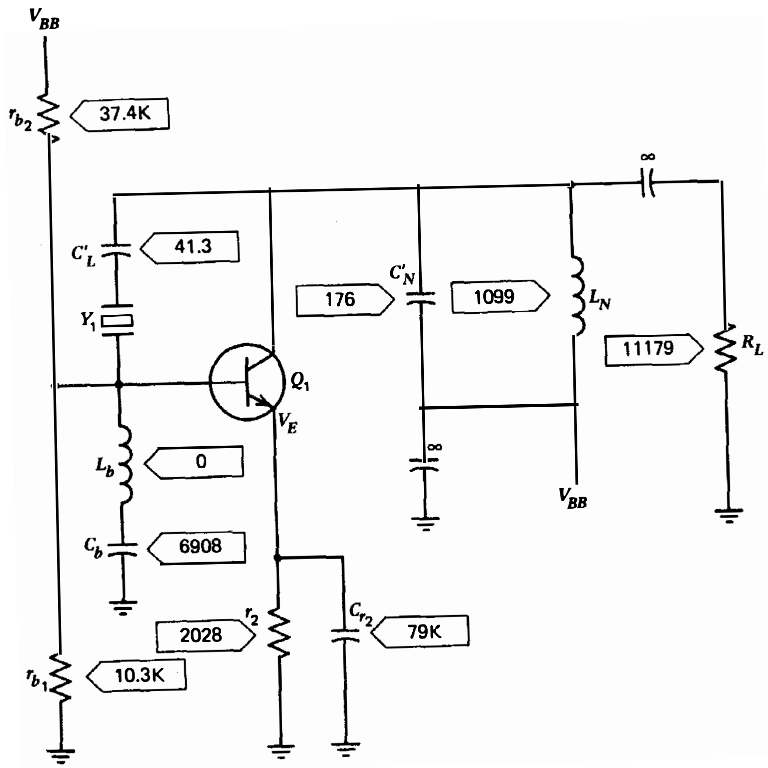


Design Example 7.5 Pierce oscillator, base emitter cutoff limiting.

All units in

℧ MHz Ω mW pF μH
mA, mV dc or rms

	Item	Value
Oscillator Performance	f	0.8
	P_L	3.3
	P_x	10
	V_{BB}	10,000
Principal Crystal Data	R_{df}	625
	I_x	4
	Cut	AT
	N	1
Transistor Data	β_o	20
	f_T	250
	BV_{CE}	15,000
	C_{cb}	1
	C_{bel}	2
	C_{ce}	2
	P_{dis}	
	Type	2N2369A
Circuit Parameters	α	0.3
	γ_1	1.4
	V_{be}	113
	η	0.33
Calculated Data	I_{BB}	4.69
	g_m	0.046
	V_E	1132



Design Example 7.6 Pierce oscillator, base emitter cutoff limiting.

All units in

℧ MHz Ω mW pF μH
mA, mV dc or rms

	Item	Value
Oscillator Performance	f	0.8
	P_L	3.3
	P_x	10
	V_{BB}	18,000
Principal Crystal Data	R_{df}	625
	I_x	4
	Cut	AT
	N	1
Transistor Data	β_o	20
	f_T	250
	BV_{CE}	30,000
	C_{cb}	1
	C_{bet}	2
	C_{ce}	2
	P_{dis}	
	Type	2N222
Circuit Parameters	α	0.3
	γ_1	1.4
	V_{be}	113
	η	0.33
Calculated Data	I_{BB}	2.03
	g_m	0.02
	V_E	3307

from Eqs. (7.6) and (7.52)

3 $$|I_3| = |I_e|\frac{|X_2|}{R_T} \tag{7.54}$$

from Eq. (7.6).

4 $$V_b \approx I_3 X_1 \tag{7.49}$$

from Eq. (7.5a).

5 $$P_L \propto V_L^2/R_L \tag{7.50}$$

6 Section 7.5.3.2(5) is applicable here.

Note: For a crystal resonator, $I_3 = I_x$.

7.6.3.3 Typical Trimming Steps

The following describes the action required to increase a given characteristic. Obviously, the opposite action decreases the same characteristic.

7.6.3.3.1 Output Power P_L

Equation (7.50) states that increasing V_L or decreasing R_L will increase the power. V_L, in turn, can be increased by increasing I_E or X_2, as stated in Eq. (7.53). I_e is increased by increasing I_E, as stated in Eq. (7.51). I_E is increased by adjusting r_{b_1}, r_{b_2}, and/or r_2.

7.6.3.3.2 Current I_3 (I_x in Crystal Oscillators)

Equation (7.54) states that I_3 increases as I_e and/or X_2 are increased. Any action that will increase V_L will also increase I_3. (See Section 7.6.3.3.1.) Increasing X_2 is accomplished by decreasing C_N'. If it is desired to change I_3 without changing V_L, it is necessary to adjust R_L for the required power, after I_3 has been adjusted.

It is interesting to note that Eq. (7.54) implies that changing C_1' will have little effect on I_3. The same equation states that I_3 increases as R_3 decreases so that if a new crystal with lower R_{df} is used, the current will increase but at a much more rapid rate than in Section 7.5.3.3.2 because of the difference in Eqs. (7.48) and (7.54).

7.6.4 Frequency Instability Due to Variations in Components Other Than Z_3

See Section 7.5.4.

7.7 MEASUREMENT TECHNIQUES FOR THE PIERCE OSCILLATOR (SEE ALSO CHAPTER 19)

The Pierce oscillator is unique in that it facilitates meaningful measurements since the emitter is ac grounded and since most measuring instruments have one of their terminals grounded. This section discusses some of the types of measurements, which are relatively easy in the Pierce oscillator but much more difficult in other oscillator configurations.

7.7.1 Measurement of I_3 in Fig. 7.1

In a crystal oscillator Z_3 is the crystal and therefore $I_3 = I_x$. I_3 is determined by measuring or calculating $|Z_1|$, which is the impedance from the base to ground, and then measuring V_b with a high-impedance RF voltmeter. Then

$$|I_3| = \frac{|V_b|}{|Z_1|} \tag{7.55}$$

For greater accuracy, the voltmeter loading should be included in $|Z_1|$.

7.7.2 Measurement of Q_{op} in Crystal Oscillators

There are many procedures by which Q_{op} can be measured. This section describes a relatively easy procedure for measuring the approximate Q_{op}.

From Eqs. (7.5) and (7.7)

$$\frac{V_L}{V_b} \approx \frac{R_T + jX_2}{-jX_1} \approx A\angle\theta \tag{7.56}$$

where

$$R_T \approx R_3 + R_{in} + R_b \tag{7.57}$$

assuming $R_2 \to 0$. Solving for θ

$$\theta \approx \tan^{-1}\frac{X_2}{R_T} + \frac{\pi}{2} \tag{7.58}$$

and

$$\frac{\partial\theta}{\partial f} \approx \frac{(1/R_T)(\partial X_2/\partial f)}{1 + (X_2/R_T)^2} \tag{7.59}$$

assuming R_T is constant over the range of f.

$$\approx \frac{(1/R_T)(\partial X_2/\partial f)}{1 + \tan^2(\theta - \pi/2)} \tag{7.59a}$$

from Eq. (7.58). Since X_1 is constant over the range of f,

$$Q_{\text{op}} = \frac{f}{2}\left|\frac{\partial\theta}{\partial f}\right|\left[1 + \tan^2\left(\theta - \frac{\pi}{2}\right)\right] \tag{7.60}$$

from Eqs. (5.77) and (7.59a).

Equation (7.60) shows how Q_{op} is measured, which may be summarized as follows:

1. A small shift in frequency, ∂f, is produced by changing X_2 slightly.
2. θ and $\partial\theta$ are measured by means of a vector voltmeter, set up to measure V_b and V_L. (Note: The meter reads θ in degrees. This should be converted to radians.)
3. Q_{op} is computed with Eq. (7.60).