6 Limiting

6.1 INTRODUCTION

In Chapter 1 (Section 1.1.1) we stated that an oscillator must include a nonlinearity called *limiting* which maintains the oscillation amplitude in stable equilibrium. This section presents an explanation of the limiting processes and the various types of limiters. This has been only sketchily treated in the literature, and an attempt is therefore made to develop a formal logical treatment of this rather difficult and somewhat vague subject.

By limiting is meant the reduction of the effective transconductance or loop gain of an oscillator as the amplitude increases. The limiter may take the following basic forms:

1 Self-limiter—which means that the amplifier producing the oscillations limits its gain by its own nonlinear action. Most oscillators use a single transistor as the amplifier and limiter and are, therefore, the self-limiting type. All the oscillators for which algorithms are supplied in this book fall into this category. Because of the simplicity of the circuitry, this type of limiting is also the most difficult to analyze and some phases have not as yet been completely and satisfactorily quantitatively explained.

In general, oscillators using this type of limiting do not have as good short-term performance as oscillators with other limiter types, but surprisingly good performance is obtainable, even with crystals operating at very low drive power.

2 External limiter—which means that limiting is performed by auxiliary devices or circuits such as diodes, symmetrical clippers, and transistors. In two-transistor oscillators, one transistor is used specifically for limiting purposes. The external limiter is discussed in Chapter 13, except that diode limiting is treated in Section 6.5.

3 Automatic Level Control Limiting (ALC)—in which the rectified output voltage is compared to a dc reference voltage. The difference voltage is then

used to adjust the amplifier gain to the value demanded by the oscillator circuit. This type of limiting produces the best short- and long-term performance. It is discussed in Chapter 14.

6.2 THE SELF-LIMITING SINGLE BIPOLAR TRANSISTOR OSCILLATOR, SINUSOIDAL v_{BE} OR $v_{BE'}$

6.2.1 Types of Limiting Actions

There are two distinct types of limiting actions in this oscillator.

1 Base emitter cutoff, or current limiting in which the fundamental Fourier component of the collector current is reduced by swinging the base emitter voltage below the contact potential. The minimum instantaneous collector voltage then exceeds the peak base voltage at equilibrium. The latter condition exists where

$$V_{CE} > 1.4(V_{ce} + V_{be}) + 700 \text{ mV}$$

2 Collector voltage limiting in which the fundamental component of the collector current is reduced by the potential of the collector swinging close to the base potential, thus drastically reducing the collector emitter resistance r_{ce}. This type of limiting is sometimes called collector voltage bottoming.

It should be noted that the material in this section is applicable to both the common emitter and common base transistor applications.

6.2.2 Advantages and Disadvantages of Each Type of Limiting

1 In a large production run of the same design, if the resonators, Z_3, have approximately the same resistance, R_3, the *be* cutoff limiter is definitely superior. However, it is difficult to economically maintain the resistance of supposedly identical quartz crystals equal. In fact, military specifications only specify the maximum resistance for a given crystal type and therefore the acceptable resistance is permitted to cover a wide range. This results in a wide range of crystal drive and power output in the same oscillator when the *be* cutoff limiter is used, and each unit will have to be individually adjusted if constant power output or crystal drive is desired. On the other hand, when the base collector limiter is used, the same crystals will produce essentially constant power output although the crystal drive will vary as the crystal resistance varies.

2 The *be* cutoff limiter has the advantage that its frequency versus power supply voltage characteristic is better than when the collector voltage limiter is used. The effect is explained in Section 7.3.2.

This advantage may not be very important now since closely regulated, economical power supplies are very readily available.

3 The *be* cutoff limiter has the further advantage that often it produces smaller operating Q degradation than the collector voltage limiter.

4 On the other hand, the oscillator circuit using collector voltage limiting requires less labor to design and analyze, as will be evident in later chapters during the presentation of the design and analysis procedures.

5 The *be* limiter will permit higher-frequency operation of the oscillator since V_{CE} is higher and therefore f_T is larger.

6 When the crystal drive in crystal oscillators is very small, the base emitter limiter (or the auxiliary diode limiter described in Section 6.5) must be used for the reasons given in Section 6.5.

6.2.3 The Base Emitter Cutoff Limiter

The theory of operation of this type of limiter has already been presented in Section 2.4. However, it is interesting and instructive to demonstrate the limiting action. This is done, using the circuit of Fig. 6.1, as follows:

1 r_{b_2}, r_{b_1}, and r_2 are selected in accordance with the procedure described in Section 2.5.

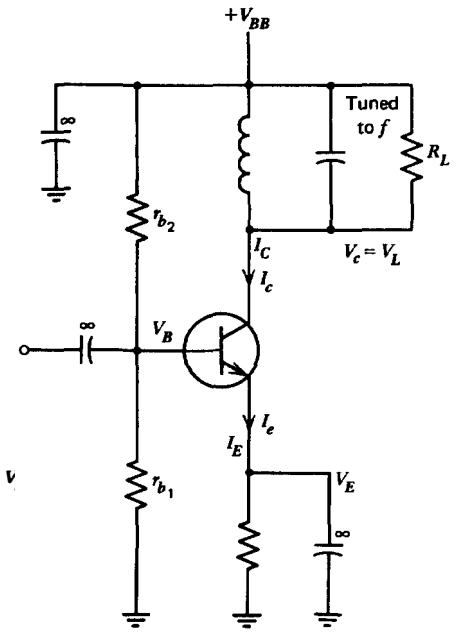


Figure 6.1 Circuit for analyzing the base emitter cutoff limiter.

2 V_{BB} and R_L are selected so that $V_{BB} - 1.4V_{c_{max}} > V_B + 1.4V_{b_{max}}$ to make certain that only base emitter cutoff limiting will take place.

3 V_b is varied, and for each value of V_b, V_c is recorded.

4 Then

$$I_c = \frac{V_c}{R_L} \tag{6.1}$$

$$g_m = \frac{I_c}{V_b} = \frac{\gamma_1 I_C}{V_b} \tag{6.2}$$

$$\alpha = \frac{g_m}{g_{m_0}} \tag{6.3}$$

where g_{m_0} is the value of g_m for small V_b (small-signal condition). γ_1 in Eq. (6.2) and α in Eq. (6.3) versus V_b are already plotted in Fig. 2.12.

6.2.4 The Collector Base Voltage Limiter

If the precautions specified in Section 6.2.3, item 2, are not taken and R_L is made too large, or V_{BB} too small, v_C approaches v_B and the limiting condition exists when $v_B \approx v_C$ because transistor action cannot exist when $v_B > v_C$.

The theory of collector base voltage limiting has not been extensively developed and very little information on a quantitative basis is available in the literature. This section will therefore develop a theoretical procedure which offers some quantitative treatment and is in reasonably good agreement with experiment.

Figure 6.2*a* shows the schematic of a circuit suitable for analyzing the base collector voltage limiter. Figure 6.2*b* shows the voltage relations that exist when limiting starts. Figure 6.2*c* shows the voltage relations that exist when the input signal V_b exceeds the limiting starting point. Note the broadening of the v_C curve at the bottom, leading to the name *bottoming effect*. The departure of the v_C wave shape from a sine wave is, of course, a function of the R_L circuit effective Q.

In both Figs. 6.2*b* and 6.2*c* the dc voltage difference between base and emitter is shown as approximately 700 mV although it varies with signal level due to bias shifts, but the voltage change has little effect on the total performance because of the biasing circuitry used. From Fig. 6.2 one obtains

$$V_{BB} - 1.4V_L = V_B + 1.4V_B - 700$$

and

$$V_B = V_E + 700$$

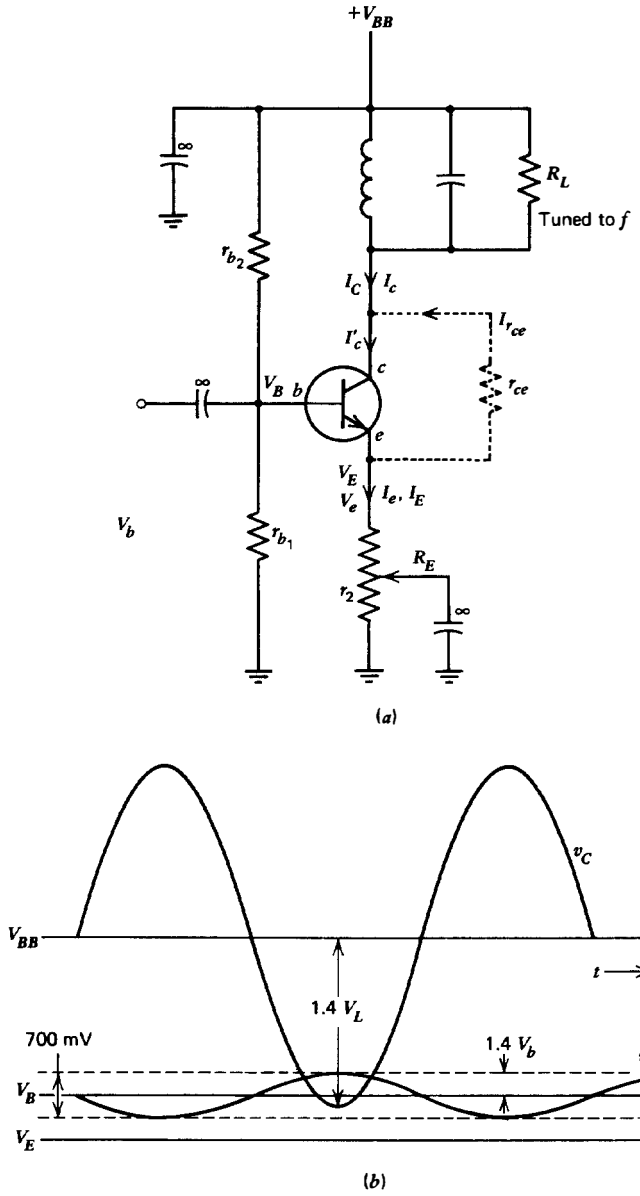
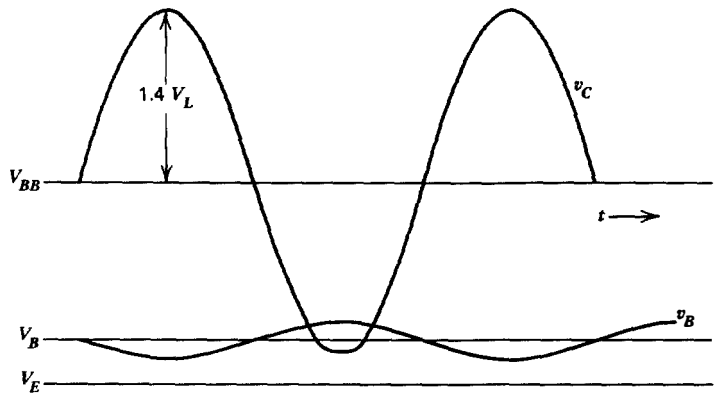


Figure 6.2 Circuit for analyzing the collector base voltage limiter. (*a*) Schematic. *Notes*: $I_C \approx I_E$. $I_o \approx I_e$. (*b*) Wave shapes at the limiting starting point. (*c*) Wave shapes past the limiting starting point.



(c)

Figure 6.2 (Continued).

from which

$$V_E = V_{BB} - 1.4(V_L + V_b) \tag{6.4}$$

Figure 6.2*a* shows the transistor output resistance r_{ce}, drawn in dashed lines, which normally approaches ∞ before limiting takes place, but becomes progressively smaller as the input signal is increased. It will be seen that as the signal starts from 0 and increases, all the I_c' current goes to the load circuit. Past the limiting point, part of the total current I_c' goes to the load circuit as I_c and the remainder goes into r_{ce} as $I_{r_{ce}}$. The division of the total current changes as a function of the input signal V_b and the dc current I_E.

Also, past the limiting point, I_c' and $I_{r_{ce}}$ increase and I_c remains essentially constant.

By definition,

$$g_m = \frac{I_c}{V_b} \tag{6.5}$$

$$g_{m_L} = \frac{I_c'}{V_b} \tag{6.6}$$

and

$$A_L = \frac{g_{m_L}}{g_m} = \frac{I_c'}{I_c} \tag{6.7}$$

From Eqs. (2.65) ai

$$g_{m_{L_0}} = \frac{1}{26/I_E + R_E} \qquad \text{at } T = 300°\text{K} \tag{6.8}$$

assuming β is reasonably large and $r'_e = r_{bb'} = 0$. From Figs. 2.12*b* and 2.13*c*, past the limiting point,

$$\gamma_1 = \frac{I'_{c_{max}}}{I_{\_}} = 1.4 \tag{6.9}$$

6.2.4.1 Limiting when $R_E = 0$

Assume that, for maximum efficiency, $I'_c = I'_{c_{max}}$ and $r_{bb'} = 0$, $r'_e = 0$, and $R_E = 0$. Then

$$V_b = V_{be} \tag{6.10}$$

and from Eq. (6.8)

$$g_{m_{L_0}} = \frac{I_C}{26} \tag{6.11}$$

From Eqs. (2.70), (6.6), (6.10),

$$\alpha V_b \frac{I_C}{26} = I'_c \tag{6.12}$$

and from Eq. (2.79) for $V_{be} \gtrsim$

$$\frac{I_C}{26}$$

or

$$I_C \approx 0.7 I'_c \tag{6.13}$$

which is consistent with Eq. (6. (6.7)

$$I_C = 0.7 A_L I_c \tag{6.14}$$

$V_b \equiv V_{be}$ will now be computed) and (6.6).

$$V_b = \frac{I'_c}{g_{m_L}} = \frac{I_c}{g_m} \tag{6.15}$$

$$= \frac{I'_c}{\alpha g_{m_{L_0}}}$$

$$\approx \frac{36}{\alpha} \text{ mV} \tag{6.16}$$

from Eqs. (6.11) and (6.13) where $\alpha < 0.3$ to make certain that Eq. (6.14) is valid.

Consider the following example:

$V_{BB} = 10$ V
$R_L = 570\ \Omega$
$V_L = 2$ V
$R_E = 0,\ r'_e = 0$
$A_L = 2$

Then

$$I_c = \tfrac{2}{570} = 3.5 \text{ mA}$$

$$I'_c = 2(3.5) = 7.0 \text{ mA}$$

$$I_C = 0.7(7) = 4.9 \text{ mA}$$

$$I_{r_{ce}} = 3.5 \text{ mA}$$

$$V_b \approx \frac{0.36}{\alpha}$$

For $\alpha = 0.3$, $V_b \approx 120$ mV

$$g_{m_L} \approx \tfrac{7}{120} \approx 0.058$$

$$g_m \approx 0.029$$

For $\alpha = 0.1$, $V_b \approx 360$ mV

$$g_{m_L} \approx 0.0194, \qquad g_m \approx 0.0097$$

6.2.4.2 *Limiting When $R_E \gg r_{e_0}$*

It is desirable to stabilize the characteristics of the transistor. This is possible by making R_E a value large compared to r_{e_0}. This is done at the expense of decreasing $I_{r_{ce}}$, as shown in the following example:

$$V_{BB} = 10 \text{ V}$$

$$R_L = 570\ \Omega$$

$$V_L = 2 \text{ V}$$

$$R_E = 5r_{e_0}, \qquad r'_e = 1\ \Omega$$

$$A_L = ?$$

then $I_c = 2/570 = 3.5$ mA.

I_C will be kept at 4.9 mA = $1.4I_c$ since a computer analysis showed that very little is gained by increasing I_C.

$$r_{e_0} = \frac{26}{4.9} + 1 = 6.3\ \Omega$$

$$R_E = 5(6.3) = 31.5\ \Omega$$

$$g_{m_{L_0}} = \frac{1}{6(6.3)} = 0.026\ \mho$$

Assume

$$g_m = \frac{g_{m_{L_0}}}{2} = 0.013\ \mho$$

then

$$V_b = \frac{3.5}{0.013} = 269\ \text{mV}$$

From Fig. 2.13*c*, $\gamma_1 = 1.2$ for $\rho = 5$ so that $I_c' = 1.2(4.9) = 5.88$ mA $= 1.7I_c$ and $I_{r_{ce}} = 2.38$ mA $= 0.7I_c$.

This design is still considered satisfactory because there is a substantial $I_{r_{ce}}$, although not as much as described in Section 6.4.1. In the algorithms for oscillators using this type of limiting, this design will be used. It should be further noted that the design is based on crystals having the maximum resistance. When the resistance decreases, I_c decreases, I_c' remains constant, and $I_{r_{ce}}$ increases, which implies that this design is safe.

To formalize the design, the following equations are developed:

$$I_C = 0.7A_{L_0}I_c \tag{6.17}$$

$$A_{L_0} = \frac{g_{m_{L_0}}}{g_m} \tag{6.18}$$

$$g_{m_{L_0}} = \frac{1}{r_{e_0} + R_E} \tag{6.19}$$

$$= \frac{1}{R_E + 26/I_E + 1} \tag{6.19a}$$

for the special case where

$$R_E = 5r_{e_0} = 5\left(\frac{26}{I_E} + 1\right) \tag{6.20}$$

$$g_{m_{L_0}} = \frac{1}{R_E\left(1 + \frac{1}{5}\right)} = \frac{0.83}{R_E} \tag{6.20a}$$

$$= \frac{1}{6(26/I_E + 1)} \tag{6.20b}$$

$$R_{\text{in}} = \frac{X_1^2}{r_{be}}, \qquad = g_m \frac{X_1^2}{\beta_o} \tag{6.21}$$

$$C_{bed} = g_m \frac{159{,}000}{f_T} \tag{6.22}$$

6.2.4.3 The Uses of the Design Procedures of Sections 6.2.4.1 and 6.2.4.2

This section will discuss when each of the above design procedures should be used.

The method in Section 6.2.4.2 is generally preferred because it minimizes transistor variations and it reduces phase noise. However, it requires a specific V_b which at high frequencies may not be realizable for a given crystal current. It will be noted from the example that V_b in the example of Section 6.2.4.1 is 120 mV while the equivalent V_b in the example of Section 6.2.4.2 is 259 mV. Also, for a given crystal drive the procedure of Section 6.2.4.1 permits a wide range of V_b for the same A_{L_0}, while the V_b for the procedure of Section 6.2.4.2 is fixed.

6.3 THE SELF-LIMITING SINGLE BIPOLAR TRANSISTOR OSCILLATOR, SINUSOIDAL i_E

6.3.1 Types of Limiting Actions

Again in this oscillator there are two distinct types of limiting actions:

1. R_{IN} variation as a function of I_e, as described in Section 2.5.2.2.
2. Collector voltage limiting which is identical to that described in Section 6.2.

6.3.2 Advantages of Each Type of Limiting

Section 6.2.2 applies except that when *be* cutoff limiting is mentioned; read R_{IN} variation limiting.

6.3.3 The R_{IN} Limiter

The theory of this type of limiter is presented in Section 2.5.2.2. The following additional material is presented to adapt this theory to oscillator design.

1 To ensure that this type of limiting is operative, $v_{C_{min}}$ must always exceed $v_{B_{max}}$.
2 For the most effective limiting, it is advisable that Eq. (2.97) be modified to

$$I_E \approx 1.4 I_e \tag{6.23}$$

so that

$$\gamma \approx 1 \tag{6.24}$$

It will be seen from the extrapolated dotted portion of Fig. 2.15 that, at this operating point, R_{IN} can assume any value larger than $2/g_{m_0}$ as demanded by the circuit equilibrium conditions. (See Chapter 11 for the effect on the operating Q.)
3 The requirements of items 1 and 2 fix the other operating points and the associated component values.

6.3.4 The Collector Base Voltage Limiter

Essentially, all the material presented in Section 6.2.4 is applicable.

6.4 THE SELF-LIMITING SINGLE JUNCTION FIELD EFFECT TRANSISTOR OSCILLATOR, SINUSOIDAL v_{GS}

Again, in this oscillator, there are two distinct types of limiting.

1 Clamped bias limiting, described in Section 2.6.4. This type of limiting is analogous to the base emitter cutoff limiting for the bipolar transistor and uses the same design procedure.
2 Drain gate voltage limiting, which is almost identical to the collector base voltage limiting for the bipolar transistor described in Section 6.2.4.

6.5 DIODE LIMITER (SEE ALSO SECTION 13.5.2)

Diode limiting is really a special form of collector limiting.

Equation (6.4) and Figs. 6.2*b* and 6.2*c* show that when V_L is small, setting the various bias points to the necessary precision becomes very difficult as V_{CB}, which is now required to be very small, is the difference of two large quantities,

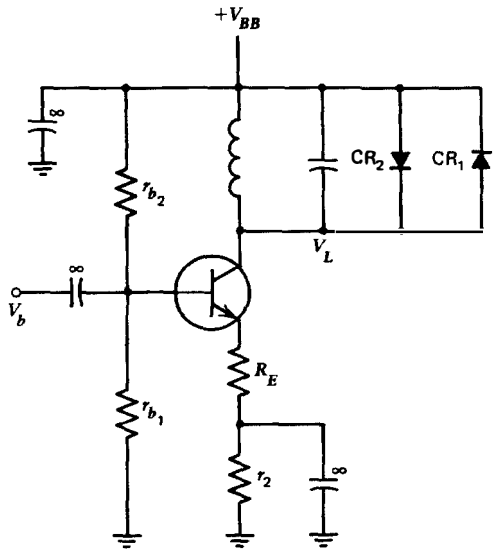


Figure 6.3 Diode limiting circuit.

V_C and V_B. This is further complicated by the bias differences that exist between the nonoscillating and the oscillating states, and the bias shifts that are caused by temperature variations.

One method of resolving these difficulties is to use auxiliary diodes as shown in Fig. 6.3. In this circuit V_L is limited by the nonlinear characteristics of CR_1 and CR_2 which tend to maintain V_L constant over a wide range of the current in the diodes. A good approximation is that V_L will be 0.5 V for silicon diodes.

Sometimes CR_2 is omitted with approximately the same results. However, the output waveform is more symmetrical when both diodes are present and the frequency voltage sensitivity is smaller.

This circuit does not completely keep V_L constant. This is due to the fact that the diodes do not maintain a strictly constant voltage as the current varies and, in addition, the diode voltage varies with temperature. The temperature variation can be compensated by a thermistor-controlled circuit, but additional complications in design and reliability are introduced.

6.6 PRINCIPAL REFERENCE

Reference 2.3 contains extensive material on nonlinear processes suitable for limiting, including complete exposition of the large-signal transistor characteristics treated in Chapter 2.