10
Temperature Compensation

The frequency stability of an AT-cut quartz crystal resonator as a function of temperature is determined primarily by the angle at which the resonator plate is cut from the mother quartz crystal. Curves showing this dependence are presented in Figure 5-6. These curves follow a cubic equation of the form

$$f = A_1(t - t_0) + A_2(t - t_0)^2 + A_3(t - t_0)^3, \qquad (10\text{-}1)$$

where f is the frequency difference between t_0, usually taken to be 20 or 25°C and the temperature t. (The values for the coefficients are given in section 10.4.) Improved frequency stability can be obtained by operating the units in a controlled-temperature environment such as a crystal oven; however, the disadvantages of such operation have become apparent in recent years, as discussed in sections 4.1.1 and 9.3. It is therefore desirable to develop other means for improving the frequency stability of quartz crystal resonators which are more nearly compatible with present-day requirements.

It has been known for many years that the resonant frequency of a crystal unit can be made to shift by placing a reactance in series with it. If this reactance is made to vary in such a manner that it counteracts the frequency shift of the resonator with temperature, a greatly improved temperature coefficient can be obtained. The advent of the varactor diode and the thermistor in the late 1950s first made this practical. A method of analog temperature compensation was developed in which a multiple thermistor–resistor network was used to generate the required voltage–temperature curve.[23]

At the time of this writing nearly all production temperature-compensated crystal oscillators (TCXOs) use this method, which we shall refer to as analog compensation. Generally, the frequency stability using this method can be made as good as 0.5 ppm from -55°C to +85°C in production by tailoring some elements in the thermistor network to the individual crystal being used. With great care, small numbers of units have been compensated to better than 0.1 ppm, but the procedure is rather tedious.

It is not surprising that, with the development of field programmable read-only memories (PROMs), digital compensation should be possible. Historically, because only small PROMs were available initially, the coarse compensation was done using analog networks, and the final corrections were made digitally. The general approach was to sense the temperature and use its value in digital form to address a memory. The contents of the particular memory location then contained the fine correction voltage required at that temperature. The digital correction voltage was converted to an analog signal and applied to a fine-compensation varactor in the oscillator. This technique is referred to as *hybrid analog-digital compensation* and makes frequency stabilities in the 0.1-ppm range practical in production. If a large memory is used so that the coarse analog compensation can be eliminated, we refer to the technique simply as *digital compensation*. Temperature compensation can also be accomplished by using microprocessing techniques in which the processor compensates its own clock oscillator or an external precision crystal oscillator.

These techniques are discussed in detail in the remainder of the chapter and, in some cases, experimental results are presented showing what can be achieved in practice.

10.1. ANALOG TEMPERATURE COMPENSATION*

As indicated earlier, most TCXOs in production at the time of this writing use analog techniques and, although many new designs will be digital, it is nevertheless of interest to discuss the technique. In general the procedure is to place a varactor in the oscillator circuit where it can pull the frequency at least as far as the crystal drifts in temperature. A voltage divider network composed of thermistors and resistors is then designed which will produce the required voltage-temperature function to compensate the oscillator.

*Several of the results presented in this section were developed under sponsorship of the US Army Electronics Command and are discussed in more detail in reference 1.

Normally, though not always, the varactor is placed in series with the crystal and has a capacitance-voltage function given by the equation

$$C = \frac{K}{(V + V_0)^n}, \tag{10-2}$$

where K, V_0, and n are constants (actually these quantities are somewhat temperature-dependent, but for a first approximation may be treated as constants). V_0 is the contact potential and is in the order of 0.75 V; n is primarily determined by the slope factor of the p–n junction and may be on the order of 0.3–2. For analog TCXOs, an n around 0.5 is often used and represents an abrupt p–n junction.

Solving equation (10-2) for V gives:

$$V = \left(\frac{K}{C}\right)^{1/n} - V_0. \tag{10-3}$$

The crystal load capacitance required to pull an amount $\Delta f/f_s$ in parts per million is given in equation (5-2) and may be arranged in the form

$$C_L = \frac{C_1}{2(\Delta f/f_s)} - C_0. \tag{10-4}$$

Substituting $\Delta f = f - f_s$ gives

$$C_L = \frac{C_1}{2\left(\frac{f - f_s}{f_s}\right)} - C_0. \tag{10-5}$$

Normally the crystal is cut slightly low in frequency so that when C_L = 32 pF the crystal is on frequency at 25°C. Thus we have $f = f_L$ at the load capacitance C_L. Now, defining Δf_L as $f - f_L$, the change in frequency from nominal, the load capacitance required by the crystal at Δf_L is given by

$$C_{x1} = \frac{C_1}{2\left[\frac{\Delta f_L}{f_s} + \frac{C_1}{2(C_0 + C_L)}\right]} - C_0. \tag{10-6}$$

The function C_{x1} can then be determined by substituting values of $\Delta f_L/f_s$ from the crystal curve such as shown in Figure 5-6. In practice only the limit values of C_{x1} are normally calculated at lowest and highest crystal frequencies. Then knowing the values of the oscillator capacitors, C_1 and C_2 (see Figure 10-11, for example), the varactor capacitance C can be calculated by recognizing that C_1, C_2, and the varactor are effectively in series. Thus

$$C = \frac{1}{\dfrac{1}{C_{x1}} - \dfrac{1}{C_1} - \dfrac{1}{C_2}}. \tag{10-7}$$

Finally then, using equation (10-3), the required voltage extremes can be found.

A large variety of thermistor–resistor networks have been successfully used to generate the required voltage function for TCXOs. One such network which works well is shown in Figure 10-1. It can be shown that the transfer function for this network is given by:

$$\frac{V_o}{V_i} = \frac{RT_3(R_1 + RT_1)(R_2 + RT_2)}{(R_1 + RT_1)(R_2 + RT_2)(R_3 + RT_3) + R_2RT_2\,[(R_1 + RT_1) + (R_3 + RT_3)]} \tag{10-8}$$

$$RT_1(T) = RT_1(T_0) \exp \beta_1 \left(\frac{1}{T} - \frac{1}{T_0}\right) \tag{10-9}$$

$$RT_2(T) = RT_2(T_0) \exp \beta_2 \left(\frac{1}{T} - \frac{1}{T_0}\right) \tag{10-10}$$

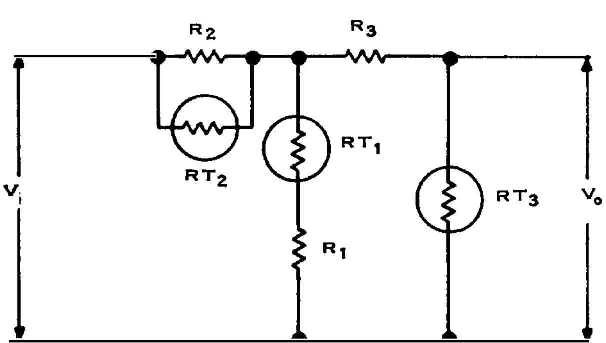

Figure 10-1. Three-stage thermistor network: schematic diagram.

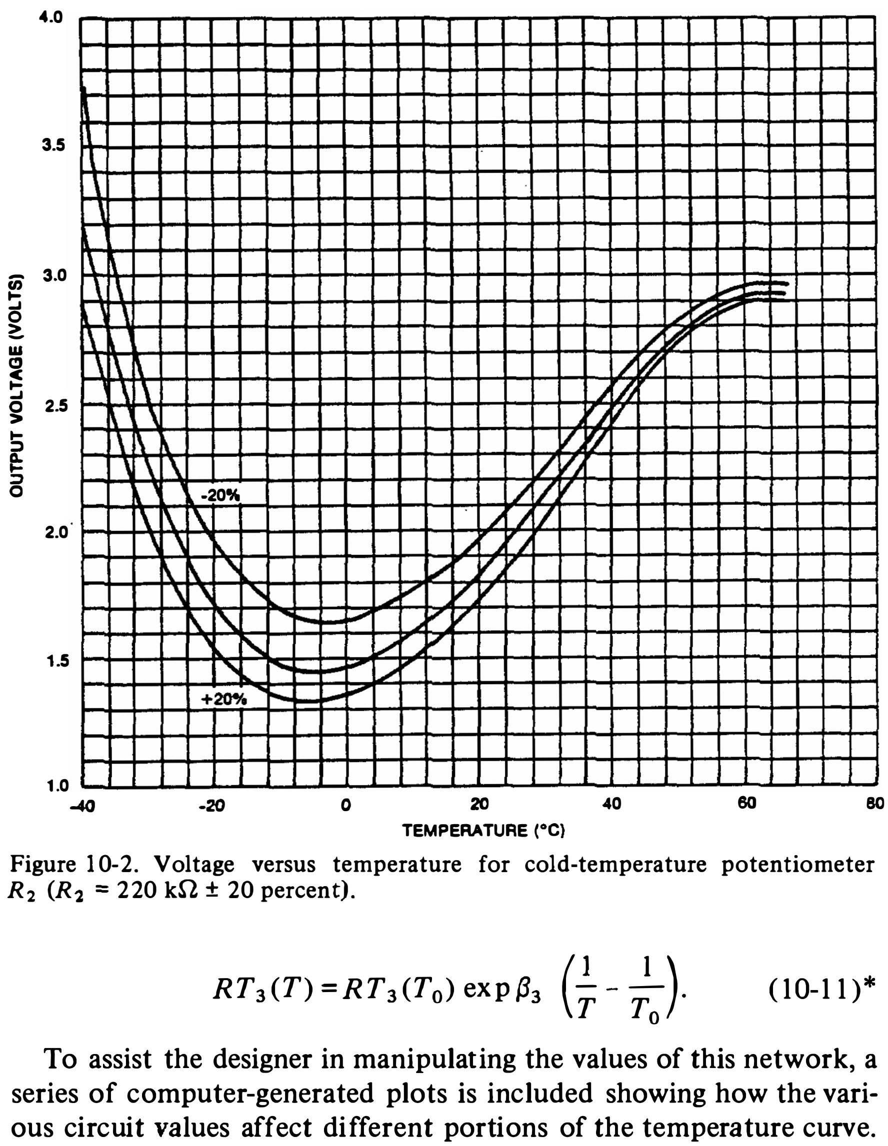

Figure 10-2. Voltage versus temperature for cold-temperature potentiometer R_2 (R_2 = 220 kΩ ± 20 percent).

$$RT_3(T) = RT_3(T_0)\ \exp \beta_3 \left(\frac{1}{T} - \frac{1}{T_0}\right). \qquad (10\text{-}11)^*$$

To assist the designer in manipulating the values of this network, a series of computer-generated plots is included showing how the various circuit values affect different portions of the temperature curve. These graphs are shown in Figures 10-2 through 10-10.

*Here β is referred to as the beta of the thermistor and is a measure of how fast the resistance decreases with increasing temperature. This temperature coefficient is determined by the composition of the thermistor during manufacture. T and T_0 are absolute temperatures in °K.

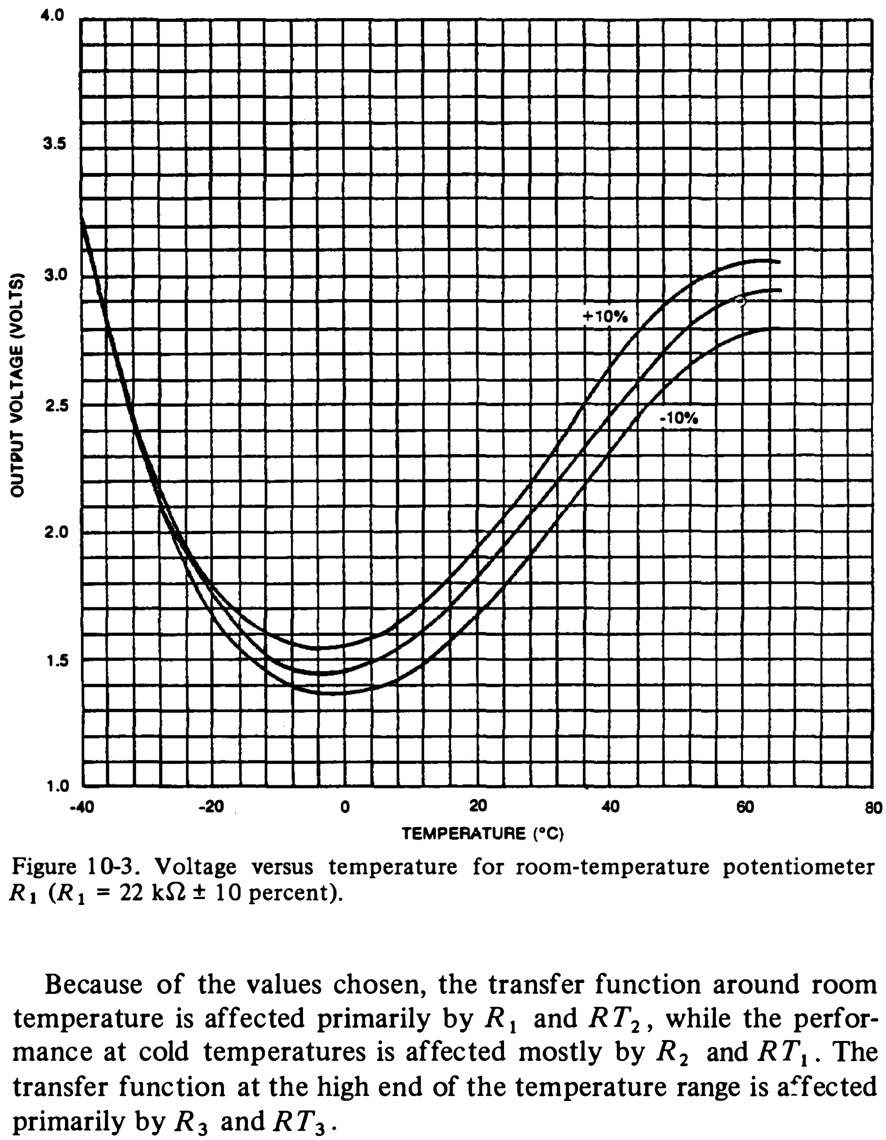

Figure 10-3. Voltage versus temperature for room-temperature potentiometer R_1 (R_1 = 22 kΩ ± 10 percent).

Because of the values chosen, the transfer function around room temperature is affected primarily by R_1 and RT_2, while the performance at cold temperatures is affected mostly by R_2 and RT_1. The transfer function at the high end of the temperature range is affected primarily by R_3 and RT_3.

A typical TCXO circuit diagram is given in Figure 10-11.

Because of the competitive nature of TCXO production, the actual procedures used by manufacturers to adjust the values of the thermistor network generally have not been available and the procedures in some cases involve as much art as science.

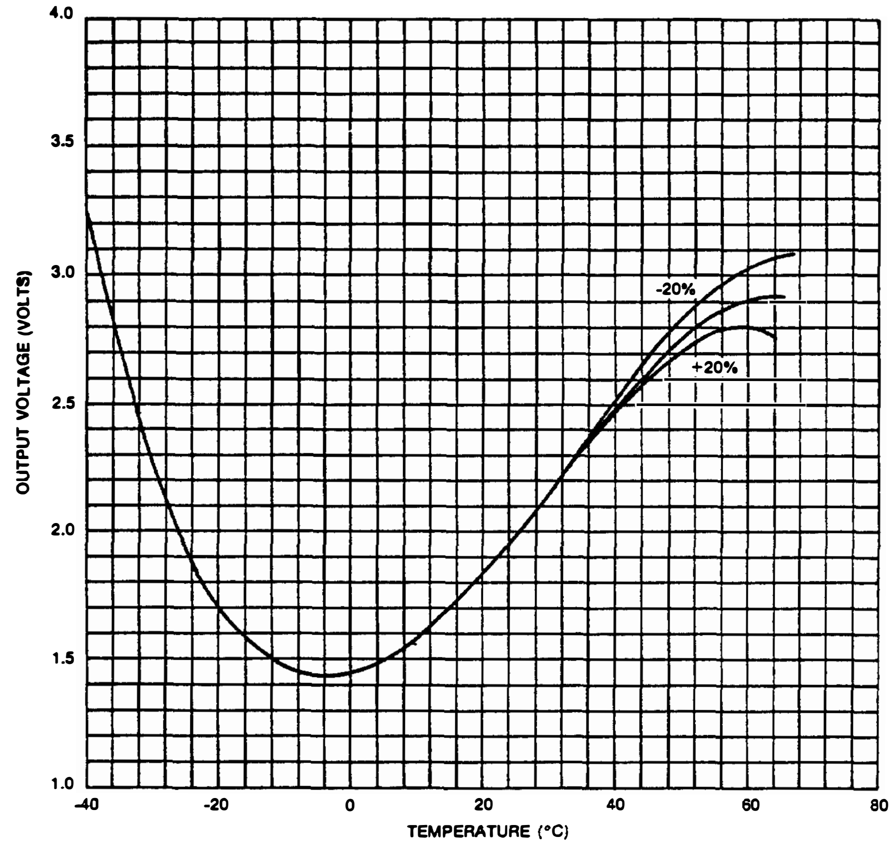

Figure 10-4. Voltage versus temperature for high-temperature potentiometer R_3 (R_3 = 33 kΩ ± 20 percent).

One approach which has been found to work well for the network of Figure 10-1 and an oscillator as shown in Figure 10-11 is described below.

The crystal is chosen to have an angle of cut so that the total frequency excursion between turning points is in the 35-ppm range. If an abrupt-junction varactor is used with an exponent of 0.5, its value is chosen to pull the crystal about 45 ppm from 1 V to two-thirds of the supply voltage. (A nominal value in the 20- to 50-pF range at 4 V dc should result.) A small selectable capacitor of perhaps 5 pF is

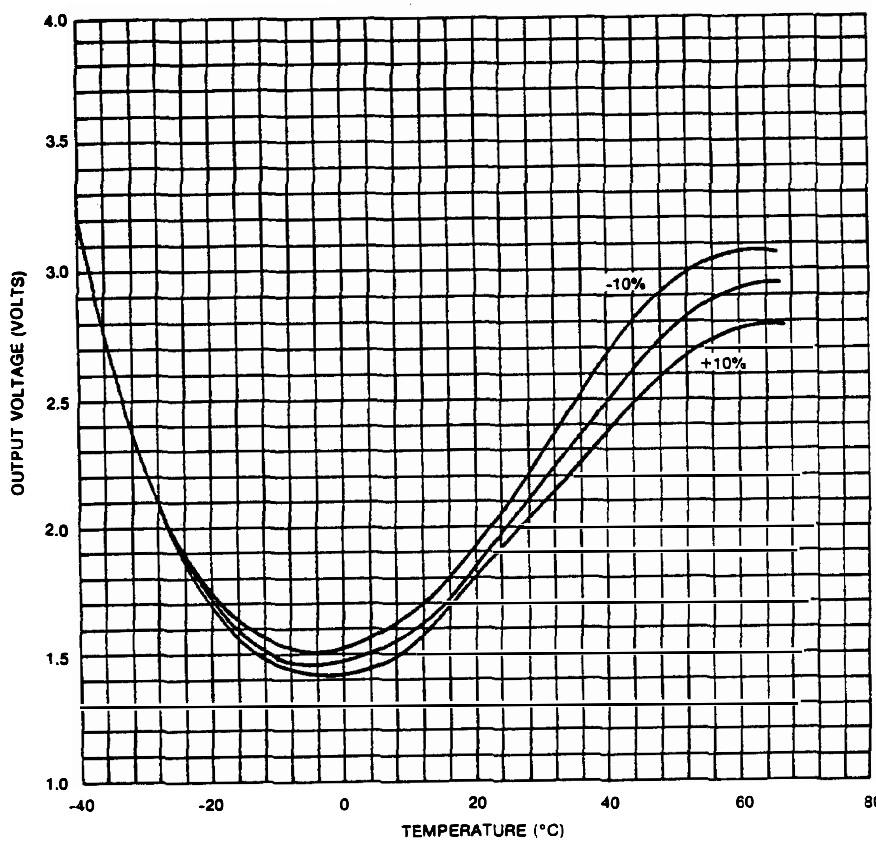

Figure 10.5. Voltage versus temperature for room-temperature thermistor RT_2 [$RT_2(T_0) = 100$ kΩ ± 10 percent, $\beta_2 = 3900$].

retained across the varactor to allow final adjustment of the pullability. It has been found appropriate to use crystals which have a $\Delta f/f$ of approximately 160 ppm between series resonance and 32 pF.

For 12 V dc at the input of the thermistor network, R_1 (the room-temperature adjustment) is set for about 2.25 V initially. The oscillator is then placed in a temperature chamber and cooled to the lowest temperature, perhaps -40°C to -55°C, and R_2 (the cold adjustment) is set to put the oscillator back on frequency. The temperature chamber is then set to a temperature around the lower turning point of

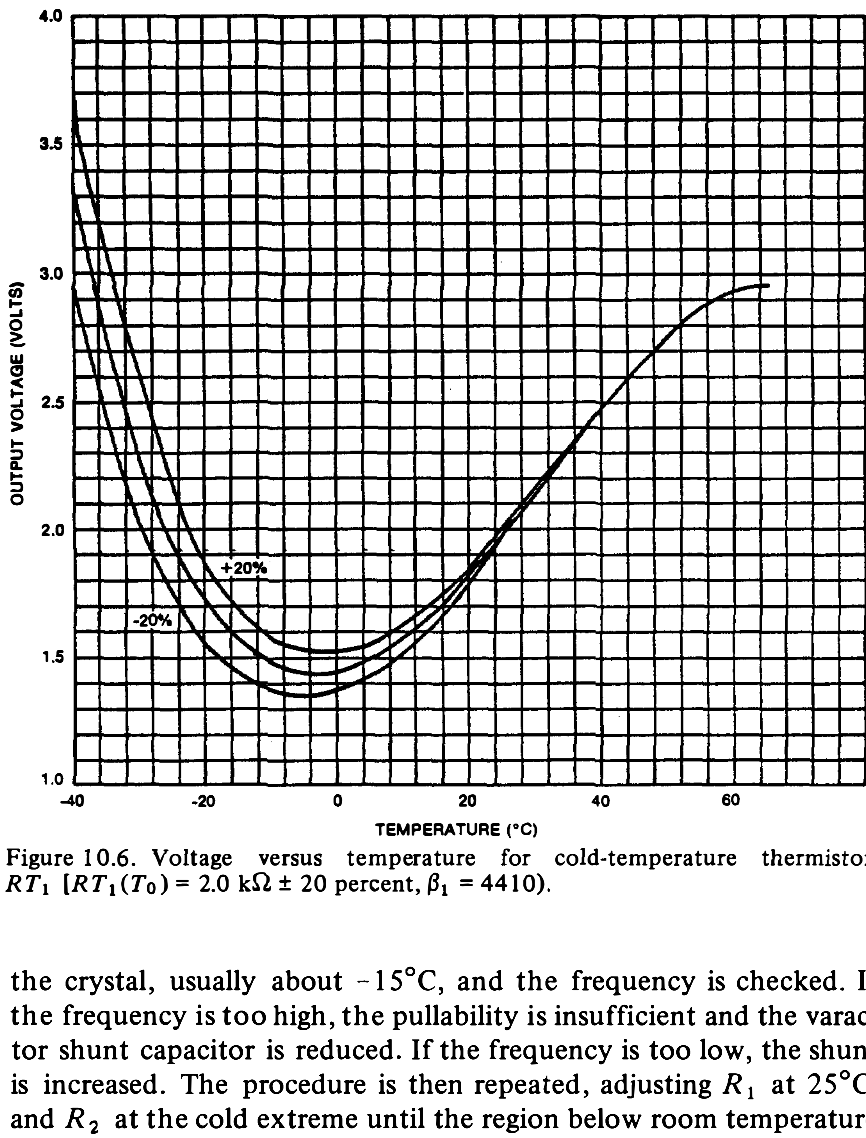

Figure 10.6. Voltage versus temperature for cold-temperature thermistor RT_1 [$RT_1(T_0)$ = 2.0 kΩ ± 20 percent, β_1 = 4410).

the crystal, usually about −15°C, and the frequency is checked. If the frequency is too high, the pullability is insufficient and the varactor shunt capacitor is reduced. If the frequency is too low, the shunt is increased. The procedure is then repeated, adjusting R_1 at 25°C, and R_2 at the cold extreme until the region below room temperature is compensated. The temperature is then increased to the upper extreme, usually 75–85°C, and R_3 (the hot adjustment) is set to put the oscillator on frequency. A confirming temperature run is then made. A typical completed TCXO curve is shown in Figure 4-1.

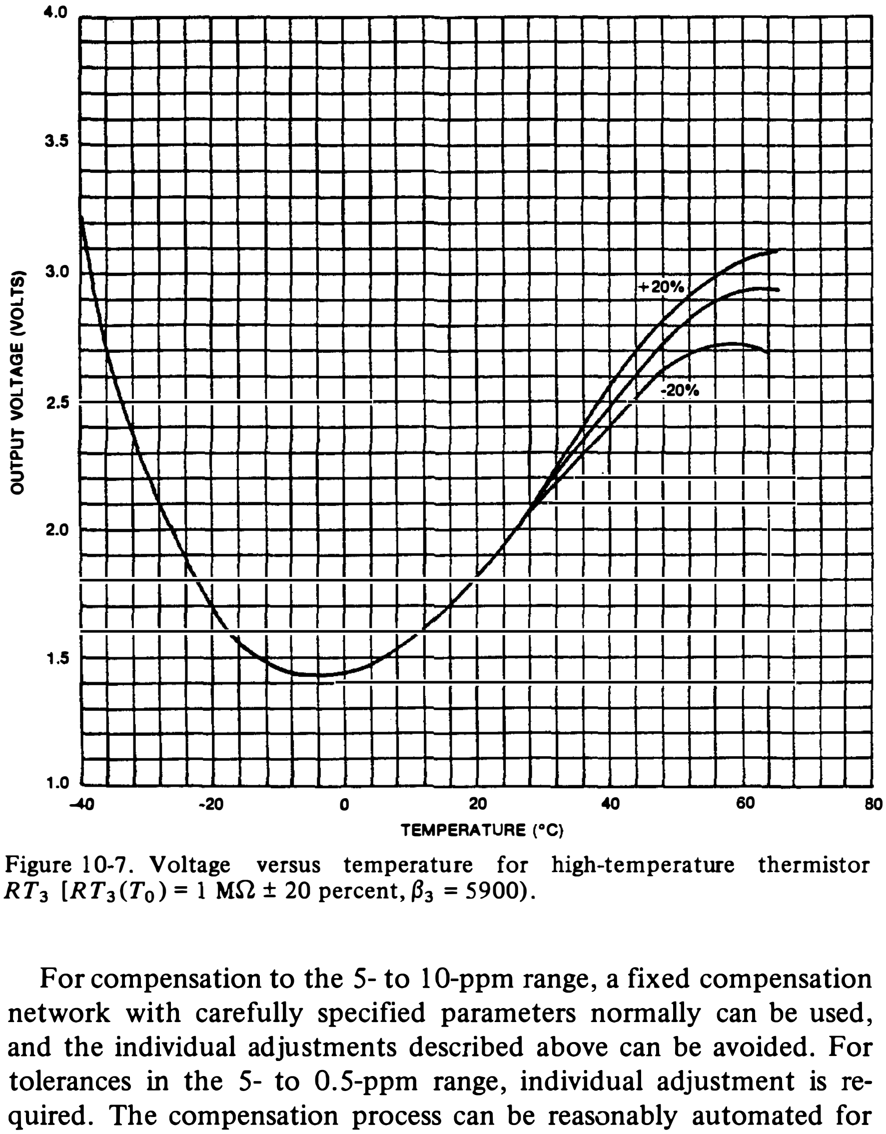

Figure 10-7. Voltage versus temperature for high-temperature thermistor RT_3 [$RT_3(T_0)$ = 1 MΩ ± 20 percent, β_3 = 5900).

For compensation to the 5- to 10-ppm range, a fixed compensation network with carefully specified parameters normally can be used, and the individual adjustments described above can be avoided. For tolerances in the 5- to 0.5-ppm range, individual adjustment is required. The compensation process can be reasonably automated for mass production.

Several other factors must be considered in the design of a TCXO, such as the voltage regulation at the input of the thermistor network and the load isolation at the buffer amplifier. Obviously, the voltage

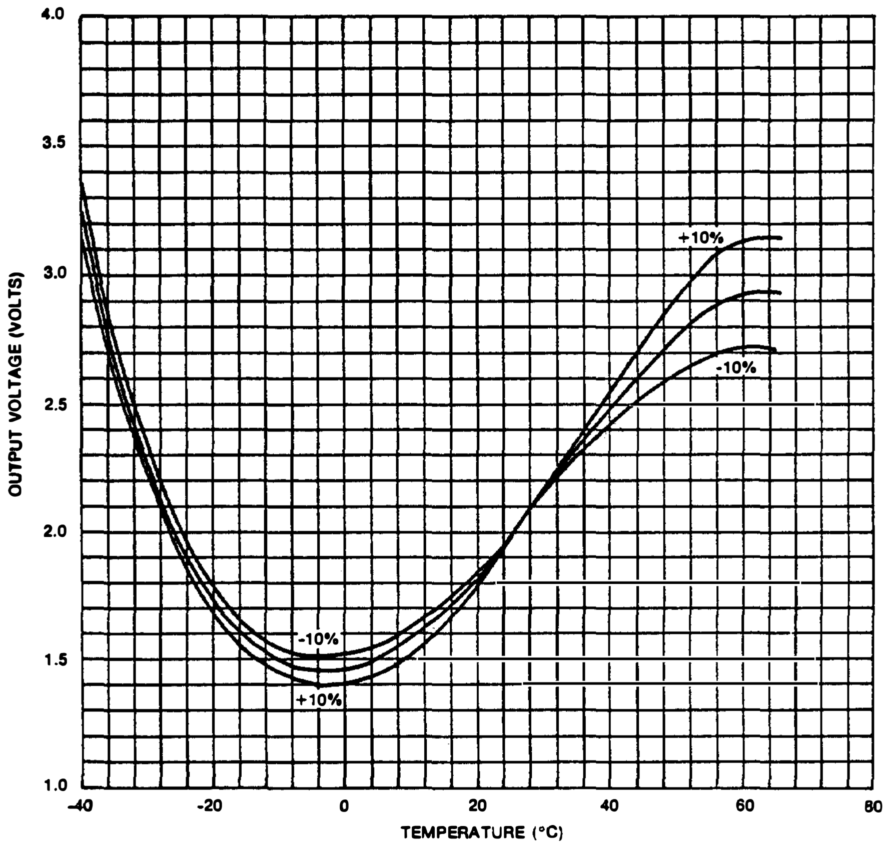

Figure 10-8. Voltage versus temperature for room-temperature thermistor RT_2 $[RT_2(T_0) = 100\ \text{k}\Omega, \beta_2 = 3900 \pm 10$ percent).

regulation must be sufficiently good so that changes in the supply voltage will not cause the varactor to pull the frequency by a significant amount compared to the frequency stability specification. In general, either a Zener diode regulator or a packaged integrated circuit regulator is used to supply current to both the oscillator and the thermistor network. It is normally of considerable importance to minimize the power dissipated in a TCXO because of self-heating and temperature gradients which may cause a frequency drift at turn-on. Therefore, a low-power voltage regulator is recommended to keep the input power below the 100-mW range.

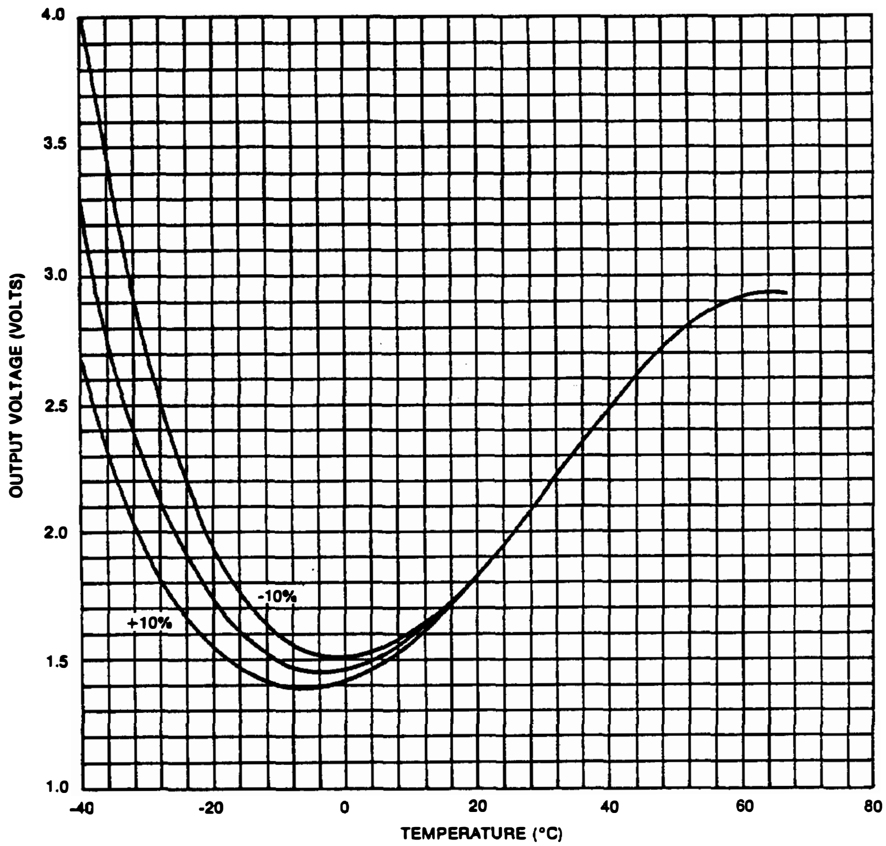

Figure 10-9. Voltage versus temperature for cold-temperature thermistor RT_1 $[RT_1(T_0) = 2\ \text{k}\Omega, \beta_1 = 4410 \pm 10$ percent).

As with changes in supply voltage, changes in the oscillator load can also perturb the frequency.

To analyze the effect, consider the phasor diagram of Figure 10-12, where E_s represents the signal voltage at some point in the oscillator loop and E_n represents an induced voltage from the output stage at the same point in the oscillator loop. Here the magnitude of E_n is exaggerated for purposes of illustration. The resultant voltage is shown as E_r. The phase shift in oscillator voltage caused by the presence of E_n is given by angle β. Angle α is the phase difference between E_s and E_n. By elementary geometry, we have $\overline{AB} = E_n$ and $\angle OAB = 180 - \alpha$.

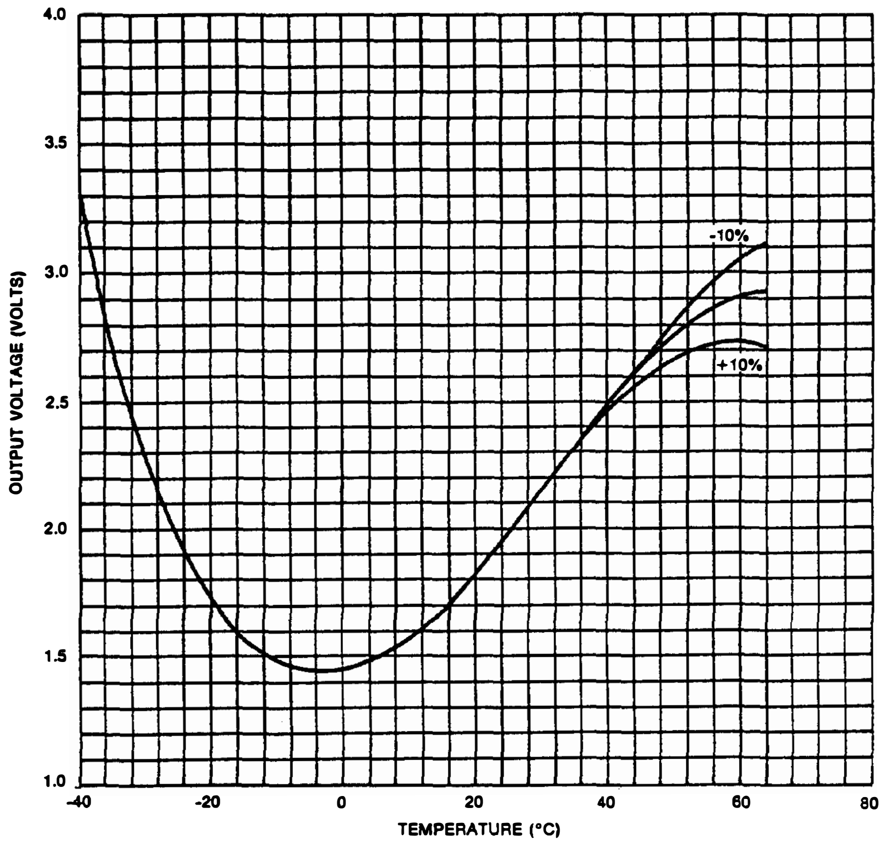

Figure 10-10. Voltage versus temperature for high-temperature thermistor RT_3 [$RT_3(T_0) = 1$ MΩ, $\beta_3 = 5900 \pm 10$ percent).

Then, by the law of sines, we have

$$\frac{\sin \beta}{\overline{AB}} = \frac{\sin (180 - \alpha)}{E_r}. \tag{10-12}$$

Rewriting and substituting E_n for $\overline{AB}$ gives

$$\sin \beta = \frac{E_n}{E_r} \sin (180 - \alpha) = \frac{E_n}{E_r} \sin \alpha. \tag{10-13}$$

If $E_n << E_s$ (as would be the case in an oscillator of practical in-

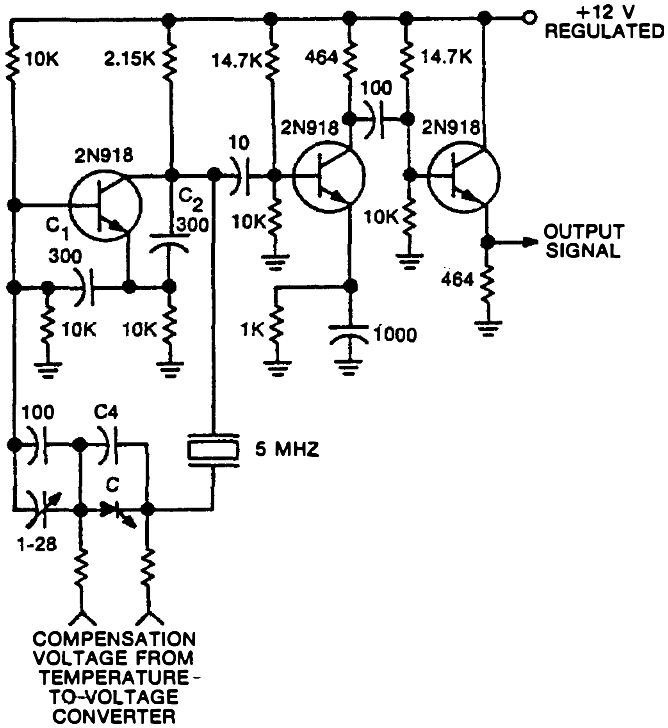

Figure 10-11. Temperature-compensated crystal oscillator and isolation amplifier.*

terest) we have $E_r \doteq E_s$ and $\sin \beta \doteq \beta$. Then

$$\beta \doteq \frac{E_n}{E_s} \sin \alpha. \tag{10-14}$$

It is now interesting to calculate the resulting frequency shift due to the presence of the induced voltage, E_n. To accomplish this, consider the circuit diagram of Figure 10-13. This is the circuit diagram of a crystal near series resonance. The current is given by

$$I = \frac{E}{R + j[\omega L - (1/\omega C)]}. \tag{10-15}$$

*See footnote p. 66.

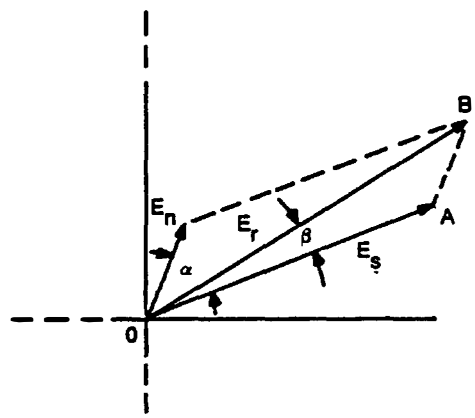

Figure 10.12. Oscillator voltage phasor diagram.

The phase angle of the current is given by

$$\theta = -\tan^{-1} \frac{\omega L - (1/\omega C)}{R}. \tag{10-16}$$

Differentiating with respect to ω, we have

$$d\theta = -\frac{1}{1 + \left[\frac{\omega L - (1/\omega C)}{R}\right]^2} \left\{ \left[\frac{L}{R} + \frac{1}{\omega^2 RC}\right] d\omega. \right\}$$

Multiplying numerator and denominator in the second term on the

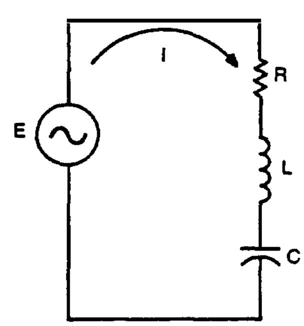

Figure 10.13. Series resonator circuit diagram.

right-hand side by $1/\omega$ gives

$$d\theta = -\frac{1}{1+\left[\dfrac{\omega L - (1/\omega C)}{R}\right]^2}\left[\frac{\omega L}{R} + \frac{1}{\omega RC}\right]\frac{d\omega}{\omega}. \qquad (10\text{-}17)$$

If the circuit is near series resonance, then

$$1 >> \left[\frac{\omega L - (1/\omega C)}{R}\right] \quad \text{and} \quad \frac{\omega L}{R} \doteq \frac{1}{\omega RC} = Q.$$

Then

$$d\theta = -2Q\frac{d\omega}{\omega} = -2Q\frac{df}{f}. \qquad (10\text{-}18)$$

For small changes, $\Delta\theta = d\theta$ and we may write

$$\Delta\theta = -2Q\frac{\Delta f}{f}. \qquad (10\text{-}19)$$

We now consider an example to obtain a feel for the required magnitude of isolation. Suppose we desire $\Delta f/f$ to be less than 5 parts in 10^8 for a particular oscillator. Assuming a loaded Q of 25,000, we have

$$\Delta\theta = -2 \times 25{,}000 \times 5 \times 10^{-8} = -2.5 \times 10^{-3} \text{ rad}.$$

Substituting in equation (10-14), we find

$$\frac{E_n}{E_s}\sin\alpha = -2.5 \times 10^{-3}.$$

If α, the phase angle between E_s and E_n, is on the order of 90 or 270 degrees, the ratio E_n/E_s must be approximately 2.5×10^{-3} or, in decibels, E_n must be 52 dB below the oscillator voltage. If the voltage gain of the amplifiers is on the order of 20 dB, the required isolation is 72 dB. This assumes the worst case where E_n and E_s are at 90 degrees. If the phase shift of the amplifier chain is designed so that it is near zero or 180 degrees, much larger values of E_n can be tolerated. If, however, the load is allowed to vary from pure inductance to pure capacitance, α will vary approximately from -45 to +45 degrees, and the improvement would be only a factor of 0.707.

Still another consideration in the design of a successful TCXO is the elimination of hysteresis. If the oscillator frequency does not repeat exactly from temperature run to temperature run, it is nearly impossible to achieve successful compensation. Hysteresis is generally caused by a component such as a capacitor or resistor which does not repeat with temperature or which jumps slightly in value. For this reason, film resistors and monolythic ceramic capacitors are often used in TCXOs. If it is noted that the frequency of a TCXO does not repeat, it is usually wise to search for the faulty component prior to any further attempts at compensation.

Apparent hysteresis can also result from insufficient stabilization time at each temperature. The wise engineer will make sure that the frequency has truly stabilized prior to moving on to the next temperature. In many TCXOs, stabilization times in the 15- to 30-minute range are not uncommon.

In the discussion so far we have assumed that a varactor is used to pull the crystal frequency. It is also possible to achieve compensation in the 5- to 10-ppm stability range by placing thermistors directly in parallel and in series with fixed capacitors in the oscillator circuit. Although this approach is perhaps somewhat less elegant than the varactor approach, it is nevertheless cost effective in some applications. A particular advantage is the fact that a voltage regulator and varactor are not required.

10.2. HYBRID ANALOG-DIGITAL COMPENSATION[7,57]

Analog temperature-compensated crystal oscillators, as described in section 10.1, with stabilities of ±5 parts in 10^7 from -40°C to +70°C, have been a commercial reality for about a decade. Such units have been produced by the thousands at reasonable cost. Stabilities of 1–2 parts in 10^7 have been achieved in small quantities over the -40°C to +70–80°C temperature range, and stabilities of 5 parts in 10^8 have also been achieved over narrower ranges in quite small quantities. In general, compensation becomes increasingly difficult beyond ±5 parts in 10^7 because of the very small component tolerances involved, of the interaction of network adjustments, and of an undefined degree of electrical hysteresis in crystals due to thermal cycling. Partial solutions to these limitations, although not entirely desirable from a production standpoint, have been the use of digital computers to solve network calculations and the use of analog segmented networks to provide greater independence of adjustments. Often a large number of temperature runs have been required to "massage" units into the 1-2 parts in 10^7 stability region. For the computerized approach, this is due to a lack of accurate component data and the inability to install the exact component values calculated. For the analog segmented approaches, the major difficulties remain the lack of true independence between segments and the accuracy with which components must be selected.

The temperature-compensation method described in this section effectively eliminates the component accuracy problem and the interaction of segments while allowing better visibility to evaluate and minimize electrical hysteresis. Using this approach, it has been possible to achieve temperature compensation to ±5 parts in 10^8 over the -40°C to +80°C temperature range under controlled test conditions.

A major portion of the effort to develop this approach was carried out by G. Buroker under the sponsorship of the Solid-State and Frequency Control Division of the United States Army Electronics Command.

A block diagram of the TCXO is shown in Figure 10-14. Compensation is achieved with both analog and digital techniques. The analog, or coarse, circuit is used in a conventional manner to reduce the oscillator temperature coefficient (TC) to ±4 parts in 10^7 or less; then the digital network adds fine corrections to reduce the overall TC to less than ±5 parts in 10^8. The TCXOs with analog compensation need only minor design refinements to be used with the hybrid approach. Primarily, these are improved voltage and load coefficients and a reduction in power dissipation.

For a typical unit, the RF circuit consists of an oscillator followed by an isolation amplifier. Stages may be stacked in pairs to save power. Power consumption by the oscillator stage and the first buffer may be less than 5 mW from the regulated source. The second buffer may require two or three times more power to meet the output requirement; however, in any event, the power consumption which results in internal heating should be minimized.

The coarse compensation network consists of the three thermistors and their associated resistors, as described in section 10.1.

Separate varactors are recommended for coarse and fine compen-

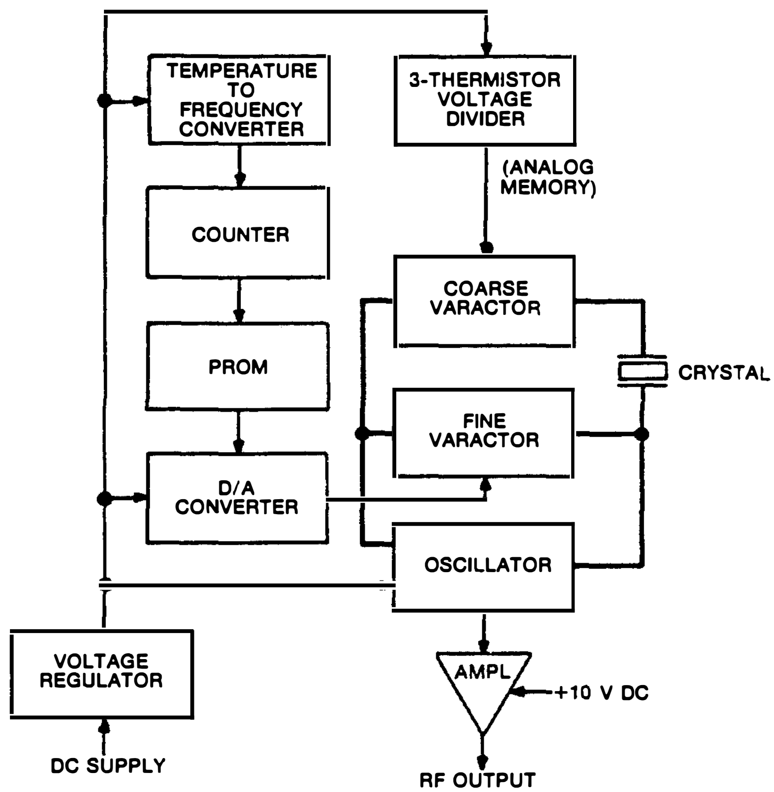

Figure 10.14. Hybrid temperature-compensated crystal oscillator: block diagram.

sation, so that the size of fine correction steps can be held nearly the same at all temperatures.

A block diagram of the fine compensation circuitry is shown in Figure 10-15. The object of this circuitry is to correct errors greater than the stability specification that remain after coarse compensation. This is accomplished with the programmable memory that remembers the proper, independent correction voltages to apply at regular intervals in the temperature range.

For purposes of this discussion, a ±5 parts in 10^8 frequency stability specification over the -40°C to +80°C temperature range is assumed. This is about the limit of what can be achieved due to hysteresis effects in the crystal and other oscillator components. The hybrid

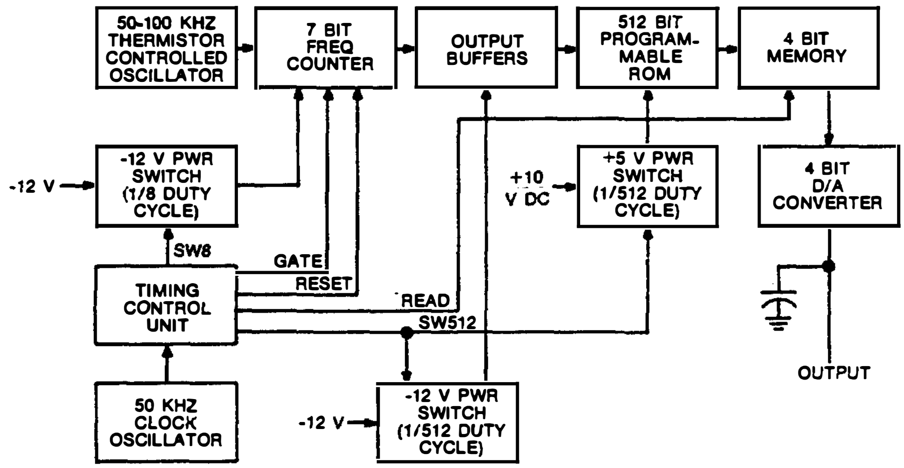

Figure 10.15. Digital fine-compensation network: block diagram.

approach can, of course, be used effectively in the 1-2 parts in 10^7 range but, as a practical matter, either straight analog or straight digital compensation (discussed in section 10.3) can be more economically employed for lesser stabilities.

Most of the development on the hybrid approach was accomplished during the early 1970s when the availability of PROMs and A/D converters in small sizes was relatively limited. Therefore, instead of using a temperature sensor followed by an A/D converter as described in section 10.3, a temperature-sensitive *RC* oscillator was used as the sensor, and the frequency counter as a means of converting the temperature to digital form.

The PROM was then addressed by the states of the counter. The D/A circuit then converts the output words of the programmed PROM to an analog voltage for TCXO correction. A clock and associated timing logic provide periodic updates and in general regulate the sequential operation of the counter.

Because of the relatively high power consumption of the PROM and the counters, switches are provided to sequence them on only when they are actually used; the control signals for these switches are generated by the timing control unit.

The required programming for the PROM is determined by stabilizing the TCXO at fixed temperatures, recording the states of the temperature registers, and simulating the correction output word with a manual switch. Required programming at intermediate temperatures is interpolated, and the entire PROM is then programmed and installed in the TCXO.

The timing signals for the digital circuitry are shown in Figure 10-16. These signals were developed in the custom MOS chip called DIGITCXO.* The first event, at the beginning of a cycle, is to energize the frequency counter flip-flops. This is accomplished by SW8 and the -12-V switch shown in Figure 10-15. Once this is accomplished, the counter flip-flops (on the chip) are reset by a 20-μs pulse. The counter gate is then opened for approximately 2 ms. Upon completion of the count, the PROM is energized by SW512, and the latch is pulsed to store the outputs of the ROM. All circuits, except the timing control, are then deenergized for 18 ms. The DIGITCXO chip contains the 7-bit frequency counter and timing control unit. The finished chip measures 0.125 X 0.145 inch and was fabricated and packaged in a 22-pin, 0.5-inch round ceramic package by the Collins MOS facility at Newport Beach, California.

Compensation of the TCXOs is accomplished with the aid of an interface adapter which replaces the ROM during compensation. A 16-position rotary switch with binary format substitutes for the PROM output lines. The adapter allows the operator to stop, hold, and read an address and update by depressing a switch. The memory location being addressed is displayed in a decimal format using a 3-digit display.

Coarse compensation is accomplished with the ROM simulator switch set at midrange and is carried out using conventional techniques. The coarse network compensates the TCXO to ±4 parts in 10^7 from -40°C to +80°C.

After the coarse compensation has been completed, the following steps are used for fine compensation:

a. Seal the cover on the coarse portion of the TCXO in preparation for fine compensation.
b. Stabilize the unit at room temperature for a minimum of

*Developed under sponsorship of the Solid-State and Frequency Control Division of the Electronics Components Laboratory, United States Army Electronics Command, Contract No. DAAB07-71-C-0136.

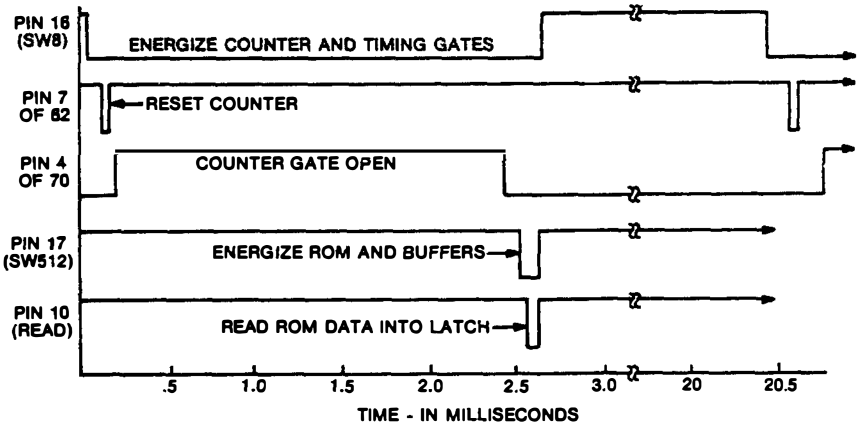

Figure 10.16. Timing diagram for MOS chip DIGITCXO.

10 hours. Beginning at -40°C, stabilize the sealed, coarsely compensated TCXO in 4–5°C intervals up to +80°C. At each temperature, record the PROM address and the decimal number of the (simulated) ROM output word that produces the smallest frequency error.

c. Tabulate the recorded PROM addresses and the desired corresponding output words. Estimate the required output words for intermediate PROM addresses by linear interpolation. (That is, if output words 8 and 3 were found to be required at addresses 107 and 112, respective intermediate interpolations are: 7 at 108, 6 at 109, 5 at 110, and 4 at 111.)
d. Program a PROM with the desired information using a PROM programmer.
e. Remove the cabling harness from the TCXO and install the programmed PROM. Clean the circuit boards and postcoat. Attach cover over digital compensation boards. (Alternatively, a confirming temperature run may be made before postcoating.)
f. Stabilize unit at room temperature for at least 10 hours. Repeat the preceding -40°C to +80°C temperature run at the same 4- or 5-degree increments to verify satisfactory performance.

The final frequency-temperature characteristic of a typical complete TCXO is graphed in Figure 10-17, along with the frequency-

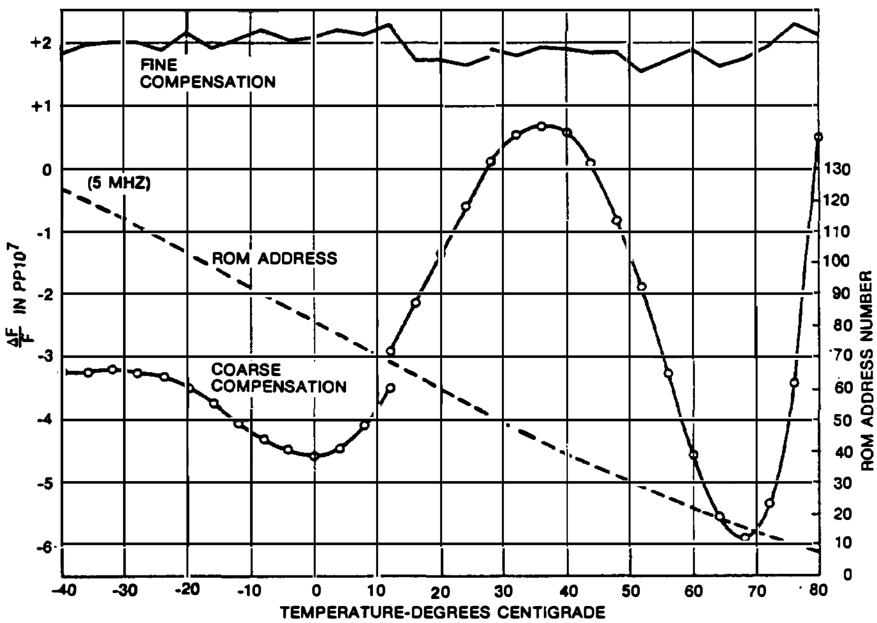

Figure 10.17. Characteristics of SN 8 after coarse and fine compensation.

temperature characteristic of the unit after coarse compensation. For this oscillator, the total frequency deviation was 70 parts in 10^8 before fine compensation and 7.5 parts in 10^8 after. Note that the curve has a discontinuity in midrange, caused by stopping the temperature run overnight. Stabilizing every 4°C from -40°C to +30°C, a complete temperature run requires two days. Also in the same figure is a plot of the PROM address versus temperature, indicating that a reasonably linear relationship was obtained.

10.3. DIGITAL TEMPERATURE COMPENSATION

The advent of larger PROMs and integrated A/D converters has simplified the compensation process so that TCXOs using entirely digital compensation are practical. The block diagram of such a unit is shown in Figure 10-18.

The crystal oscillator contains a single varactor, as in the case of the analog-compensated oscillators and, by application of the proper

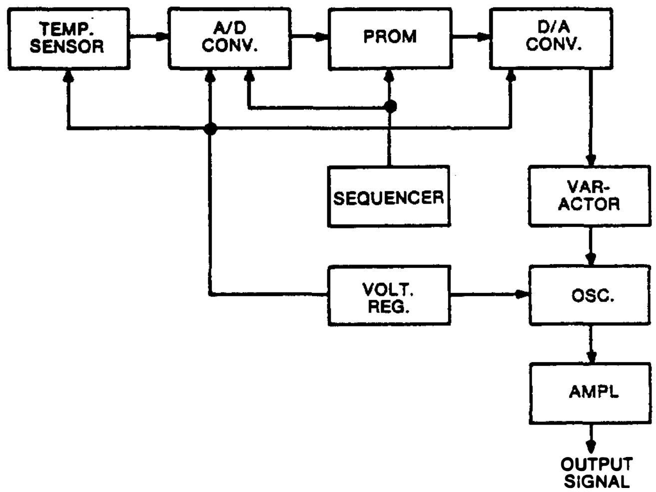

Figure 10-18. Digitally temperature compensated oscillator.

voltage to this varactor, the frequency is pulled by exactly the amount required to compensate for the temperature drift. In digital TCXOs it is generally desirable to use a hyper-abrupt varactor, with an exponent near unity, which gives a nearly linear frequency-voltage curve. The voltage range required can be found by the method outlined in section 10.1 with the aid of equations (10-3), (10-6), and (10-7). It should be noted that a voltage of less than about 1 V should be avoided because the RF voltage across the varactor may cause rectification and override the correction voltage.

The actual correction voltage is obtained in the following manner. First the voltage from the temperature sensor, such as a thermistor or diode, is digitized using the A/D converter. The digitized temperature word is then used as an address for the memory which contains the correction voltage required for the oscillator at that particular temperature. The contents of the memory location are latched into a digital-to-analog converter and the analog voltage is applied to the varactor. Since temperature changes relatively slowly, continuous corrections are not required. The temperature of an oscillator rarely changes more than 10 degrees per minute, and since the maximum rate of frequency change is less than 1 ppm/°C, a few corrections per second are sufficient. Consequently the A/D converter and the PROM can be turned off most of the time to save power and may be pulsed on only momentarily when a new correction is being made.

In most cases, it is desirable to minimize the memory required by the TCXO; thus it is important to choose the optimum word size for a given stability. It is most convenient to use uniformly spaced temperature intervals to address the memory. The slope of the frequency–temperature curve of a crystal, of course, varies greatly over the temperature range, as can be seen from Figure 5-6. The memory word size and capacity must be adequate to accommodate the worst-case slope. For a typical TCXO crystal with a frequency difference between the upper and lower turning points of about 32 ppm, we find slopes on the order of 1.4 ppm/°C at -55°C, -0.5 ppm/°C at 25°C, and 0.7 ppm/°C at 85°C. Let the worst-case slope be represented by S. Figure 10-19 shows how the compensation varies over a temperature interval from t_1 to t_2 if the exact compensation values are used at t_1 and t_2. The worst-case error occurs just before t_2 is reached when the frequency correction contained in the t_1 address is still being used but the crystal requires the value near t_2. This error can be cut essentially in half by overcompensating at t_1 so that the compensation is correct midway between t_1 and t_2. This is shown graphically between t_k and t_{k+1} in Figure 10-19. The frequency error due to the slope is then given by:

$$\Delta f_1 = \frac{(t_{k+1} - t_k)\,S}{2}. \tag{10-20}$$

Since a finite memory word size is used, an additional error occurs due to the fact that the exact desired value cannot always be obtained with a finite word size. In the worst case, the frequency can be set only to within one-half the frequency change represented by the least significant bit of the memory. Let this error be Δf_2. Then

$$\Delta f_2 = \frac{\text{total frequency correction range}}{2\ (\text{no. of correction levels})} \tag{10-21}$$

and the total worst-case frequency error is given by

$$\Delta f = \Delta f_1 + \Delta f_2. \tag{10-22}$$

We may then write:

$$\Delta f = \frac{S}{2}\left(\frac{T}{n}\right) + \frac{F}{2}\left(\frac{1}{2^b}\right), \tag{10-23}$$

where

S = maximum frequency–temperature slope of the crystal, in parts per million per Celsius degree.
T = the total temperature range over which the oscillator must operate, in Celsius degrees.
n = the number of words in the memory. Then each temperature interval is given by $t_{k+1} - t_k = T/n$.
F = the maximum peak-to-peak frequency excursion of the crystal, in parts per million.
b = the number of bits in each correction word.
Δf = the maximum frequency error to be allowed; in parts per million.

We wish to minimize the total number of memory bits required given by

$$M = nb. \tag{10-24}$$

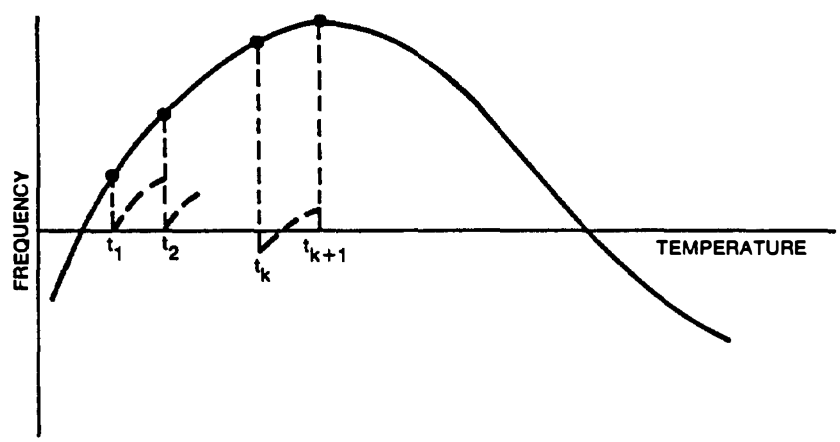

Figure 10-19. Frequency–temperature curve with exact compensation at t_1 and t_2.

Solving equation (10-23) for n gives

$$n = \frac{ST}{2\Delta f - (F/2^b)}. \qquad (10\text{-}25)$$

Substituting equation (10-25) into equation (10-24) gives

$$M = \frac{bST}{2\Delta f - (F/2^b)}. \qquad (10\text{-}26)$$

We may determine the value of b to minimize M by differentiating and setting $dM/db = 0$. We find

$$\frac{dM}{db} = \frac{\left(2\Delta f - \frac{F}{2^b}\right) ST - 2^{-b} bSTF \ln 2}{\left(2\Delta f - \frac{F}{2^b}\right)^2}. \qquad (10\text{-}27)$$

Equation (10-27) is zero if the numerator is zero. Setting the numerator to zero leads to the expression

$$2^b = \frac{F(1 + b \ln 2)}{2\Delta f}. \qquad (10\text{-}28)$$

Equation (10-28) cannot be solved in closed form; it must be evaluated by trial and error. Once b, the word size, has been determined, the number of words required can then be found from equation (10-25).

As an example, suppose that the following values are assumed:

$\Delta f = 0.1$ ppm,
$F = 32$ ppm,
$T = 85°\text{C} - (-55°\text{C}) = 140°\text{C}$, and
$S = 1.4$ ppm/°C.

Then from equation (10-28) we find

$$b \doteq 10.35 \qquad \text{for} \qquad \Delta f = 0.1 \text{ ppm}.$$

For $\Delta f = 0.5$ and 3 ppm, the values of b are 7.65 and 4.45, respectively. The values of M from equation (10-26) are given in Table 10-1 for several values of b and frequency stabilities of 0.1, 0.5, and 3 ppm for the crystal and temperature range above. Thus we see that it is possible to build a 0.5-ppm TCXO with an 8 × 256 PROM. In

Table 10-1. Memory Size for F = 32 ppm, S = 1.4 ppm, and T = 140°C.

Word size (bits)	Memory size (bits)		
	0.1 ppm	0.5 ppm	3 ppm
4	–	–	196
5	–	–	196
6	–	–	214
7	–	1,829	238
8	20,906	1,792	267
10	11,615	2,023	–
11	11,694	–	–
12	12,238	–	–

many cases it may be convenient not to offset the corrections as was done at t_k and t_{k+1} in Figure 10-19 to achieve optimum performance. If compensation is accomplished simply by using the nearest available value at the temperature breakpoints, then twice the number of words are required.*

10.4. TEMPERATURE COMPENSATION WITH MICROPROCESSORS

From section 10.3 it can be seen that the memory requirements for digital compensation beyond 0.5 ppm are substantial and that it is desirable to operate on the stored data in some manner to reduce the number of correction values required. Perhaps the simplest algorithm which can be used is to interpolate between stored data points. This can be accomplished in several ways using digital logic or digital–analog combinations. Perhaps the most attractive means, however, is by the use of a microprocessor. Because of the availability of low-cost microprocessors, many items of communications equipment are being designed with a processor. In some cases, the microprocessor can be used to generate frequency corrections during idle time. A one-shot multivibrator can be used to request an interrupt every few seconds, or the processor may be programmed to service the TCXO

*Digital compensation of crystal oscillators is discussed in reference 47, which also contains several interesting variations of the basic approach discussed here.

at regular intervals. In other applications, as minimum microprocessor systems become available with self-contained I/O, PROM, and RAM on the chip, it is desirable to include a dedicated microprocessor in a semiprecision or precision frequency standard. The processor can be pulsed on momentarily to generate a correction and then turned off to save power and reduce self-heating.

An experiment was conducted to demonstrate the feasibility of temperature-compensating a crystal oscillator using the INTEL-8080 processor. A linear interpolation program was used to generate correction voltages from the following equation:

$$V = V_n + \frac{(V_{n+1} - V_n)(t - t_n)}{(t_{n+1} - t_n)}. \tag{10-29}$$

Here the temperature t is assumed to be between the stored values t_n and t_{n+1}, which correspond to compensating voltages of V_n and V_{n+1}, respectively.

A linear temperature sensor was used in the crystal oscillator and the output of the sensor was converted to an 8-bit digital number using a single-chip A/D converter. After the correction voltage was calculated, the output was converted to an analog signal and applied to the varactor. The program was written to allow 16-bit temperature data, although only 8 bits were used for the test oscillator.* It should be noted that although 16-bit temperature words can be accepted, the difference between any two adjacent temperatures may not exceed 7 bits.

A flow chart of the temperature-compensation program is given in Figure 10-20. Once the temperature is determined, a search is made for a correction value. If the exact value is found, no calculation is required and a test is made to determine if the correction voltage is the same as that determined on the previous pass. If so, the output value is left unchanged and a branch is made to repeat the program. If the correction value is different, the new value is read into the output latch and a branch is executed to the beginning of the pro-

*It is also possible to determine the temperature by using the processor to count the frequency of a thermistor-controlled *RC* oscillator. Approximately 33 machine level instructions are required to determine temperature in this way. The method was not used in this experiment.

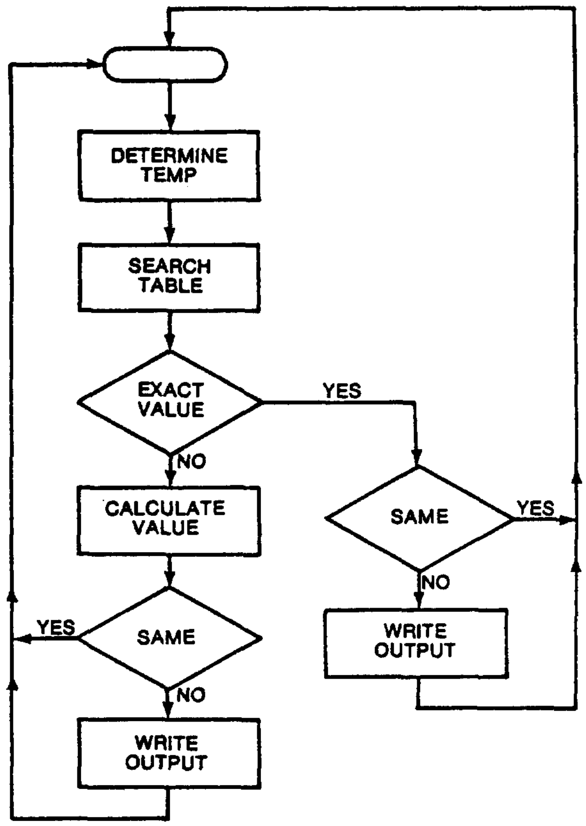

Figure 10-20. Overall flow chart of temperature compensation program.

gram. In the more likely event that the exact correction value is not stored for the particular ambient temperature under consideration, the search routine finds the nearest temperature-voltage pair above and below the actual temperature. The interpolation program then calculates a correction voltage based on equation (10-29), and a test is made to determine if the correction is different from the value found in the previous pass. If so, the output latch is updated and control is passed to the beginning of the program. If the output is the same, the latch is left unchanged.

A graph of the curve for the uncompensated crystal oscillator is shown in Figure 10-21 along with the final compensated curve. The

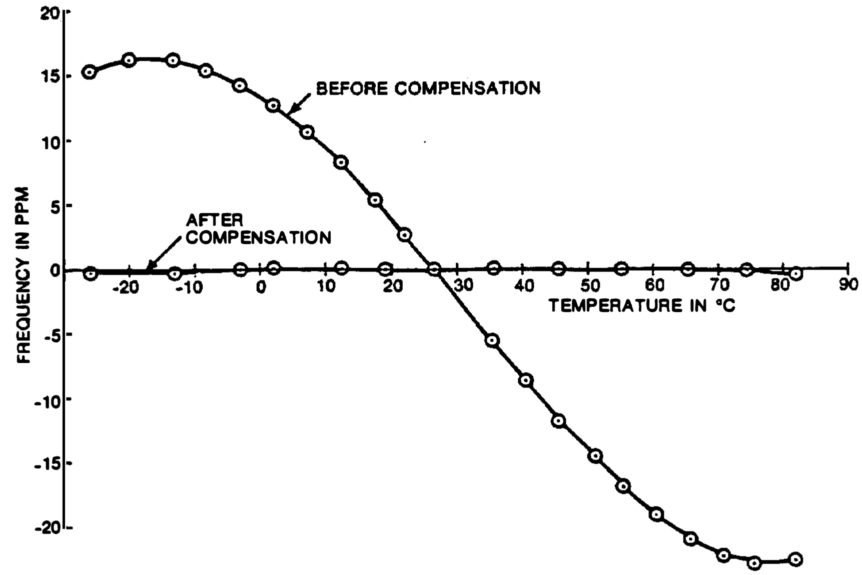

Figure 10-21. Frequency-Temperature for microprocessor compensated crystal oscillator.

compensated curve is also shown in Figure 10-22 with the ordinate expanded by a factor of 25. As can be seen, the frequency of this 5-MHz crystal oscillator is within $+2 \times 10^{-7}$ to -4×10^{-7} of the normal frequency over the entire temperature range from -26°C to +82°C.* A schematic diagram of the oscillator is shown in Figure 10-23. The A/D converter, not shown, was an MM4357. The D/A converter, shown in Figure 10-24, consists of 8 CMOS buffers followed by a ladder network. A simplified block diagram of the processor is shown in Figure 10-25. An INTEL-MCS-80 design system was used, and the program for the test oscillator was stored in RAM via a TTY.

The test setup is shown in Figure 10-26 and includes the TTY as well as a small test fixture used to monitor the temperature. The test fixture also has the capability to force the digital output to any

*The processor itself was not included in the temperature chamber; however, the crystal oscillator as well as the A/D and D/A converters were exposed to the temperature change.

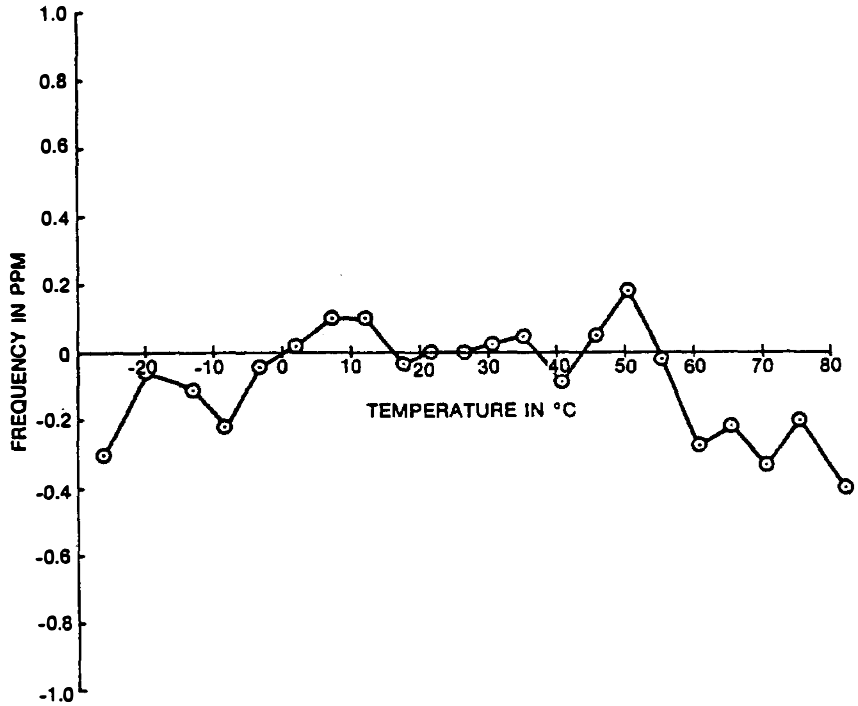

Figure 10-22. Frequency–Temperature for microprocessor compensated crystal oscillator (expanded scale).

value, thus allowing convenient data taking on the initial temperature run when the correction table is being determined. The oscillator is initially run over temperature and, at intervals of 5–10 degrees, the output switches are adjusted to put the oscillator on frequency. The temperature (address) is then read and recorded along with the correction required. The values used in this experiment are listed in hexadecimal notation, in Table 10-2. Photographs of the temperature chamber, the processor, test fixture, and oscillator are shown in Figures 10-27, 28, 29, and 30.

The microprocessor program was written in assembly language and requires 221 bytes of storage. In addition, 10 bytes of RAM are required as scratch-pad memory. A listing of the memory assignments is given in Tables 10-3 and 10-4.

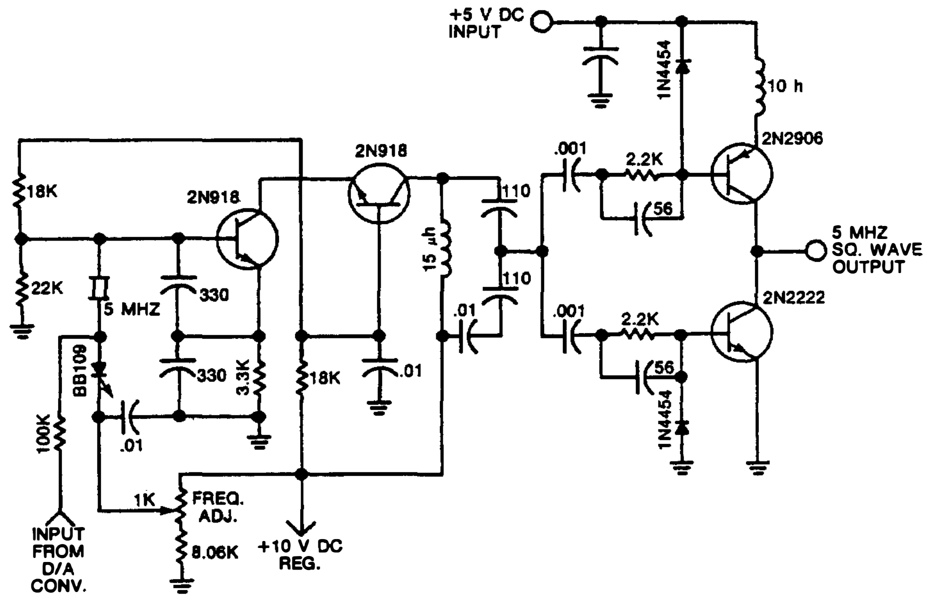

Figure 10-23. Schematic diagram of experimental oscillator using INTEL-8080 processor.

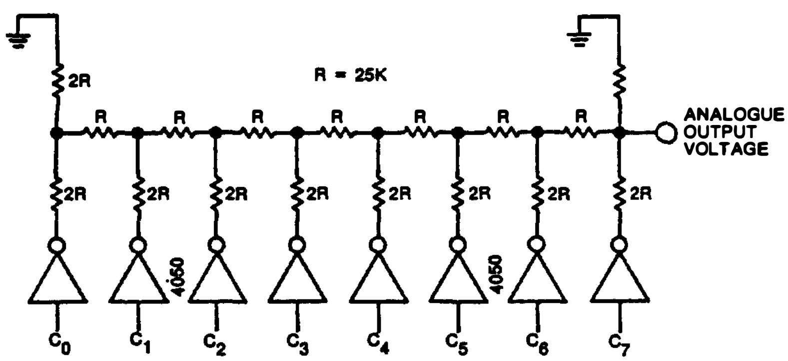

Figure 10-24. Digital-to-analog converter used with TCXO shown in Figure 10-23.

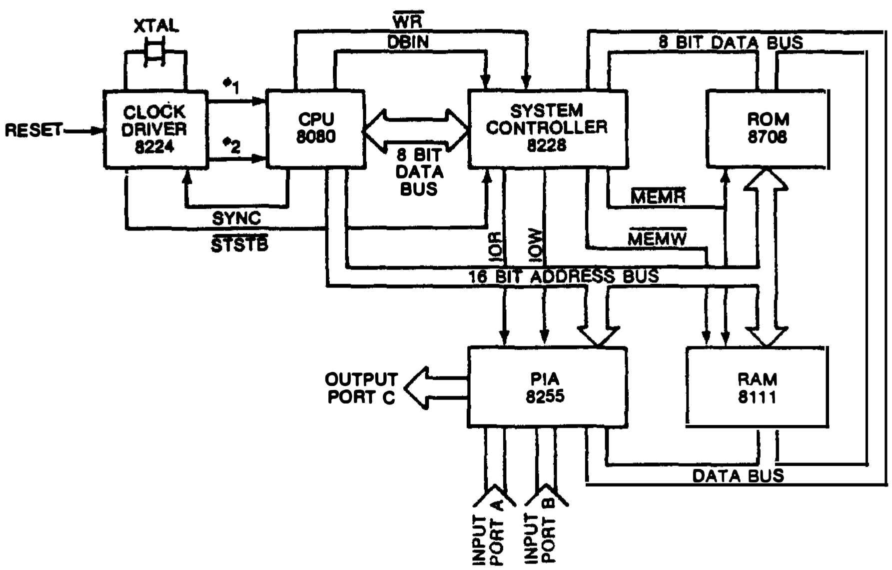

Figure 10-25. Simplified block diagram of processor used with TCXO shown in Figure 10-23.

Table 10-2. Stored Temperature-Frequency Correction Data.

Temp.	Corr.	Temp.	Corr.
00	00	78	A5
0A	61	82	8D
14	A3	8C	74
1E	CA	96	5D
28	DF	A0	45
32	ED	AA	30
3C	F0	B4	1E
46	EE	BE	12
50	E7	C8	0D
5A	DC	D2	0F
64	CC	D7	13
6E	BA	FF	FF

Figure 10-26. Test setup for microprocessor temperature compensation.

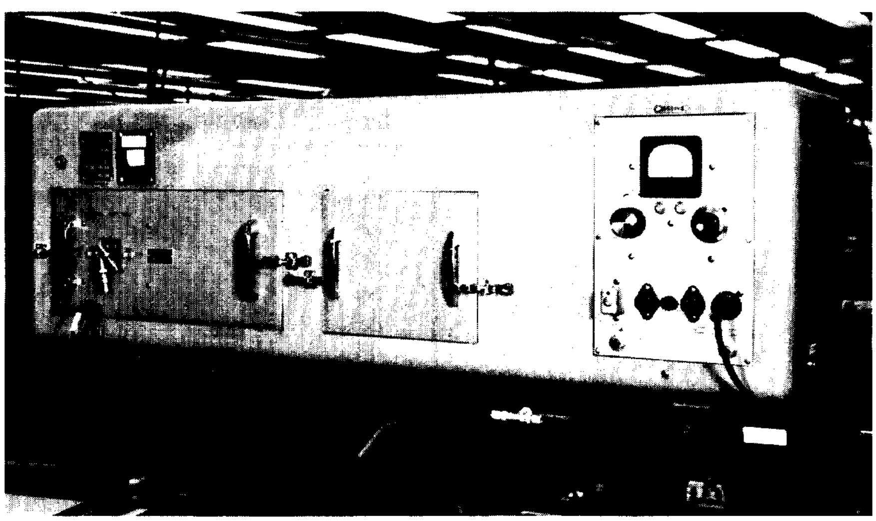

Figure 10-27. Temperature chamber used in experiment.

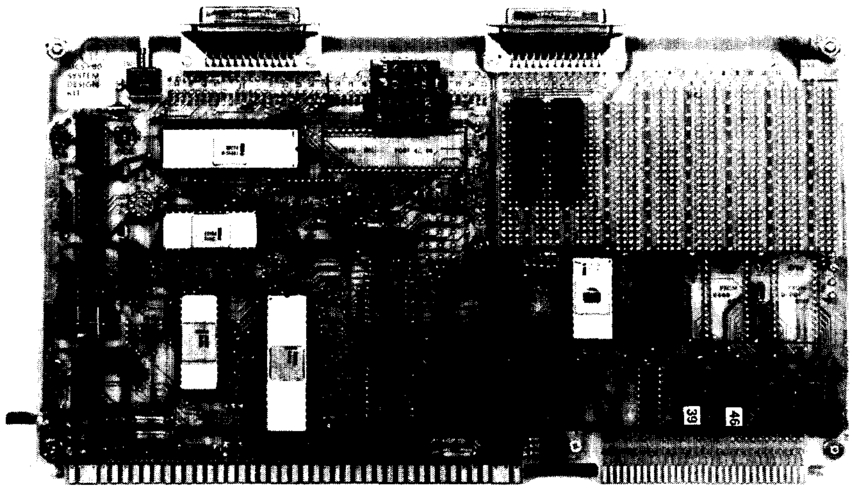

Figure 10-28. Processor used in experiment.

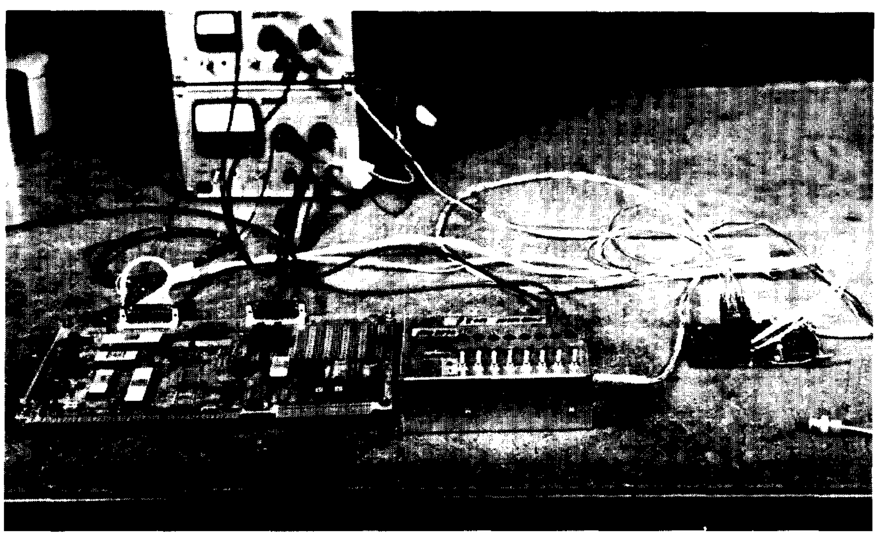

Figure 10-29. Close-up of test fixture and processor.

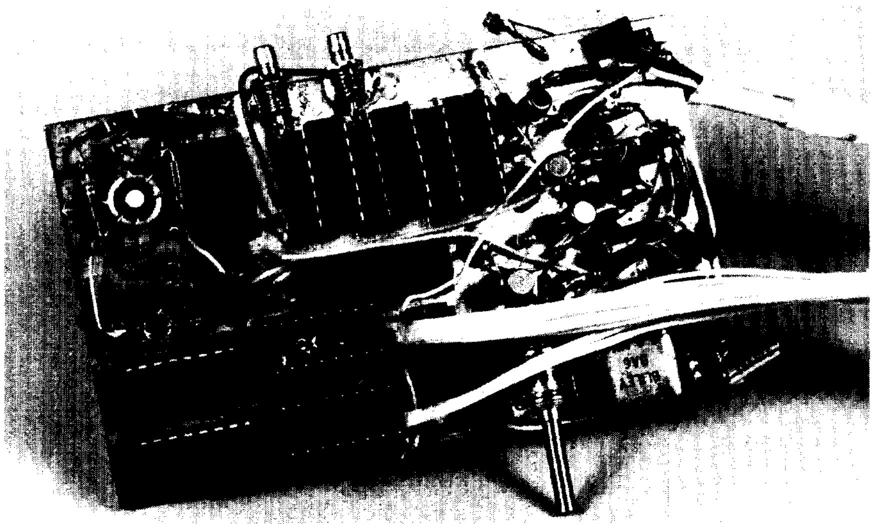

Figure 10-30. Oscillator used in experiment.

Table 10-3. Memory Usage.

Description	Location
Ambient temperature	
least significant byte (LSB)	PIAIA
most significant byte (MSB)	PIAIB
Stored correction data	
T1 (LSB)	DTA
T1 (MSB)	DTA+1
F1	DTA+2
T2 (LSB)	DTA+3
T2 (MSB)	DTA+4
F2 (LSB)	DTA+5
–	
–	
–	
–	
–	
End of file	
FF	DTA+n-1
FF	DTA+n
Correction voltage output	PIAOC

Table 10-4. Internal Memory and Register Usage.[a]

Description	Register/Memory
Ambient temperature	
T(LSB)	RAM
T(MSB)	RAM+1
Output to interpolation program	
TN(LSB)	RAM+3
TN(MSB)	RAM+4
FN	RAM+5
TN+1(LSB)	RAM+6
TN+1(MSB)	RAM+7
FN+1	RAM+8
FN+1−FN[b]	RAM+8
Working registers	
sign of $F_{n+1} - F_n$	RAM+2
dividend $T - T_n$	C
divisor $T_{n+1} - T_n$	D
quotient and multiplier $(T - T_1)/(T_{n+1} - T_n)$	E
multiplicand $(F_{n+1} - F_n)$	A
product	HL
counter for multiplication and division	B
store previous output	RAM+9

[a]A listing of the program is reproduced on the following pages.
[b]F_{n+1} in RAM+8 is destroyed by the program after $F_{n+1} - F_n$ is formed.

The program is loaded beginning at a location called ROM, which for the MCS-80 system was assigned a value 1200 in hexadecimal (H). The first scratch-pad location is called RAM and was assigned a value 1365H. The stored data table begins at a location called DTA and has a value 1300H. The 8255 peripheral interface adapter was wired so that port A, designated PIAIA, has an address 14H; port B, designated PIAIB, a value 15H; and port C, designated PIAOC, an address 16H.

The frequency accuracy of a crystal oscillator which is compensated using microprocessor techniques depends on many of the same factors as other methods of temperature compensation. Among these

```
8080 MACRO ASSEMBLER, VER 2.4          ERRORS = 0 PAGE 1

1365                        ORG 1365H
1365              RAM:      DS 9
1300                        ORG 1300H
1300              DTA:      DS 75
0017                        PIACR SET 17H
0014                        PIAIA SET 14H
0015                        PIAIB SET 15H
0016                        PIAOC SET 16H
                                        ;BEGINNING OF LINEAR SEARCH PROGRAM
1200                        ORG 1200H   ;ADDRESS OF FIRST INSTRUCTION IN PROGRAM
1200   3E92       ROM:      MVI A,92H ;SET PIA FOR A AND B INPUT, C FOR OUTPUT
1202   D317                 OUT PIACR ; SET PIA A AND B FOR INPUT, C FOR OUTPUT
1204   DB14                 IN PIAIA  ; READ IN A PORT OF PIA, LSB OF TEMP
1206   216513               LXI H,RAM
1209   77                   MOV M, A
120A   DB15                 IN PIAIB  ;READ IN B PORT OF PIA, MSB OF TEMP
120C   23                   INX H
120D   77                   MOV M,A
120E   216513               LXI H, RAM
1211   5E                   MOV E, M
1212   23                   INX H
1213   56                   MOV D, M
1214   210013               LXI H,DTA       ;LOAD ADDRESS OF FIRST STORED COMPENSATION DATA
1217   7B         LOOP3:    MOV A,E         ;LOAD LSB OF ACTUAL TEMP INTO ACCUMULATOR
1218   96                   SUB M           ;SUBTRACT T-IN LSB
1219   47                   MOV B,A
121A   23                   INX H           ;SET ADDRESS FOR MSB OF STORED TEMP
121B   7A                   MOV A,D
121C   9E                   SBB M           ;SUBTRACT MOST SIGNIFICANT BIT OF TEMP T-TN
121D   DA4012               JC X5       ;RESULT NEG READ OUT STORED POINTS
1220   CA2612               JZ X15
1223   C32C12               JMP X14
1226   78         X15:      MOV A, B
1227   E600                 ANI 0
1229   CA3112               JZ X4
122C   23         X14:      INX H           ;SKIP FREQ CORRECTION
122D   23                   INX H           ;INCREMENT ADDRESS TO NEXT STORED TEMP POINT
122E   C31712               JMP LOOP3       ;JUMP BACK TO BEGINNING OF SEARCH ROUTINE
                                            ;THE FOLLOWING INSTRUCTIONS WRITE OUT THE FREQ
                                            ;CORRECTION WORD IF THE SENSED TEMPERATURE
                                            ;COINSIDES WITH A STORED TEMPERATURE EXACTLY
1231   23         X4:       INX H           ;ADVANCE HL TO STORED FREQ CORRECTION
1232   7E                   MOV A,M
1233   216E13               LXI H,RAM+9 ; LOAD ADDRESS OF PREVIOUS OUTPUT
1236   BE                   CMP M      ; COMPARE WITH PREVIOUS OUTPUT
1237   CA0412               JZ ROM+4   ;SKIP PRINT OUT IF OUTPUT SAME AS BEFORE
123A   77                   MOV M,A    ; STORE NEW OUTPUT IF DIFFERENT
123B   D316                 OUT PIAOC
123D   C30412               JMP ROM+4       ;TRANSFER CONTROL TO BEGINNING OF PROGRAM
1240   2B         X5:       DCX H
```

are hystereses, temperature transients, the inaccuracy in determining temperature, and the inaccuracy in setting analog correction voltage to the desired value. The microprocessor has several advantages over other methods of compensation, however. Since a search for stored correction values can be made, it is reasonable to store points closer together over portions of the temperature range where the crystal has the largest slope. It is also possible to use various algorithms to calculate the correction required between stored points. In this discussion, a linear interpolation is assumed. It is possible, however, to develop algorithms based on more than the two closest stored values, such as fitting the cubic equation of the crystal.

```
8080 MACRO ASSEMBLER, VER 2.4               ERRORS = 0 PAGE 2

1241  2B               DCX H
1242  2B               DCX H
1243  2B               DCX H          ;SET HL TO ADDRESS OF CORRECTION DATA BELOW TEMP
1244  116813           LXI D,RAM+3    ;LOAD ADDRESS WHERE DATA TO BE PLACED
1247  0606             MVI B,6        ;SET B TO TRANSFER 6 BYTES OF DATA
1249  7E         X6:   MOV A,M        ;READ DATA INTO ACCUMULATOR
124A  23               INX H          ;INCREMENT SOURCE ADDRESS
124B  EB               XCHG           ;TRANSFER IN DESTINATION ADDRESS
124C  77               MOV M,A        ;PLACE DATA AT DESTINATION ADDRESS
124D  23               INX H          ;INCREMENT DESTINATION ADDRESS
124E  EB               XCHG           ;SET UP SOURCE ADDRESS
124F  05               DCR B          ;DECREMENT COUNTER
1250  C24912           JNZ X6         ;IF TRANSFER COMPLETE, CONINUE
                                      ; BEGINNING OF INTERPOLATION PROGRAM
1253  216D13     BK1:  LXI H,RAM+6    ;LOAD ADDRESS OF F2
1256  7E               MOV A,M        ;LOAD F2 INTO ACCUMULATOR
1257  216A13           LXI H,RAM+5    ;LOAD ADDRESS OF F1
125A  5E               MOV E,M        ;PLACE F1 IN E
125B  BB               CMP E          ;COMPARE A-E,I.E. SET CY IF F2 L.T. F1
125C  DA6712           JC X7          ; JP IF F1 G.T. F2
125F  216713           LXI H,RAM+2    ;LOAD ADDRESS OF FLAG
1262  3600             MVI M,0        ;SIGN BIT 0 IF F1 L.T. F2
1264  C36F12           JMP X8         ;SKIP INTERCHANGE IF  F1 L.T. F2
1267  57         X7:   MOV D,A        ;INTERCHANGE E AND A
1268  7B               MOV A,E
1269  5A               MOV E,D
126A  216713           LXI H,RAM+2    ;SET UP ADDRESS OF SIGN FLAG
126D  36FF             MVI M,0FFH     ;SINCE F2-F1 IS NEG SET FLAG
126F  93         X8:   SUB E          ;FORM ABS F2-F1
1270  216013           LXI H,RAM+8    ;SET UP ADDRESS TO STORE ABS F2-F1
1273  77               MOV M,A        ;STORE DIFFERENCE
1274  216513           LXI H,RAM      ;SET UP ADDRESS OF T LSB
1277  7E               MOV A,M        ;ACCUMULATOR HOLDS LSB OF T
1278  216813           LXI H,RAM+3    ;SET UP ADDRESS OF T1 LSB
127B  96               SUB M          ;FORM T-T1
127C  4F         X16:  MOV C,A
127D  216B13           LXI H,RAM+6    ;SET UP ADDRESS OF T2 LSB
1280  7E               MOV A,M        ;T2 LSB IN ACC
1281  216813           LXI H,RAM+3    ;SET UP ADDRESS OF T1 LSB
1284  96               SUB M          ;ACCUMULATOR HOLDS T2-T1
1285  57         X17:  MOV D,A
                                      ;THE FOLLOWING INSTRUCTIONS CONTAIN
                                      ;THE 8 BIT DIVISION PROGRAM
1286  1E00       BK2:  MVI E,0        ;INITIALIZE QUITENT TO ZERO
1288  0609             MVI B,9H       ;SET UP COUNTER FOR 8 SHIFTS
128A  79         X11:  MOV A,C        ;PLACE DIVIDEND IN ACC LSB
128B  92               SUB D          ;TRY SUBTRACTION
128C  DA9E12           JC X5          ;JUMP IF SUBTRACTION UNSUCCRSSFUL
128F  17               RAL            ;SHIFT DIVIDEND
1290  4F               MOV C,A        ;MOVE SHIFTED DIVIDENT BACK TO C
1291  7B               MOV A,E
```

For this discussion, let the frequency error at any given temperature be represented by

$$E = St_{\mathrm{lsb}} + \frac{F}{2^b} + \delta \text{ ppm} \qquad (10\text{-}30)$$

where

E is the overall frequency error in parts per million;
S is the maximum slope of the frequency-temperature curve of the oscillator in parts per million per Celsius degree;
t_{lsb} is the temperature range represented by the least significant bit of the digital temperature input;
F is the total frequency pulling range of the varactor;

```
8080 MACRO ASSEMBLER, VER 2.4          ERRORS = 0 PAGE 3

1292  37                STC            ;SET CARRY
1293  17                RAL            ;ROTATE CARRT INTO QUOTENT
1294  5F                MOV E,A        ;MOVE QUOTENT BACK TO E
1295  C3A012            JMP X10
1298  79        X9:     MOV A,C        ;MOV C INTO ACC TO RESTORE
1299  3F                CMC            ;COMPLEMENT CARRY I.E. SET CY=0
129A  17                RAL            ; ROTATE DIVIDEND
129B  4F                MOV C,A        ;RESTORE LSB OF DIVIDEND
129C  AF                XRA A          ;CLEAR CARRY
129D  7B                MOV A,E        ;PLACE QUOTENT IN ACC
129E  17                RAL            ;ROTATE ZERO INTO QUOTENT
129F  5F                MOV E,A        ;REPLACE ROTATED QUOTENT IN E
12A0  05        X10:    DCR B          ;DECREMENT COUNTER
12A1  C2AA12            JNZ X11        ;PROCEED WITH NEW SUBTRACTION
                                       ;THE FOLLOWING INSTRUCTIONS PERFORM A 16X8
                                       ;BIT MULTIPLICATION
12A4  1600      BK3:    MVI D,0        ;SET MSB MULTIPLICAND TO ZERO
12A6  216D13            LXI H,RAM+8    ;SET UP ADDRESS OF F2-F1
12A9  7E                MOV A,M        ;MOV F2-F1 INTO ACCUMULATOR
12AA  210000            LXI H,0        ;INITIALIZE PRODUCT TO ZERO
12AD  0608              MVI B,8        ;SET UP CONTROL LOOP FOR 8 OPERATIONS
12AF  29        LOOP:   DAD H          ;SHIFT PARTIAL PRODUCT LEFT AND INTO CARRY
12B0  17                RAL            ;ROTATE MULTIPLIER BIT TO CARRY
12B1  D2B712            JNC DEC        ;TEST MULTIPLIER AT CARRY
12B4  19                DAD D          ;ADD MULTIPLICAND TO PARTIAL PRODUCT IF CY=1
12B5  CE00              ACI 0          ;ADD CARRY
12B7  05        DEC:    DCR B          ;DECREMENT B LOOP COUNTER
12B8  C2AF12            JNZ LOOP       ;REPEAT IF NOT 8 TIMES
12BB  EB                XCHG           ;PLACE PRODUCT IN DE
12BC  216713            LXI H, RAM+2   ;LOAD ADDRESS OF SIGN
12BF  AF                XRA A          ;CLEAR A
12C0  86                ADD M          ;BRING SIGN BIT INTO ACC
12C1  FACC12            JM X13         ;JUMP IF NEGATIVE PRODUCT
12C4  216A13            LXI H,RAM+5    ;LOAD ADDRESS OF F1
12C7  7E                MOV A,M        ;F1 TO ACCUMULATOR
12C8  82                ADD D          ;FORM CORRECTION
12C9  C3D112            JMP X12        ;GO TO READ OUT INSTRUCTIONS
12CC  216A13    X13:    LXI H,RAM+5    ;LOAD ADDRESS OF F1
12CF  7E                MOV A,M        ;F1 IN ACC
12D0  92                SUB D          ;FORM CORRECTION
12D1  216E13    X12:    LXI H,RAM+9    ; LOAD ADDRESS OF PREVIOUS OUTPUT
12D4  BE                CMP M          ; COMPARE WITH PREVIOUS OUTPUT
12D5  CA0412            JZ ROM+4       ;SKIP PRINT OUT IF OUTPUT SAME AS BEFORE
12D8  77                MOV M,A        ; STORE NEW OUTPUT IF DIFFERENT
12D9  D316              OUT PIAOC
12DB  C30412    BK4:    JMP ROM+4      ;START OVER
                        END
NO PROGRAM ERRORS
```

b is the number of bits in the digital correction word; and

δ is the error resulting from the spacing between stored correction values.

If a linear interpolation program is used, the error δ is the difference between the actual crystal curve and a straight line joining the two nearest stored correction values.

It is assumed here that a linear modulator is used so that the correction voltage is proportional to the frequency correction required.

It is well known that the frequency–temperature curve for a quartz crystal is a cubic equation of the form

$$\frac{\Delta f}{f} = A_1 X + A_2 X^2 + A_3 X^3 \text{ ppu} \qquad (10\text{-}31)$$

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                         SYMBOL TABLE

* 01

A      0007      B      0000      BK1    1253 *    BK2    1286 *
BK3    12A4 *    BK4    12D8 *    C      0001      D      0002
DEC    12B7      DIA    1300      E      0003      H      0004
L      0005      LOOP   12AF      LOOP1  1217      M      0006
PIACR  0017      PIAIA  0014      PIAIB  0015      PIAOC  0016
PSW    0006      RAM    1365      ROM    1200      SP     0006
X10    12A0      X11    128A      X12    1201      X13    12CC
X14    122C      X15    1226      X16    127C *    X17    1285 *
X4     1231      X5     1240      X6     1249      X7     1267
X8     126F      X9     1298
```

where $X = t - t_0$. The coefficients vary slightly with the crystal parameters and a comprehensive listing is given by Bechmann in ref. 4. From this reference one set of values for plated resonators using natural quartz are given below. For a fundamental-mode AT-cut crystal,

$$A_1 \doteq (\text{ANG})(-5.15 \times 10^{-6}) \tag{10-32}$$

$$A_2 \doteq (\text{ANG})(-4.5 \times 10^{-9}) - 0.1 \times 10^{-9} \tag{10-33}$$

$$A_3 \doteq (\text{ANG})(-20 \times 10^{-12}) + 130 \times 10^{-12} \tag{10-34}$$

where ANG is the angle in degrees of arc from the angle of cut to give a zero slope at t_0. (The term t is the temperature in Celsius degrees and t_0 is taken to be 20°C.)

For a third overtone AT-cut crystal,

$$A_1 \doteq (\text{ANG})(-5.15 \times 10^{-6}) \tag{10-35}$$

$$A_2 \doteq (\text{ANG})(-4.5 \times 10^{-9}) - 1.7 \times 10^{-9} \tag{10-36}$$

$$A_3 \doteq 105 \times 10^{-12} \tag{10-37}$$

and for a fifth overtone,

$$A_1 \doteq (\text{ANG})(-5.5 \times 10^{-6}) \tag{10-38}$$

$$A_2 \doteq (\text{ANG})(-4.5 \times 10^{-9}) - 1.2 \times 10^{-9} \tag{10-39}$$

$$A_3 \doteq 105 \times 10^{-12} \tag{10-40}$$

If we substitute $X = t - 20$ into equation (10-31) we obtain

$$\frac{\Delta f(t)}{f} = b_1 t + b_2 t^2 + b_3 t^3 + b_4 \tag{10-41}$$

where

$$b_1 = A_1 - 40A_2 + 1200A_3 \quad (10\text{-}42)$$

$$b_2 = A_2 - 60A_3 \quad (10\text{-}43)$$

$$b_3 = A_3 \quad (10\text{-}44)$$

$$b_4 = 400A_2 - 20A_1 - 8000A_3. \quad (10\text{-}45)$$

The microprocessor uses a linear interpolation algorithm of the form

$$f(t_1) + \frac{f(t_2) - f(t_1)}{(t_2 - t_1)}(t - t_1), \quad (10\text{-}46)$$

and the frequency error over the interval t_1 to t_2 is given by the difference between equations (10-41) and (10-46) and is

$$\delta = f(t) - f(t_1) - \frac{[f(t_2) - f(t_1)](t - t_1)}{(t_2 - t_1)}. \quad (10\text{-}47)$$

It is convenient in dealing with this equation to perform a coordinate transformation, as shown in Figure 10-31. Using the dotted axes we have

$$F(T) = f(t) - f(t_1) \quad \text{and} \quad T = t - t_1.$$

The equation (10-41) becomes

$$F(T) = b_1(T + t_1) + b_2(T + t_1)^2 + b_3(T + t_1)^3 + b_4 - f(t_1). \quad (10\text{-}48)$$

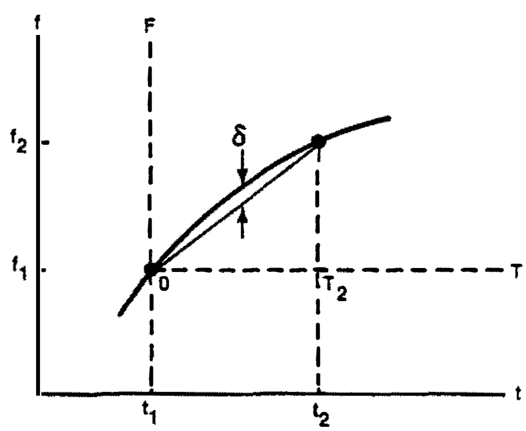

Figure 10-31. Frequency-Temperature curve transformation.

Expanding and simplifying gives

$$F(T) = (b_1 + 2b_2t_1 + 3b_3t_1^2)\,T + (b_2 + 3b_3t_1)\,T^2 + b_3T^3. \qquad (10\text{-}49)$$

We may then write equation (10-47) as

$$\delta = F(T) - \frac{F(T_2)\,T}{T_2}, \qquad 0 \leqslant T \leqslant T_2. \qquad (10\text{-}50)$$

Substituting from equation (10-49) we have

$$\delta = (b_1 + 2b_2t_1 + 3b_3t_1^2)\,T + (b_2 + 3b_3t_1)\,T^2 + b_3T^3 - [(b_1 + 2b_2t_1 + 3b_3t_1^2)\,T_2 + (b_2 + 3b_3t_1)\,T_2^2 + b_3T_2^3]\,\frac{T}{T_2}, \qquad (10\text{-}51)$$

which can be simplified to

$$\delta = -(b_2T_2 + 3b_3t_1T_2 + b_3T_2^2)\,T + (b_2 + 3b_3t_1)\,T^2 + b_3T^3. \qquad (10\text{-}52)$$

Obviously, $\delta = 0$ at $T = 0$ and $T = T_2$ because of the way the expression for δ was constructed. A maximum or minimum occurs near the center of the interval and is found by setting $d\delta/dT = 0$.

Let

$$K_1 = -(b_2T_2 + 3b_3t_1T_2 + b_3T_2^2) \qquad (10\text{-}53)$$

$$K_2 = (b_2 + 3b_3t_1). \qquad (10\text{-}54)$$

Then

$$\delta = K_1T + K_2T^2 + b_3T^3 \qquad (10\text{-}55)$$

$$\frac{d\delta}{dT} = K_1 + 2K_2T + 3b_3T^2. \qquad (10\text{-}56)$$

Setting this expression to zero and solving for T gives

$$T = -\frac{2K_2 \pm \sqrt{4K_2^2 - 12b_3K_1}}{6b_3} \qquad (10\text{-}57)$$

$$T = \frac{-K_2[1 \mp \sqrt{1 - (3b_3K_1/K_2^2)}]}{3b_3}. \qquad (10\text{-}58)$$

However, if the intervals are small so that

$$\left|\frac{3K_1b_3}{K_2^2}\right| = \left|\frac{-3b_3(b_2T_2 + 3b_3t_1T_2 + b_3T_2^2)}{(b_2 + 3b_3t_1)^2}\right| \ll 1 \qquad (10\text{-}59)$$

we may expand $\sqrt{1-(3b_3K_1/K_2^2)}$ using the binomial series and retain only the first two terms; thus

$$(1+m)^\alpha \doteq 1+\alpha m \qquad \text{for} \qquad m \ll 1$$

and equation (10-58) becomes

$$T=\frac{-K_2}{3b_3}\left(1-1+\frac{3b_3K_1}{2K_2^2}\right) \tag{10-60}$$

$$T=-\frac{K_1}{2K_2}. \tag{10-61}$$

Now substituting from (10-53) and (10-54)

$$T=\frac{b_2T_2+3b_3t_1T_2+b_3T_2^2}{2(b_2+3b_3t_1)}. \tag{10-62}$$

If the temperature interval is small as previously assumed,

$$(b_2+3b_3t_1) \gg b_3T_2 \qquad \text{and} \qquad T \doteq \frac{T_2(b_2+3b_3t_1)}{2(b_2+3b_3t_1)}=\frac{T_2}{2}. \tag{10-63}$$

Thus the maximum error occurs in the center of the temperature interval. Substituting this into equation (10-52) gives:

$$\delta_{max}=-(b_2T_2+3b_3t_1T_2+b_3T_2^2)\frac{T_2}{2}+(b_2+3b_3t_1)\frac{T_2^2}{4}+\frac{b_3T_2^3}{8}, \tag{10-64}$$

which may be simplified to

$$\delta_{max}=\frac{-T_2^2}{4}\left[\frac{3}{2}b_3T_2+b_2+3b_3t_1\right]. \tag{10-65}$$

Values of δ_{max} are given in Table 10-5 for temperature intervals of 3°C, 6°C, and 10°C using a typical TCXO crystal with ANG = 7 minutes of arc (0.1167 deg). Then from equations (10-32) to (10-34) and (10-42) to (10-45) we have

$$b_1=-4.228\times10^{-7}$$

$$b_2=-8.287\times10^{-9}$$

Table 10-5. Maximum Tracking Error for Stored Temperature Intervals of 3°C, 6°C, and 10°C.

Ambient temp. t_1 (°C)	δ_{max} (ppm)		
	$T_2 = 3°C$	$T_2 = 6°C$	$T_2 = 10°C$
-55	0.0648	0.254	0.686
-30	0.0432	0.167	0.447
-15	0.0303	0.116	0.303
0	0.0174	0.0642	0.159
10	0.0087	0.0298	0.0635
15	0.0044	0.0125	0.0157
25	-0.0042	-0.0219	-0.0800
50	-0.0257	-0.108	-0.319
65	-0.0387	-0.167	-0.463
80	-0.0516	-0.212	-0.607
95	-0.0645	-0.263	-0.750

$$b_3 = 1.2766 \times 10^{-10}$$

$$b_4 = 1.074 \times 10^{-5}.$$

It is possible, of course, to use the microprocessor to calculate the frequency correction directly from the cubic equation of the crystal or to use other algorithms taking advantage of more than the two nearest stored correction values. These methods may be used in connection with a fine-correction lookup table to compensate for minor irregularities in the crystal curve.

Temperature compensation using microprocessors is subject to the same ultimate limitations on accuracy as the digital method of compensation, namely temperature transients and frequency hysteresis. At the time of this writing the limit is about ±5 parts in 10^8 for an AT-cut crystal, because of hysteresis. As better crystals are developed it will be possible to make additional improvements in the compensation accuracy by the addition of more bits in the temperature and frequency correction words.

Research to improve the accuracy of TCXOs has been carried out in various laboratories for over two decades and will no doubt continue for some years to come. The requirement for highly accurate frequency and time standards which are also low-cost, low-power, and small in size is considerable, and promises many benefits to a broad spectrum of the electronics industry, including both military and commercial areas as well as in data processing and transmission equipment. Many techniques remain to be tried, and the use of microprocessors will no doubt play an important roll in implementing many of them.