7
Oscillator Circuits

This chapter treats a number of crystal oscillator configurations in detail. Design information as well as practical schematic diagrams for the recommended circuits are presented. In addition, the characteristics of the various recommended oscillator types are summarized and compared in table 7-1.

7.1. PIERCE, COLPITTS, AND CLAPP OSCILLATORS

The Pierce, Colpitts, and Clapp oscillators are actually the same circuit but with the ground point at a different location. Figure 7-1 shows the basic ac schematic diagram.

In the Pierce oscillator, the ac ground is at the emitter; in the Colpitts, at the collector; and in the Clapp, at the base. In a practical circuit, the stray capacitances and biasing resistors shunt different elements for each of the three configurations, making the circuits perform somewhat differently. Each of the circuits can be made to cover a broad range of crystal frequencies. These circuits are among the most noncritical of crystal oscillators and the permissible component tolerances are generally more than adequate. The output power is only moderate, however. Of the three possible configurations, the Pierce is the most desirable, electrically. This results from the stray capacitances appearing across capacitors C_1 and C_2, which generally are quite large. In the Clapp and Colpitts configurations, a good deal of the stray capacitance appears across the crystal, limiting the high-frequency application to about 30 MHz.

In the Pierce and Clapp oscillators, the base-biasing resistors are across large capacitors and thus do not affect the performance of the circuit. In the Colpitts configuration, however, the biasing resistors are across the crystal and degrade performance at lower frequencies (below about 3 MHz). The Colpitts configuration also is more sus-

Table 7-1. Recommended Crystal Oscillator Types.

Oscillator Type	Recommended Frequency Range	Relative Frequency Stability	Power Output	Waveform	Ability to Operate Properly When Circuit Stray Capacitance and Inductance Are Large	Ability to Operate Over a Band of Frequencies Without Retuning	Ease of Design	Remarks	Paragraph
Gate	16 kHz to 20 MHz	Low	Moderate	Square wave	Good	High	Moderate	Recommended for logic level output in low-stability applications.	7.6
Pierce	100 kHz to 20 MHz	High	Moderate	Poor at low freq, fair to good above 3 MHz	Very good	High	Simple	Recommended unless one side of crystal must be grounded.	7.2
Colpitts	1 to 20 MHz	Moderate	Moderate	Fair to good	Good	High	Moderate	Generally inferior to Pierce and Clapp. Recommended if Pierce and Clapp cannot be used.	7.3
Clapp	2 to 20 MHz	Moderate to high	Moderate	Fair to good	Good	High	Moderate	Generally inferior to Pierce. Recommended if one side of crystal must be grounded. Should not be used with low supply voltages.	7.4
Impedance inverting Pierce	20 to 75 MHz	High	Low	Good	Fair	Low	Difficult	Recommended if large stray inductances cannot be eliminated from crystal switch.	7.2.9 thru 7.2.11
Grounded base	20 to 150 MHz	Moderate	High	Good	Poor	Low	Moderate	Recommended if stray inductance and capacitance can be kept low.	7.5

ceptible to squegging. These problems can be overcome using a field effect transistor for lower frequencies, since very large gate-biasing resistors then can be used.

The Clapp oscillator has a unique disadvantage in that free-running oscillations can occur if a choke is used to supply the dc voltage to the collector. The problem is best solved by putting a fairly large resistor in series with the choke or by using a resistor alone. The resistance must be kept large, however, since it shunts the crystal. For this reason, the Clapp oscillator is not desirable for use with low supply voltages.

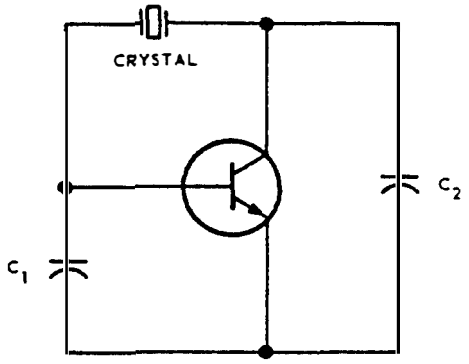

Figure 7.1. Pierce, Colpitts, and Clapp oscillators: basic ac schematic diagram.

Of the three possible configurations, the Pierce oscillator is generally the simplest and the Colpitts the most difficult to design. The Pierce oscillator has the disadvantage that one side of the crystal cannot be grounded, often making it undesirable for use with crystal switches.

The frequency stability of the Pierce oscillator is generally in the range from 0.0002 to 0.0005 percent worse than the stability of the crystal alone. The Clapp oscillator is slightly inferior to the Pierce and the Colpitts is slightly inferior to the Clapp in this respect. If no adjustment is provided to put the crystal exactly on frequency, additional frequency errors will be present as a result of differences in transistors, components, and crystal resistance.

7.2. PIERCE OSCILLATOR

7.2.1. Small-Signal Analysis

The general oscillator theory presented in Chapter 2 can be applied conveniently to the Pierce oscillator. Specifically, the conditions of oscillation are fulfilled in the following way. Referring to Figure 7-2, the basic phase shift network is composed of C_1, C_2, and the crystal, which looks inductive. Capacitors C_1 and C_2 are normally so large that they effectively swamp out the transistor output and input impedances. If this is the case, and if the effective resistance of the crystal is low, then the following explanation is applicable. The crystal looks inductive and is series resonant with capacitors C_1 and

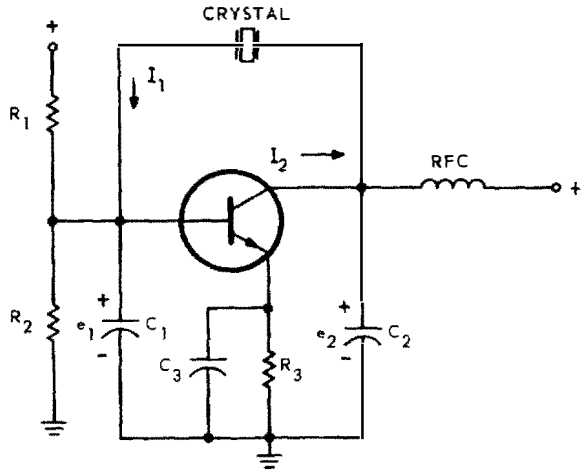

Figure 7-2. Pierce oscillator circuit: schematic diagram.

C_2. The frequency of oscillation automatically adjusts itself so that this is true. Therefore, the combination of the crystal and C_1 alone has a net inductive reactance at the operating frequency.

Consequently, current I_1 lags voltage e_2 by 90 degrees. Voltage e_1 being developed across capacitor C_1 lags current I_1 by 90 degrees, making it 180 degrees behind collector voltage e_2. Since the combination of C_1 and the crystal is resonant with C_2, the collector looks into a resistive load.

The phase shift through the transistor is 180 degrees and the total phase shift around the loop is 360 degrees.

The condition of a loop gain of unity can be found in the following manner. It can be shown (see Appendix E) that the ratio of the voltages

$$\frac{e_1}{e_2} \doteq -\left(\frac{C_2}{C_1}\right). \tag{7-1}$$

Putting this in terms of reactances gives

$$\frac{e_1}{e_2} \doteq -\left(\frac{X_1}{X_2}\right). \tag{7-2}$$

For oscillation to take place, the transistor gain A must be such that

$$A\left(\frac{e_1}{e_2}\right) \geqslant 1. \tag{7-3}$$

The transistor voltage gain is approximately given by

$$A = -g_{fe} Z_L \tag{7-4}$$

where g_{fe} is the transconductance of the transistor and Z_L is the load seen by the collector. It can be shown (see Appendix E) that this load is given by

$$Z_L \doteq \frac{X_2^2}{R_e},$$

where

$$X_2 = -\frac{1}{\omega C_2}. \tag{7-5}$$

Then

$$A = \frac{-g_{fe}(X_2)^2}{R_e} \tag{7-6}$$

and substituting this into equation 7-3 gives

$$-\left[\frac{g_{fe}(X_2)^2}{R_e}\right]\left[\frac{e_1}{e_2}\right] \geqslant 1 \tag{7-7}$$

but since

$$\frac{e_1}{e_2} = -\left(\frac{X_1}{X_2}\right), \qquad \frac{g_{fe}(X_2)^2}{R_e}\left(\frac{X_1}{X_2}\right) \geqslant 1 \tag{7-8}$$

or

$$g_{fe} X_1 X_2 \geqslant R_e \tag{7-9}$$

The loop gain is then

$$\left(\frac{g_{fe} X_1 X_2}{R_e}\right) \tag{7-10}$$

and must be greater than unity. To a first approximation we may use $g_{fe} = 0.04 I_e$, where g_{fe} is in mhos and I_e is in milliamperes.

This explanation is somewhat idealized because of the assumptions made. A rigorous analysis of the Pierce oscillator is given in Appendix B. The results are.

$$g_{fe} X_1 X_2 \geqslant R_e + K_1 \qquad \text{(gain equation)} \qquad (7\text{-}11)$$

$$X_1 + X_2 + X_e = 0 + K_2 \qquad \text{(phase shift equation)} \qquad (7\text{-}12)$$

where

g_{fe} = real part of the forward transfer admittance, sometimes referred to as the transconductance.
$X_1 = -1/\omega C_1$,
$X_2 = -1/\omega C_2$,
R_e = effective crystal resistance, and
X_e = crystal reactance.

K_1 and K_2 are corrective terms which are negligible if the previous assumptions are fulfilled. They are as follows:

$$K_1 = -X_1(X_2 + X_e)\, g_{ie} - X_2(X_1 + X_e)\, g_{oe} - R_e X_1 X_2 [g_{ie} g_{oe} + b_{fe} b_{re}] - b_{re} g_{fe} X_1 X_2 X_e \qquad (7\text{-}13)$$

$$K_2 = b_{fe} X_1 X_2 + X_1 X_2 X_e g_{ie} g_{oe} - R_e [X_1 g_{ie} + X_2 g_{oe}] + b_{re} X_1 X_2 + b_{re} b_{fe} X_1 X_2 X_e - b_{re} g_{fe} X_1 X_2 R_e. \qquad (7\text{-}14)$$

For definitions of the Y-parameters, refer to Chapter 6. The input and output short-circuit capacitances of the transistor may be accounted for by including them in C_1 and C_2, respectively. If the oscillator is loaded, the load must be included in the output admittance of the transistor; that is, g_{oe} in the equations should be [g_{oe} of the transistor + $(1/R_L)$], where R_L is the load.

In the case of field effect transistors at low frequencies, $y_{fe} = g_m$, $y_{ie} = 0$, $y_{oe} = 1/r_d$, $y_{re} = 0$, and the equations simplify as follows:

$$g_m X_1 X_2 \geqslant R_e - \frac{X_2(X_1 + X_e)}{r_d} \qquad (7\text{-}15)$$

$$X_1 + X_2 + X_e = -\frac{R_e X_2}{r_d} \qquad (7\text{-}16)$$

Equations (7-11) and (7-12) can be used best by successive approximation. The first values of X_1 and X_2 may be calculated assuming

that $K_1 = K_2 = 0$. These values of X_1 and X_2 then are substituted into the total equations. It should be obvious then which terms are negligible, and they are eliminated. The equations then are rewritten using the significant terms. Usually the remaining equation will be only moderately complicated.

In some cases the Y-parameters of the transistor may not be known or, from other considerations, the reader may elect to use a purely experimental approach in designing a Pierce oscillator. For such an approach, the following guidelines can be given. In general, C_1 and C_2 should be as large as possible but still allow the circuit to oscillate with two to three times the maximum permissible crystal resistance.* This usually results in the crystal reactance (X_e) being quite small. A trimmer capacitor is then placed in series with the crystal to bring it on frequency. (X_e in the equation then represents the reactance of the crystal in series with the trimmer.)

In the higher portion of the frequency range, C_1 and C_2 in series may become less than the desired crystal load capacitance for minimum gain requirements. The crystal then may be put on frequency by placing a variable inductor in series with it. This may be undesirable, however, since it can lead to free-running oscillations. A better solution may be to let $C_1 = C_2 = 2C_L$. This condition leads to a maximum X_1X_2 product for a given load capacitance C_L. If this does not allow sufficient gain, then a small inductor in series with the crystal must be used.

Regardless of the frequency, it is desirable to make

$$|X_1| << \frac{1}{g_{ie}}, \tag{7-17}$$

and

$$|X_2| << \frac{1}{g_{oe}}. \tag{7-18}$$

This minimizes the effects of transistor input and output admittances.

For a highly stable oscillator, the loading should be light. A good

*This can be determined by adding resistance in series with the crystal until oscillation will not occur.

rule to follow is to tap considerably farther down than for optimum matching. An example of this is shown in Figure 7-3, (see section 7.2.3 below), where the ratio of C_4/C_2 is larger than that required for maximum output.

Best stability occurs if C_1 and C_2 are as large as possible, because they swamp out any change in transistor input or output capacitance.

To a first approximation, it can be shown that maximum stability results if

$$\frac{C_2}{C_1} = \left[\frac{dC_{out}/dT}{dC_{in}/dT}\right]^{1/2} \tag{7-19}$$

where dC_{out}/dT is the change in collector-to-emitter capacity with respect to the parameter being studied, and dC_{in}/dT is the variation in base-to-emitter capacity with respect to the same parameter. The ratio C_2/C_1 usually is determined by other factors, however, such as crystal load capacitance, output voltage, or crystal drive. Since the load on the collector is $Z_L \doteq X_2^2/R_e$, larger outputs usually are obtained if X_2 is made large (small C_2).

It should be remembered that the equations derived using the Y-parameters are based on a linear analysis and predict starting conditions only. They give no indication concerning the final amplitude or of the crystal drive level. A method for determining the steady-state value of drive level as well as the output voltage is discussed in the following paragraphs.

7.2.2. Large-Signal Analysis

If the starting conditions for oscillation are satisfied, the amplitude of oscillation continues to grow until nonlinear effects reduce the effective loop gain to unity. If the starting conditions are satisfied at more than one frequency, oscillations begin at both frequencies and the one reaching the saturation amplitude first causes the other to die out. Normally, multiple or spurious oscillation is not a problem and will not be considered at this time.

In a transistor oscillator, the predominant nonlinearity occurs because the base-to-emitter junction is cut off during part of the cycle. As discussed in section 3.2 of Chapter 3, under certain conditions of biasing, collector saturation may also occur. Generally

collector saturation tends to increase the dependence of the oscillator on the supply voltage and is therefore avoided.

Assuming that collector saturation does not occur, the amplitude of oscillation can be determined by applying the nonlinear results of section 6.4 of Chapter 6. To accomplish this, the small-signal analysis of section 7.2.1 (above) is first completed.

The small-signal transconductance required for oscillation is found from equation (7-11) and is:

$$g_m = \frac{R_e + K_1}{X_1 X_2} \tag{7-20}$$

If the actual small-signal transconductance of the transistor is given by g_{m0}, then the excess small-signal loop gain is g_{m0}/g_m. This value is used to enter the graph of Figure 6-6 and determines the value of V which will be required to reduce the loop gain to unity. The value V is the normalized base-to-emitter voltage. The actual voltage is $E \cos \omega t$ where $E = VKT/q$. As noted earlier $KT/q \doteq 26$ mV at room temperature. Then using equation (7-1), the approximate collector voltage is found to be

$$e_2 = -e_1 \left(\frac{C_1}{C_2}\right) \tag{7-21}$$

where $e_1 = E/\sqrt{2}$ volts rms.

The crystal drive level is then given by

$$P_c = \frac{e_2^2 R_e}{X_2^2} \tag{7-22}$$

and should not exceed the manufacturer's specification.

The graph of Figure 6-6 can also be used to determine the increase in the effective input and output impedances of the transistor and the reduction in input capacitance:

$$g_{ie} \doteq \frac{g_{ieo}}{R_{\text{in}}/R_{\text{in}o}} \tag{7-23}$$

The transistor input capacitance was lumped into C_1; therefore it will also decrease with amplitude, causing a slight increase in frequency. If desired, the new values of g_{ie}, g_{oe}, and C_1 can be used in calculating the K_1 used in equation (7-20).

The graphs of Chapter 6 also provide an indication of the bias shift resulting from oscillation. This is shown in Figure 6-7. The value of V found earlier is used to determine the reduction in base-to-emitter voltage. An appropriate adjustment can then be made to the bias network to establish the desired steady-state value of emitter current.

Finally, the graph of Figure 6-8 can be used to determine the harmonic content of the collector current. Since the collector feeds the input of the π network containing the crystal and since for practical purposes the crystal is an open circuit at the harmonic frequencies, the collector voltage waveform can be determined by multiplying the appropriate harmonic current by the reactance of C_2 at that frequency.

The impedance seen by the collector at the fundamental frequency is approximately given by

$$Z = \frac{X_2^2}{R_e}. \tag{7-24}$$

Therefore the ratio of harmonic voltage to fundamental voltage is given by

$$\frac{e_n}{e_{\text{fund}}} = \frac{i_n (X_2/n)}{i_{\text{fund}} (X_2^2/R_e)} \tag{7-25}$$

$$\frac{e_n}{e_{\text{fund}}} = \frac{i_n R_e}{i_{\text{fund}} n X_2} \tag{7-26}$$

Where n is the harmonic number, i_n and i_{fund} can be read from the graph of Figure 6-8 knowing V, or from equation (6-24) by taking i_n/i_{fund} as the ratio of hyperbolic Bessel functions $I_n(V)/I_1(V)$.

If the oscillator is loaded heavily, Z must be appropriately adjusted and the fundamental component of the waveform will be reduced, compared to the harmonics.

Since the base voltage of the transistor is established by the crystal current through C_1, it has the best waveform.

In some applications a tank circuit tuned to a harmonic of the crystal frequency is inserted in the collector circuit to produce a frequency multiplier. This procedure generally works quite well, and the graph of Figure 6-8 can be used to estimate the harmonic output power.

In some applications of frequency standards, it is desirable to use emitter degeneration on the transistor, for example to reduce the $1/f$ noise. In these applications the graphs of Figures 6-6 through 6-8 do not apply. A piecewise linear analysis has been included, however, which gives good results if sufficient feedback is used.

This analysis assumes that the transistor, with feedback, is linear during that part of the cycle when it conducts and is completely shut off during the remainder of the cycle. The results are presented in Figures 6-10, 6-11, and 6-12. These graphs can be used in place of Figures 6-6, 6-7, and 6-8 in the previous description. The actual base-to-emitter voltage is found to be

$$E = VI_e(\text{mean})\,(R_f + r_e)_0 \tag{7-27}$$

where R_f is the emitter degeneration resistor, r_e is the intrinsic emitter resistance, I_e(mean) is the steady-state emitter current, and E is the peak base-to-ground voltage in volts.

In general the nonlinear analyses are not as accurate as the analyses we are accustomed to seeing based on linear models in small-signal applications. The results are, however, quite useful in the initial design of oscillator circuits and give a reasonable approximation when the cutoff frequency of the transistor is more than 10 or 20 times the operating frequency.

7.2.3. 1- to 3-MHz Pierce Oscillator*

Typical performance characteristics for the 1- to 3-MHz Pierce oscillator shown in Figure 7-3 are given below.

a. Crystal: CR-18/U or similar.
b. Load capacitance: 32 pF.
c. Drive level: 1–6 mW, depending on frequency and crystal resistance.
d. Factors affecting frequency stability are as follows:
   1. Temperature coefficient of crystal: ±0.005 percent from −55°C to +105°C.
   2. Aging rate of crystal: See section 5.7.

*A number of typical oscillator circuits are presented in this chapter. The performance indicated is that observed on a single circuit and may vary considerably with layout and components used. The circuits are listed as starting points only and should not be used without optimization and thorough testing in the configuration actually used. (See Chap. 8.)

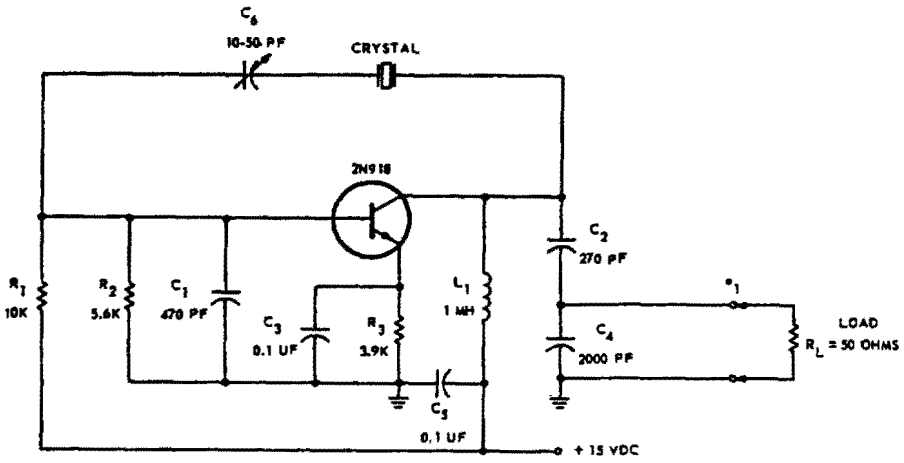

Figure 7-3. 1- to 3-MHz Pierce oscillator: schematic diagram.

3. Temperature stability of oscillator circuitry: 1.5 parts in 10^9/°C at 1 MHz, and 1.6 parts in 10^8/°C at 3 MHz.
4. Voltage coefficient of oscillator: 3 parts in 10^7 at 1 MHz, and 1 part in 10^7 at 3 MHz for a 10-percent supply voltage change.

e. Output: For $R_L = 50\ \Omega$, e_1 is approximately 0.25–0.40 V, depending on frequency and crystal resistance. Waveform at 1 MHz is poor.
f. Permissible load: $50 \leqslant R_L \leqslant \infty$.
g. Power input: 40 mW.

NOTE. Although the circuit will oscillate with any standard crystal in the 1- to-3-MHz range, some adjustment of C_6 is necessary over the frequency range to put crystals exactly on frequency.

7.2.4. 1- to 10-MHz Pierce Oscillator

Typical performance characteristics for the 1- to 10-MHz Pierce oscillator shown in Figure 7-4 are given below.

a. Crystal: CR-18/U or similar.
b. Load capacitance: 32 pF.
c. Drive level: 0.75–4 mW, depending on the frequency and crystal resistance.
d. Factors affecting frequency stability are as follows:

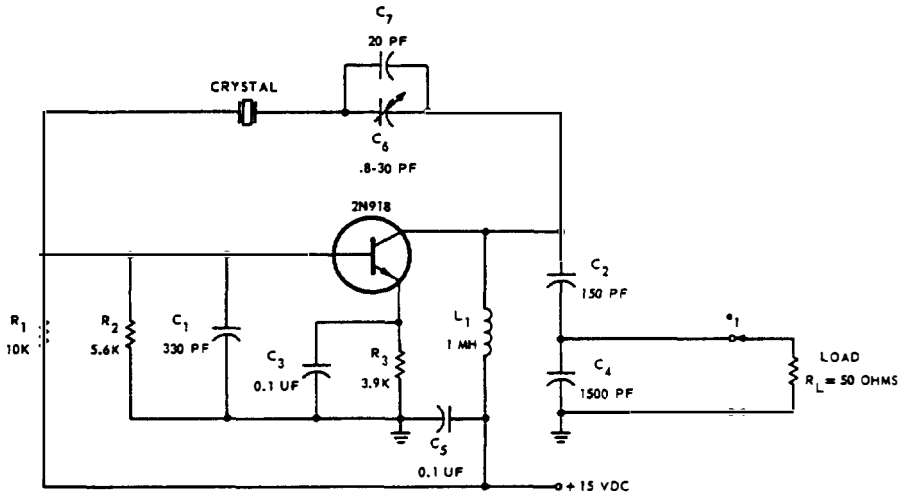

Figure 7-4. 1- to 10-MHz Pierce oscillator circuit: schematic diagram.

1. Temperature coefficient of crystal: ±0.005 percent from -55°C to +105°C.
2. Aging rate of crystal: See section 5.7.
3. Temperature stability of oscillator circuitry: 3 parts in 10^8/°C at 1 MHz, 2.2 parts in 10^8/°C at 5 MHz, and 1.5 parts in 10^8/°C at 10 MHz.
4. Voltage coefficient of oscillator: 1.5 parts in 10^6 at 1 MHz, 2.5 parts in 10^7 at 3 MHz, and 2.3 parts in 10^7 at 10 MHz for a 10-percent change in supply voltage.

e. Output: For $R_L = 50\ \Omega$, e_1 is approximately 0.02 V at 10 MHz, and 0.35 V at 3 MHz and 1 MHz. e_1 varies considerably with crystal resistance. The waveform below 3 MHz is poor. Distortion at 1 MHz is 30 percent; at 5 MHz, it is 6 percent.

f. Permissible load: $50 \leqslant R_L \leqslant \infty$.

g. Input power: 35 mW.

NOTE. Although the circuit will oscillate with any standard crystal in the 1- to 10-MHz range, some adjustment of C_6 is necessary over the frequency range to put crystals exactly on frequency.

7.2.5. 10- to 20-MHz Pierce Oscillator

Typical performance characteristics for the 10- to 20-MHz Pierce oscillator shown in Figure 7-5 are given below.

a. Crystal: CR-18/U, CR-66/U, or similar.
b. Load capacitance: 32 or 30 pF.
c. Drive level: 0.3–1.0 mW, depending on the frequency and crystal resistance.
d. Factors affecting frequency stability are as follows:
   1. Temperature coefficient of crystal: ±0.005 percent from −55°C to +105°C for CR-18/U, ±0.002 percent for CR-66/U.
   2. Aging rate of crystal: See section 5.7.
   3. Temperature stability of oscillator circuitry: 2.6 parts in 10^8/°C at 10 MHz and 2 parts in 10^8/°C at 20 MHz.
   4. Voltage coefficient of oscillator: 2 parts in 10^7 at 20 MHz and 4 parts in 10^8 at 10 MHz for a 10-percent supply voltage variation.
e. Output (see Note 1): For $R_L = 100\,\Omega$, e_1 is approximately 0.05–0.10 V, depending on frequency and crystal resistance. Voltage e_2 is in the range from 1.5 to 2.0 V.
f. Permissible load: $100 \leqslant R_L \leqslant \infty$.
g. Input power: 15 mW.

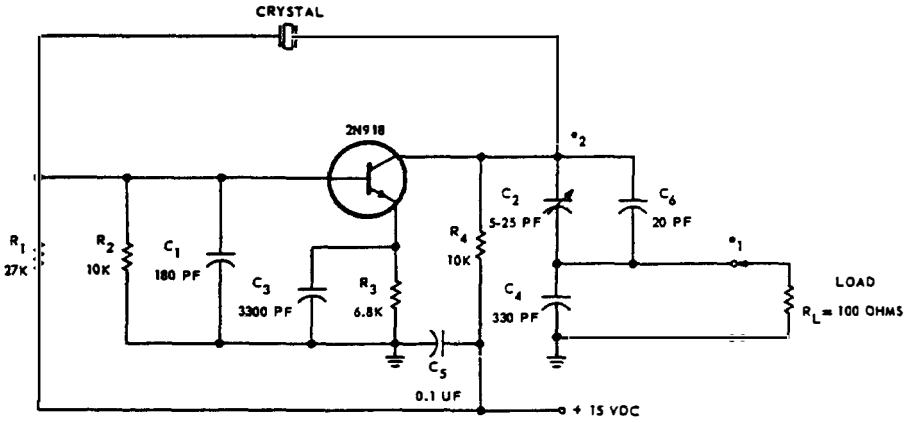

Figure 7-5. 10- to 30-MHz Pierce oscillator: schematic diagram.

NOTE 1. The output power can be increased by a factor of 3–5 by making several modifications. Change R_1 to 5.6 kΩ, R_3 to 10 kΩ, R_4 to 47 μH, C_1 to 220 pF, and R_L to 50 Ω. However, the frequency instability contribution of the oscillator circuitry is increased by roughly the same factor.

NOTE 2. Although the circuit will oscillate with any standard crystal in the 10- to 20-MHz range, some adjustment of C_2 is necessary over the frequency range to put crystals exactly on frequency.

7.2.6. Overtone Pierce Oscillator

The Pierce oscillator, as shown in Figure 7-2, cannot be used with overtone crystals. The circuit can oscillate with less gain on the fundamental frequency of the crystal than on an overtone. It is therefore necessary to provide some means of preventing the unwanted oscillation. If the collector capacitance is replaced by a tank circuit, this can be done conveniently. From equation (7-9) it can be seen that the reactances X_1 and X_2 must be of like sign for oscillation to take place. If the tank circuit is resonant between the fundamental and third overtone (or third and fifth overtones, if fifth-overtone crystals are to be used), oscillation of the unwanted modes will be prevented because the tank is inductive and has a positive sign. A capacitive reactance still appears at the desired frequency, however, and the desired oscillation can take place.

Equations (7-11) and (7-12) may be used to analyze the circuit provided the reactance of the tank circuit is substituted for X_2 in the equations. It can be shown that

$$X_2 = \frac{X_L}{1 - (f/f_r)^2},$$

where L and C_2 form the tank circuit, $X_L = 2\pi fL$, and $f_r = 1/2\pi\sqrt{LC_2}$. The effective output conductance of the transistor must be modified by adding the shunt conductance of the tank if it is not negligible. The tank conductance is given by $G_L = 1/QX_L$.

Above about 50 MHz, currently available transistors do not possess a sufficiently large y_{fe} to oscillate with 32-pF crystals and still maintain adequate reserve gain. If crystals are operated at a 20-pF load

capacitance, the upper range can be extended to about 75 MHz. The reason for this can be seen from equations (7-11) and (7-12): $X_e \doteq -(X_1 + X_2)$, and since X_e for a given load capacitance is decreasing as the frequency increases, X_1 and X_2 also must be made to decrease. The product $X_1 X_2$ for a given value of $(X_1 + X_2)$ is largest when $X_1 = X_2$ and is given by $X_e^2/4$.

The transconductance required for oscillation then is given by:

$$g_{fe} = \frac{4R_e}{X_e^2}$$

This increases as the square of the frequency. Unfortunately, the effective resistance of a crystal increases as the load capacitance is made smaller according to the relationship

$$R_e = R_1 \left(\frac{C_L + C_0}{C_L} \right)^2$$

and a C_L of 20 pF is about the limit for crystals having a C_0 of 4 pF. Thus, the use of a parallel resonant Pierce oscillator is not practical above about 75 MHz. The use of any parallel resonant oscillator above 30 MHz has a serious disadvantage in that standard crystals which are ground to be on frequency at series resonance cannot be used. The parallel resonant Pierce oscillator has a major advantage, however, in that it is practically impossible for free-running oscillations to take place. Series resonant oscillators have a potential to free-run through the C_0 of the crystal if not designed carefully. Figure 7-6 is an example of a Pierce oscillator which can be used with overtone crystals.

7.2.7. 25-MHz Pierce Oscillator

Typical performance characteristics for the 25-MHz Pierce oscillator shown in Figure 7-6 are given below.

a. Crystal: Fundamental or overtone.
b. Maximum resistance: 50 Ω.
c. Load capacitance: 32 pF.
d. Drive level: 2 mW.

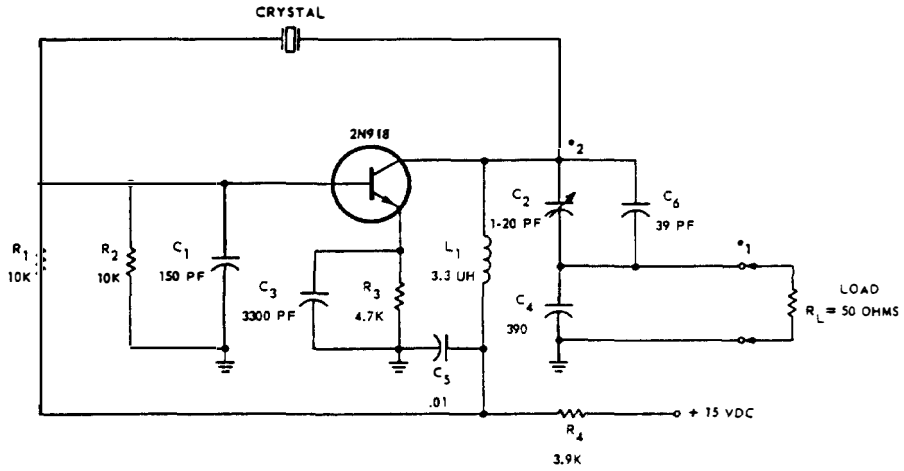

Figure 7-6. 25-MHz Pierce oscillator: schematic diagram.

e. Factors affecting frequency stability are as follows:
   1. Temperature coefficient of crystal: ±0.002 to ±0.005 percent from -55°C to +105°C, depending on crystal type.
   2. Aging rate of crystal: See section 5.7.
   3. Temperature stability of oscillator circuitry: 3 parts in 10^9/°C with third-overtone crystal.
   4. Voltage coefficient of oscillator: 2.3 parts in 10^7 for a 10-percent supply voltage change with overtone crystal.
f. Output: If $R_L = 50\ \Omega$, e_1 is approximately 0.1 V. The voltage e_2 is approximately 1.2 V. The output variation versus temperature is approximately ±6 percent from -55°C to +100°C.
g. Permissible load: $50 \leqslant R_L \leqslant \infty$.
h. Input power: 22 mW.

7.2.8. Impedance-Inverting Pierce Oscillator

The Pierce oscillator can be modified to use series resonant crystals. This is done by adding an inductor in series with the crystal to bring its frequency down to series resonance. Several advantages result from such a modification. First, standard, series resonant overtone crystals can be used. Also the reactances X_1 and X_2 can be made larger so that the transistor gain requirement is decreased. The power output also can be increased substantially.

The addition of a series inductor has several disadvantages, the most important of which is susceptibility to free running. If the inductor is relatively large, free-running oscillations may occur through the crystal C_0 instead of through the motional arm of the quartz. This is particularly true if the tank circuit is tuned so that the crystal frequency is being pulled high.

Free running can be alleviated if the crystal C_0 is resonated out by placing an inductor across it. It is then possible, however, for the oscillator to free-run below the crystal frequency through the C_0 compensating inductor. This sometimes occurs if the tank circuit is tuned so that the crystal frequency is being pulled low. Both of these free-running problems can be alleviated often by de-Q-ing the C_0 compensating inductor so that a circuit similar to that of Figure 7-8 (see section 7.2.10 below) results. Caution should be exercised here, since shunting the crystal with low impedances may increase the tendency of the oscillator to jump to a crystal spurious response.

Equations (7-11) and (7-12) may be used to analyze the series resonant Pierce oscillator if it is remembered that the quantity X_e includes both the reactance of the crystal and the inductor in series with it.

If a crystal switch with a significant amount of stray capacitance

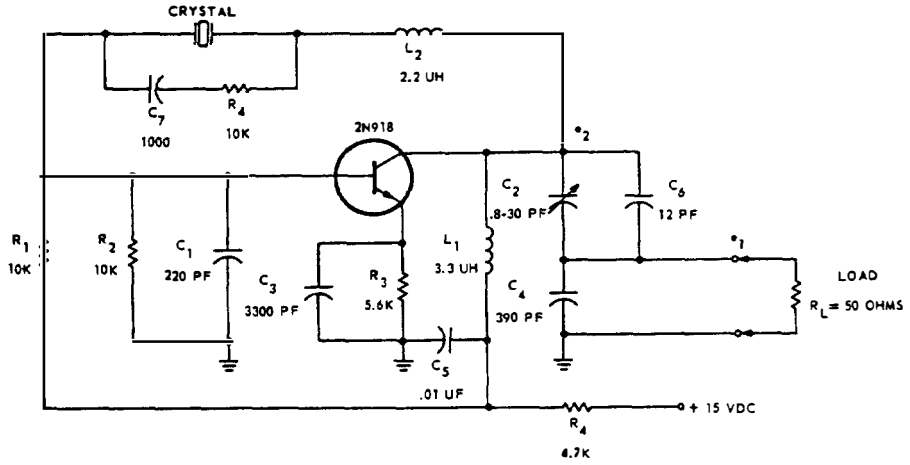

Figure 7-7. 25-MHz impedance-inverting Pierce oscillator: schematic diagram.

is to be used, it usually is better to locate the crystals and switch on the base side of the series inductor, as the circuit is less susceptible to stray capacitance on that side of the inductor.

In the design of VHF Pierce oscillators, excessive crystal drive is often a problem. This usually can be solved by decreasing the transistor emitter current until an acceptable drive level is obtained.

The Pierce oscillator family cannot be tuned for maximum output; they must be tuned for on-frequency operation. This may be a considerable disadvantage for field maintenance.

Figures 7-7, 7-8, and 7-9 are examples of impedance-inverting Pierce oscillators, and are included as a guide for designing such circuits.

7.2.9. 25-MHz Impedance-Inverting Pierce Oscillator

Typical performance characteristics for the 25-MHz impedance-inverting Pierce oscillator shown in Figure 7-7 are given below.

a. Crystal: Similar to CR-67/U.
b. Load capacitance: Series resonance.
c. Drive level: Nominally 2 mW.
d. Factors affecting frequency stability are as follows:
   1. Temperature coefficient of crystal: ±0.0025 percent.

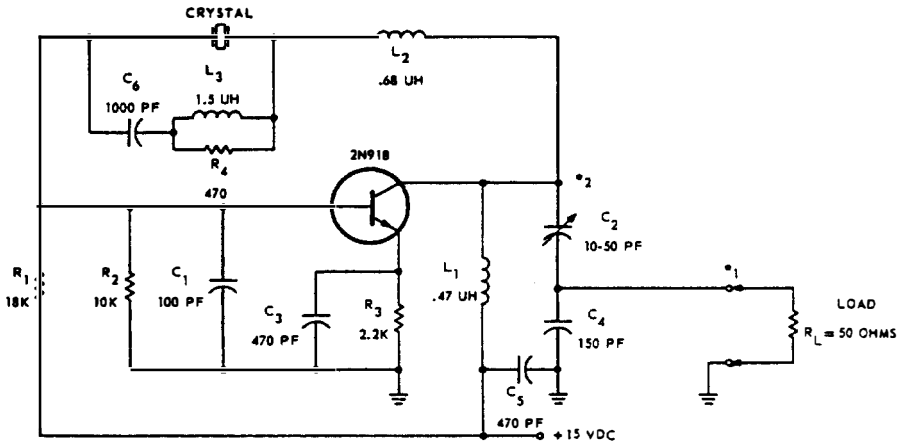

Figure 7-8. 50-MHz impedance-inverting Pierce oscillator: schematic diagram.

2. Aging rate of crystal: See section 5.7.
3. Temperature stability of oscillator circuitry: 1.6 parts in 10^8/°C.
4. Voltage coefficient of oscillator: 1 part in 10^7 for a 10-percent variation in supply voltage.

e. Output: If $R_L = 50\ \Omega$, e_1 is approximately 0.15 V. Distortion is about 2.5 percent. The voltage e_2 is on the order of 2.5 V. Output voltage variation over the temperature range from -55°C to +105°C is approximately ±8 percent.
f. Permissible load: $50 \leqslant R_L < \infty$.
g. Input power: 20 mW.

7.2.10. 50-MHz Impedance-Inverting Pierce Oscillator

Typical performance characteristics for the 50-MHz impedance-inverting Pierce oscillator shown in Fig 7-8 are given below.

a. Crystal: Similar to CR-84/U.
b. Load capacitance: Series resonance.
c. Drive level: 1 mW.
d. Factors affecting frequency stability are as follows:
   1. Temperature coefficient of crystal: ±0.002 percent from -55°C to +105°C.
   2. Aging rate of crystal: See section 5.7.
   3. Temperature stability of oscillator circuitry: 3 parts in 10^9/°C.
   4. Voltage coefficient of oscillator: 1.5 parts in 10^7 for a 10-percent supply voltage variation.
e. Output: For $R_L = 50\ \Omega$, e_i is approximately 0.3 V, and e_2 is on the order of 1.5 V. The output voltage change with temperature is approximately ±10 percent from -55°C to +100°C.
f. Permissible load: $50 \leqslant R_L \leqslant \infty$.
g. Input power: 40 mW.

7.2.11. 75-MHz Impedance-Inverting Pierce Oscillator

Typical performance characteristics for the 75-MHz impedance-inverting Pierce oscillator shown in Figure 7-9 are given below.

a. Crystal: Similar to CR-56/U.

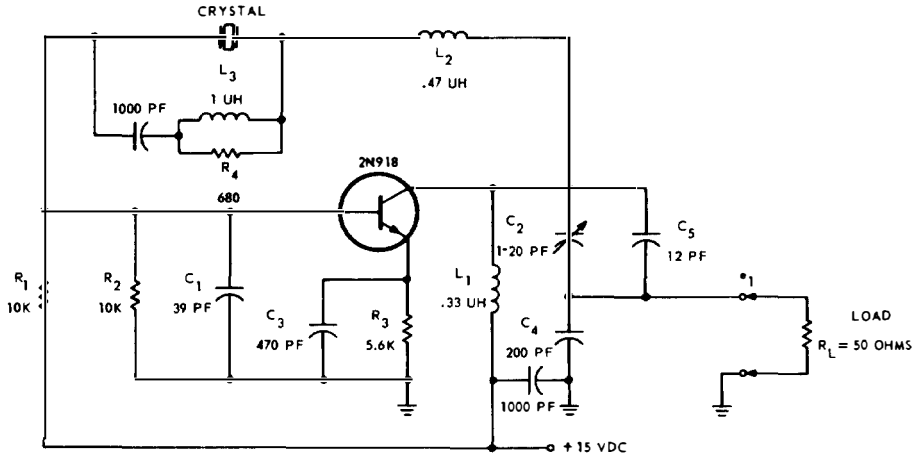

Figure 7-9. 75-MHz impedance-inverting Pierce oscillator: schematic diagram.

b. Load capacitance: Series resonance.
c. Drive level: Approximately 0.6 mW.
d. Factors affecting frequency stability are as follows:
   1. Temperature coefficient of crystal: ±0.005 percent from -55°C to +105°C.
   2. Aging rate of crystal: See section 5.7.
   3. Temperature stability of oscillator circuitry: 4.2 parts in 10^9/°C.
   4. Voltage coefficient of oscillator: 1 ppm for a 10-percent supply voltage variation.
e. Output: For R_L = 50 Ω, e_1 is approximately 0.05 V. The output voltage change with temperature is approximately ±15 percent from -55°C to +100°C.
f. Permissible load: $50 \leqslant R_L \leqslant \infty$.
g. Input power: 30 mW.

7.3. COLPITTS OSCILLATOR

The Colpitts oscillator is actually a Pierce oscillator with the collector rather than the emitter at ac ground. If appropriate allowances are made for strays, the Pierce oscillator equations can be used for this circuit also. It may be desirable, however, to look at the Colpitts

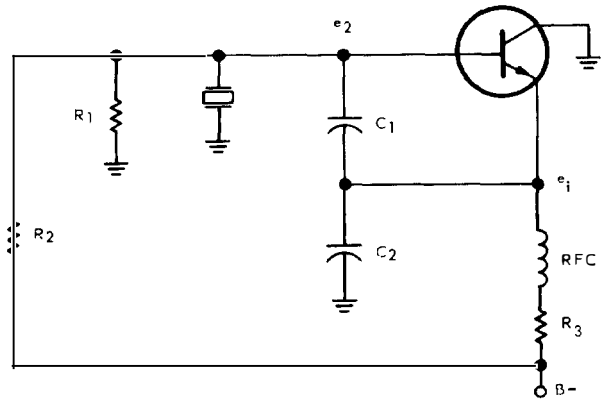

Figure 7-10. Colpitts crystal oscillator: schematic diagram.

circuit as a unique circuit analyzed in its own way. This gives a better feel for the quantities involved. (See Figure 7-10.) The Colpitts oscillator behaves quite differently from the Pierce oscillator in certain respects. The most important difference is in the biasing arrangement, which may present problems for the Colpitts circuit. The resistors R_1 and R_2 are not entirely negligible for low frequencies and may have several degrading effects. They may increase the effective resistance of the crystal branch of the circuit, thus reducing its Q in addition to decreasing the loop gain. They also may cause relaxation-type oscillations under certain conditions. Both of these problems can be reduced by using field effect transistors (FET). Temperature stability is somewhat worse with an FET, however.

The Colpitts oscillator can be thought of as an emitter-follower and a capacitive tapped tank circuit, as shown in Figure 7-11.

If capacitors C_1 and C_2 are large enough so that the input and output impedances of the transistor are effectively swamped, and if the crystal resistance R_e is small, then it can be shown (see Appendix F) that the step-up ratio of the tank circuit is

$$\frac{e_2}{e_1} \doteq \frac{X_1 + X_2}{X_2} \tag{7-28}$$

with voltages e_1 and e_2 in phase. (For this to be true, the crystal is

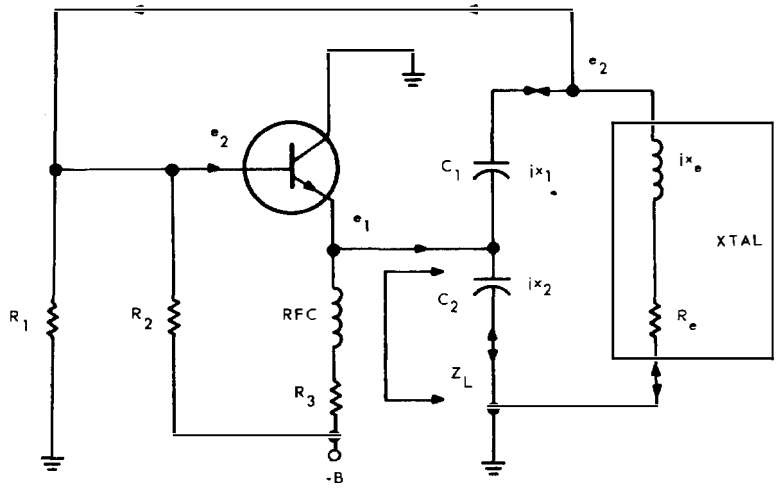

Figure 7-11. Colpitts oscillator: signal flow diagram.

resonant with the series combination of C_1 and C_2.) It also can be shown (see Appendix F) that the load seen by the emitter-follower is

$$Z_L \doteq \frac{X_2^2}{R_e} \tag{7-29}$$

and is purely resistive. The gain of the emitter-follower is

$$A = \left(\frac{e_1}{e_2}\right) = \frac{g_m Z_L}{1 + g_m Z_L}. \tag{7-30}$$

Since Z_L is resistive, the phase shift through the emitter-follower is zero, and the phase shift of the entire loop is zero. Oscillation then will take place if the loop gain exceeds unity. This is true if

$$\frac{e_2}{e_1} \; A \geqslant 1. \tag{7-31}$$

Substituting for A and e_2/e_1 gives

$$\left(\frac{g_m Z_L}{1 + g_m Z_L}\right)\left(\frac{X_1 + X_2}{X_2}\right) \geqslant 1 \tag{7-32}$$

Then substituting for Z_L gives

$$\left[\frac{g_m X_2^2/R_e}{1 + g_m X_2^2/R_e}\right]\left(\frac{X_1 + X_2}{X_2}\right) \geqslant 1. \tag{7-33}$$

But simplifying this gives

$$g_m X_1 X_2 \geqslant R_e, \tag{7-34}$$

which is the same equation obtained for the Pierce oscillator, as might be expected. Also, since the crystal must be resonant with the series combination of C_1 and C_2, the crystal reactance can be calculated using the equation $X_1 + X_2 + X_e = 0$, where X_e is the crystal reactance.

This analysis is quite limited by the assumptions made. When any one of them is not satisfied, equations (7-11) and (7-12) developed for the Pierce oscillator may be used. Here again the linear analysis gives no information concerning output voltage or crystal drive.

In some cases, the Y-parameters of the transistor may not be known or, for other reasons, the reader may elect to use an experimental approach to designing a Colpitts oscillator. For such an approach, the following guidelines may be used: In general, C_1 and C_2 should be as large as possible but still allow the circuit to oscillate with two to three times the maximum permissible crystal resistance.* If this results in the crystal reactance X_e being smaller than that of the specified load capacity, a trimmer capacitor may be placed in series with the crystal to trim the crystal onto frequency. As in the Pierce oscillator, it is desirable to let $|X_2| \ll 1/g_{oe}$ and $|X_1| \ll 1/g_{ie}$. This minimizes the effect of transistor input and output conductances on the circuit. Best stability also occurs if C_1 and C_2 are as large as possible because they swamp out any change in the transistor capacitances. Still another effect makes it desirable to make C_1 and C_2 as large as possible in the Colpitts oscillator. Referring to Figure 7-10, it can be seen that the reactance of the crystal (or the resultant reactance of the crystal and a series trimmer) will be smaller

*This can be determined by adding resistance in series with the crystal until oscillation will not occur.

if C_1 and C_2 are large, thus minimizing the shunt effects of R_1 and R_2.

The large-signal analysis presented for the Pierce oscillator in section 7.2.2 can also be applied to the Colpitts oscillator by recognizing that if the ac ground point were moved from the collector to the emitter, the circuits would be basically the same.

Again, as in the case of the linear analysis, additional insight may be obtained from an analysis based on the Colpitts configuration itself. Such an analysis has been made in Appendix I, based on the principle of harmonic balance. This analysis also shows an effect of amplitude on the frequency of oscillation. The analysis is made using the circuit of Figure 7-12. Here the crystal is replaced by an equivalent resistance and inductance. While this substitution would not be valid for a transient analysis or an analysis based on the variation of parameters, it is nevertheless satisfactory using the principle of harmonic balance, even though differential equations are used initially. The justification for this rests on the argument that the principle of harmonic balance is a steady-state solution, and replacing the crystal reactance by its series capacitance–inductance combination would only result in a slower buildup of oscillation. One might wonder if the resultant additional filtering afforded by the series *LC* combination would affect the result, since harmonics could beat together to produce a fundamental component. It should be observed, however, that even with the equivalent circuit shown, the impedance of the resonant circuit is so low at the harmonic frequencies that these components have a negligible effect on the amplitude of oscillation.

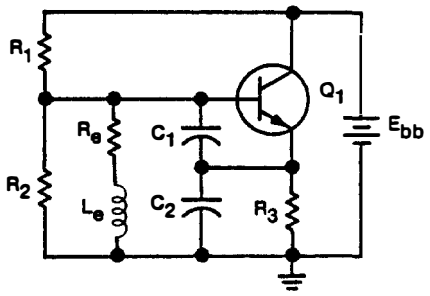

Figure 7-12. Colpitts oscillator circuit.

In the analysis, it is assumed that the biasing resistors R_1, R_2, and R_3 have a negligible effect on the ac performance. It will be found in general that the nonlinear analyses become formidable when even a few effects are considered, and therefore it is impossible to consider all the effects simultaneously. The general approach is to consider only one or two effects in a given analysis to determine how these parameters influence behavior. Other analyses are then made to determine how some of the neglected effects modify the behavior. For this analysis, it is assumed that the transistor reactances and its output impedance are negligible.

From equation (I-36) in Appendix I, we see that the amplitude of oscillation is determined by the expression:

$$X_1 X_2 g_m = R_e - \frac{X_1(X_e + X_2)}{R_{\text{in}}} \tag{7-35}$$

where $X_1 = -1/\omega C_1$, $X_2 = -1/\omega C_2$, X_e is the crystal equivalent reactance, and g_m and R_{in} are the equivalent transconductance and input resistance at the final stabilized amplitude. The relationship between the small-signal values and the large-signal equivalent values is consistent with the nonlinear analysis discussed in section 6.4, and the ratios g_m/g_{m0} and $R_{\text{in}}/R_{\text{in0}}$ may be read from the graph of Figure 6-6. As a first approximation, the last term of equation (7-35) may be neglected and the required value of g_m determined. Then from transistor data or by using the approximation $g_{m0} = qI_e/KT = 0.04I_e$, where I_e is in milliamperes, we find the ratio g_m/g_{m0}. Then using Figure 6-6, a value of V can be determined. This value can be used to read the ratio $R_{\text{in}}/R_{\text{in0}}$. The value of R_{in} can then be calculated.

The analysis of Appendix I, equation (I-28), also shows that the frequency of oscillation must satisfy the expression:

$$X_e + X_1\left(1 + \frac{R_e}{R_{\text{in}}}\right) + X_2 = 0 \tag{7-36}$$

where R_{in} is the equivalent input resistance at the final amplitude as defined above. From this equation, the crystal reactance X_e can be calculated (or if it is fixed, the values of X_1 and X_2 to obtain X_e can be found). The values of X_1, X_2, X_e, and R_{in} can then be substituted in equation (7-35) to obtain a corrected value of g_m if required.

The value of V can also be used to find the actual voltage across C_1, which is

$$V_1(\text{peak ac}) = \frac{VKT}{q} \doteq 26 \text{ mV times } V.$$

Since the circulating current in the tank circuit, consisting of R_e, L_e, C_1, and C_2, is normally large compared to the base current, the ac voltage across C_2 is given by

$$V_2 = \frac{V_1 C_1}{C_2}.$$

The bias shift due to oscillation from equation (6-23) is given by

$$V_{\text{bias}} = \frac{KT}{q} \ln I_0(V)$$

and may be read from the graph of Figure 6-7.

Several typical examples of Colpitts crystal oscillators are given in Figures 7-13 and 7-14. They are included as guidelines for designing circuits of this type. For these circuits, the output was taken from the emitter through a capacitive divider. It may be convenient to take the output from another point in the circuit if a larger voltage is required and a high-impedance load exists.

7.3.1. 3- to 10-MHz Colpitts Oscillator *

Typical performance characteristics for the 3- to 10-MHz Colpitts oscillator shown in Figure 7-13 are given below.

a. Crystal: CR-18/U or similar.
b. Load capacitance: 32 pF.
c. Drive level: 2–10 mW, depending on the frequency and crystal resistance.
d. Factors affecting frequency stability are as follows:
   1. Temperature coefficient of crystal: ±0.005 percent from −55°C to +105°C.
   2. Aging rate of crystal: See section 5.7.
   3. Temperature stability of oscillator circuitry: 4.4 parts in 10^8/°C at 10 MHz and 6.3 parts in 10^8/°C at 3 MHz.

*See footnote p. 66.

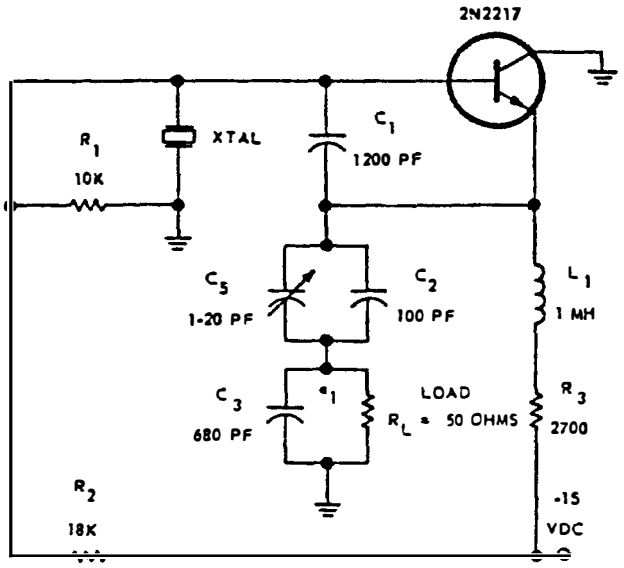

Figure 7-13. 3- to 10-MHz Colpitts oscillator: schematic diagram.

4. Voltage coefficient of oscillator: 1.3 parts in 10^7 at 3 MHz, 3 parts in 10^7 at 5 MHz, and 6 parts in 10^7 at 10 MHz for a 10-percent supply voltage variation.

e. Output: If R_L = 50 Ω, e_1 is approximately 0.05 V at 10 MHz and 0.25 V at 3 MHz, depending on the crystal resistance. Distortion is about 7 percent at 10 MHz and 17 percent at 3 MHz.

f. Permissible load: $50 \leqslant R_L \leqslant \infty$.

g. Power input: 55 mW.

NOTE. Although the circuit will oscillate with any standard crystal in the 3- to 10-MHz range, some adjustment of C_5 is necessary over the frequency range to put crystals exactly on frequency.

7.3.2. 10- to 20-MHz Colpitts Oscillator

Typical performance characteristics for the 10- to 20-MHz Colpitts oscillator shown in Figure 7-14 are given below.

a. Crystal: CR-18/U, CR-66/U, or similar.

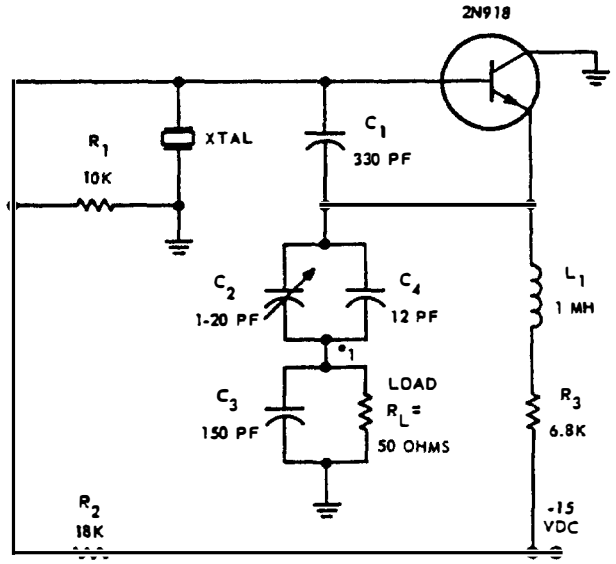

Figure 7-14. 10- to 20-MHz Colpitts oscillator: schematic diagram.

b. Load capacitance: 32 or 30 pF, respectively.
c. Drive level: 1–2 mW, depending on frequency and crystal resistance.
d. Factors affecting frequency stability are as follows:
   1. Temperature coefficient of crystal: ±0.005 percent from −55°C to +105°C for CR-18/U or ±0.002 percent from −55°C to +105°C for the CR-66/U.
   2. Aging rate of crystal: See section 5.7.
   3. Temperature stability of oscillator circuitry: 4.4 parts in 10^8/°C at 10 MHz and 1.8 parts in 10^8/°C at 20 MHz.
   4. Voltage coefficient of oscillator: Approximately 1.5 parts in 10^7 for a 10-percent change in supply voltage.
e. Output: For $R_L = 50\ \Omega$, $e_1 = 0.15$–0.20 V, depending on frequency and crystal resistance.
f. Permissible load: $50 \leqslant R_L \leqslant \infty$.
g. Input power: 26 mW.

NOTE. Although the circuit will oscillate with any standard crystal in the 10- to 20-MHz range, some adjustment of C_2 is necessary over the frequency range to put crystals exactly on frequency.

7.4. CLAPP OSCILLATOR

The Clapp oscillator is actually a Pierce oscillator with the base rather than the emitter at ac ground. If appropriate allowances are made for strays, then the Pierce oscillator equations can be used for this circuit. It may be desirable, however, to look at the Clapp oscillator as a unique circuit analyzed in its own way. This gives a better feel for the quantities involved. The most important disadvantage of the Clapp oscillator is that free-running oscillations may occur through the RF choke if resistor R_4 is too small. (See Figure 7-15.) If a fairly high supply voltage is available, R_4 can be made so large that the choke is not needed.

The Clapp oscillator can be thought of as a grounded-base amplifier stage loaded with a tank circuit. The tank has a capacitive tap from which energy is fed back to the emitter. Refer to Figure 7-16 for a signal diagram.

If we assume that the emitter base capacitance is included in C_1, that the collector-to-emitter capacitance is included in C_2, and that $R_e \ll X_e$, then the circuit can be analyzed as follows. It is assumed that the input impedance of the common-base amplifier is $1/g_m$, where g_m is the transconductance of the transistor. Also the gain of the stage

$$\frac{e_1}{e_2} = A \doteq g_m Z_L$$

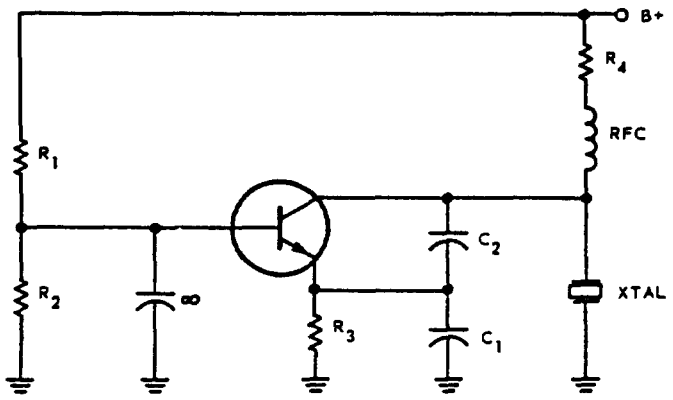

Figure 7-15. Clapp crystal oscillator: schematic diagram.

where Z_L is the collector load impedance. The voltage ratio of the tapped tank circuit is given approximately (see Appendix D) by

$$\frac{e_2}{e_1} = \frac{X_1}{X_1 + X_2}. \tag{7-38}$$

The phase angle between the voltages is very small; for practical purposes, the voltages e_1 and e_2 are in phase. The phase shift through the amplifier is determined by the phase angle of Z_L. It can be shown (see Appendix D) that Z_L, the impedance presented to the collector by the tank when the capacitive tap is loaded by the transistor input impedance $1/g_m$, is given by

$$Z_L \doteq \frac{(X_1 + X_2)^2}{R_e + g_m X_1^2} \tag{7-39}$$

This expression is derived under the condition that $X_1 + X_2 + X_e = 0$. Here, again, the phase angle is very small and, for this discussion, will be neglected. With a resistive load, then, the phase shift through the amplifier is zero; therefore, the phase shift through the entire loop is zero, fulfilling the phase shift requirements. The gain requirement is that the quantity $(e_2/e_1)A \geqslant 1$. The gain of the transistor is

$$A = g_m Z_L = \frac{g_m (X_1 + X_2)^2}{R_e + g_m X_1^2} \tag{7-40}$$

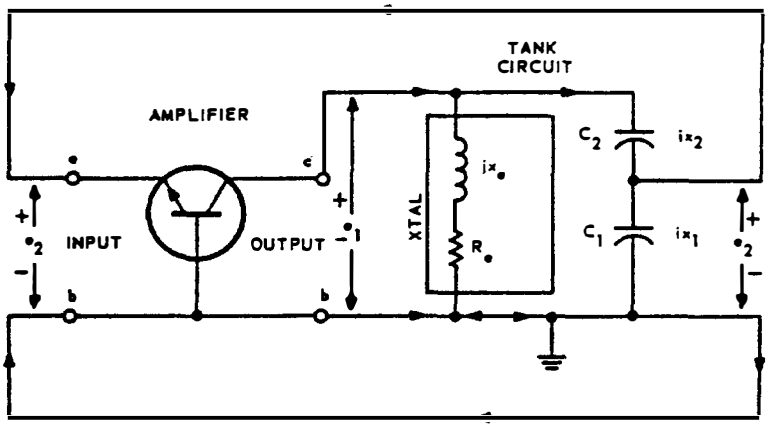

Figure 7-16. Clapp crystal oscillator: signal flow diagram.

and

$$\frac{e_2}{e_1} = \frac{X_1}{X_1 + X_2}.$$

Substituting these,

$$\left(\frac{X_1}{X_1 + X_2} \right) \left[\frac{g_m (X_1 + X_2)^2}{R_e + g_m X_1^2} \right] \geqslant 1. \qquad (7\text{-}41)$$

This fortunately simplifies to the equation derived for the Pierce oscillator: $g_m X_1 X_2 \geqslant R_e$. Also, it has been shown that the phase shift requirements will be fulfilled if $X_1 + X_2 + X_e = 0$.

This analysis is quite limited by the assumptions made. When any one of them is not satisfied, equations (7-11) and (7-12) developed for the Pierce oscillator may be used.

Here again the linear analysis gives no information concerning output voltage or crystal drive. Also, in some cases the Y-parameters of the transistor may not be known, and experimental design techniques must be used.

In general, C_1 and C_2 should be as large as possible but still allow the circuit to oscillate with two to three times the maximum permissible crystal resistance.* If this results in the crystal reactance X_e being smaller than that required for the specified load capacitance, a trimmer capacitor may be placed in series with the crystal. Whether or not a series capacitor is used, it may be desirable to provide some variable reactive element to trim the crystal onto frequency.

It should be noted that when C_1 and C_2 are large, the sum $X_1 + X_2$ is small, making the RF choke in series with R_4 unnecessary under some conditions.

A load can be connected to the Clapp oscillator in any one of several places. Maximum voltage can be obtained on the collector. Any impedance connected to this point must be high. A lower impedance and moderate voltages can be found at the emitter. A very low impedance output can be obtained by inserting a capacitor equal to approximately five times the value of C_1 between C_1 and

*This can be determined by adding resistance in series with the crystal until oscillation will not occur.

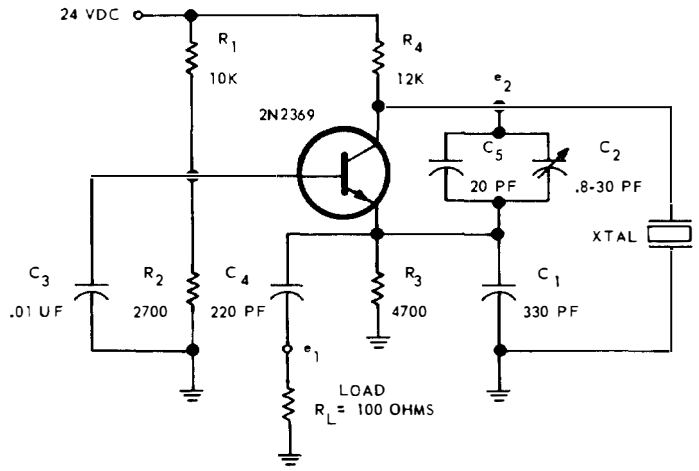

Figure 7-17. 3- to 20-MHz Clapp oscillator: schematic diagram.

ground. The output then is taken from the connection of C_1 and the added capacitor.

The schematic diagram of a practical Clapp oscillator is given in Figure 7-17.*

7.4.1. 3- to 20-MHz Clapp Oscillator Circuit

a. Crystal: CR-18/U, CR-66/U, or similar.
b. Load capacitance: 32 or 30 pF, respectively.
c. Crystal drive level: 1–5 mW, depending on frequency and crystal resistance.
d. Factors affecting frequency stability are as follows:
   1. Temperature coefficient of crystal: ±0.005 percent from −55°C to +105°C for CR-18/U or ±0.002 percent from −55°C to +105°C for CR-66/U.
   2. Aging rate of crystal: 5 parts in 10^6/month to several parts in 10^8/month, depending on crystal. See section 5.7.
   3. Temperature coefficient of oscillator: 3 parts in 10^8/°C at 3 MHz, 7 parts in 10^9 at 5 MHz, and 2.4 parts in 10^8 at 20 MHz.
   4. Voltage coefficient: 2 parts in 10^6 at 3 MHz, 9 parts in 10^7

*See footnote p. 66.

at 5 MHz, 4 parts in 10^7 at 10 MHz, and 6 parts in 10^7 at 20 MHz for a 10-percent change in supply voltage.

e. Output conditions: With $R_L = 100\ \Omega$, $e_1 \doteq 0.15$–0.3 V, depending on frequency and crystal resistance. Distortion (at 5 MHz) = 15 percent. The output may be taken from the collector with a very high-impedance load. Voltage $e_2 \doteq 3$–7 V, depending on frequency and crystal resistance. The output change over the temperature range from −55°C to +100°C is approximately 5 percent.
f. Permissible load: $100 \leqslant R_L < \infty$.
g. Input power: 65 mW.

NOTE 1. The oscillator can be operated from a 15-V supply if several changes are made. The resistor R_4 is decreased to 5.6 kΩ, and a 500-μH choke is added in series with it. The choke is necessary to prevent unduly loading the collector circuit. The resistor in series with the choke is necessary to prevent the oscillator from free-running through the choke instead of oscillating through the crystal. The emitter resistor R_e is reduced to 2.7 kΩ.

NOTE 2. Although the circuit will oscillate with any standard crystal in the 3- to 20-MHz range, some adjustment of C_2 is necessary over the frequency range to put crystals exactly on frequency.

7.5. GROUNDED-BASE OSCILLATOR

The basic circuit of the grounded-base crystal oscillator is shown in Figure 7-18.

This circuit can be used from several megahertz to above 150 MHz. It is most commonly used in the range from 20 to 100 MHz. The circuit is capable of delivering high output power, has medium frequency stability, and is about average in difficulty to design. It is basically a zero phase shift oscillator. This makes it undesirable for use with a complicated crystal switch in the region above 75 MHz where lagging phase shift problems become severe.

Basically, the grounded-base oscillator circuit works as follows: The voltage on the emitter of the transistor is amplified and appears

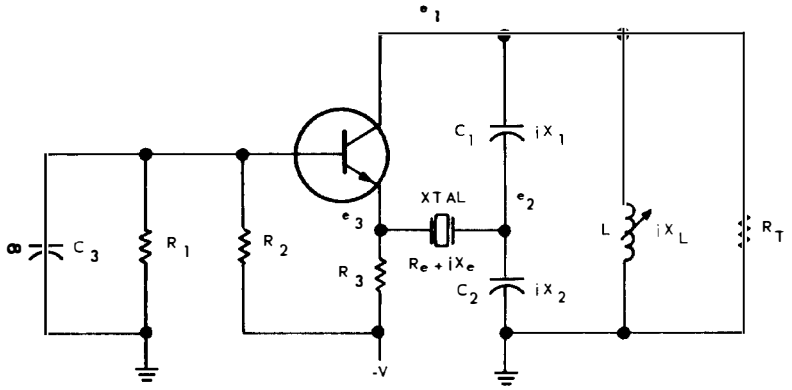

Figure 7-18. Grounded-base oscillator: schematic diagram.

on the collector as

$$e_1 = e_3 y_{fb} Z_t \tag{7-42}$$

where Z_t is the impedance presented to the collector by the tank. For most oscillators, the tank is tuned to resonance and thus appears resistive. The voltage e_1 then lags e_3 by the angle of the forward transfer admittance of the transistor, which at lower frequencies is small.

A small amount of phase shift also is caused by the capacitive tap on the tank circuit. This is a leading phase shift, however, and tends to compensate for the phase lag in the transistor. If the capacitor C_2 is fairly large, this phase shift is negligible and the voltage on the tap is given approximately by

$$e_2 = e_1 \left(\frac{C_1}{C_1 + C_2}\right) = -e_1 \left(\frac{X_2}{X_L}\right). \tag{7-43}$$

The grounded-base input impedance of the transistor normally is somewhat inductive so that leading phase shift also occurs between the tap on the tank e_2 and the emitter. The emitter voltage e_3 is related to e_2 by the expression

$$e_3 = \left(\frac{e_2}{1 + Z_e y_{ib}}\right) \tag{7-44}$$

where Z_e is the crystal impedance and y_{ib} is the transistor input

admittance. If the crystal is at series resonance, and if the transistor input admittance is only slightly inductive, then the expression simplifies to

$$e_3 \doteq e_2 \left(\frac{R_{in}}{R_{in} + R_e} \right) \tag{7-45}$$

where R_{in} is the input resistance of the transistor and R_e is the crystal resistance. The phase shift that does occur tends to compensate for the phase lag in the transistor. For oscillation to take place, all three of the phase shifts must add up to zero, and the loop gain must equal or exceed unity.

The equations which must be satisfied for these conditions to occur are derived in Appendix C and are presented here as equations (7-46) and (7-47).

$$g_{fb} = \frac{1}{R_T}\left(\frac{X_L}{X_2}\right)\left[\frac{R_e + R_{in}}{R_{in}}\right] + \frac{1}{R_{in}}\left(\frac{X_2}{X_L}\right) + b_{ib}\left(\frac{X_1}{R_T}\right) - b_{ib}\left(\frac{X_L}{X_2}\right)\left(\frac{X_e}{R_T}\right) \tag{7-46}$$

$$X_e = b_{fb} R_T R_{in}\left(\frac{X_2}{X_L}\right) + X_1\left(\frac{X_2}{X_L}\right) - b_{ib} R_{in}\left[R_e + R_T\left(\frac{X_2}{X_L}\right)^2\right] \tag{7-47}$$

where $X_1 = -1/\omega C_1$, $X_2 = -1/\omega C_2$, $X_L = \omega L$, $R_{in} = 1/g_{ib}$, and R_T is the total resistance shunting the tank circuit ($R_T \doteq R_L$). (For definitions of the g and b transistor parameters, refer to Chapter 6.

In deriving these equations, the following assumptions were made:

a. The reverse transfer admittance of the transistor, y_{rb}, is negligible.
b. The transistor output admittance, y_{ob}, is either negligible or lumped in with R_T and L.
c. The tank components $X_1 + X_2 + X_L = 0$. (This is approximately resonance.)

Even with these assumptions, the equations appear formidable but are nevertheless quite useful. If equation (7-46) is minimized for

transistor gain, it will be found that minimum g_{fb} is required when

$$\frac{X_L}{X_2} = -\left(\frac{R_T}{R_e + R_{in}}\right)^{1/2}. \tag{7-48}$$

This assumes that the crystal is operated at series resonance, $X_e = 0$. The minimum g_{fb} is then given by

$$g_{fb(min)} = -\frac{2}{R_{in}}\left(\frac{R_e + R_{in}}{R_T}\right)^{1/2} + b_{ib}\left(\frac{X_1}{R_T}\right). \tag{7-49}$$

For a first approximation, it may be desirable to neglect the reactive component b_{ib} of the transistor input impedance in the gain equation so that

$$g_{fb(min)} \doteq -\frac{2}{R_{in}}\left(\frac{R_e + R_{in}}{R_T}\right)^{1/2}. \tag{7-50}$$

If

$$\left(\frac{b_{ib}}{g_{fb}}\right)\left(\frac{X_1}{R_T}\right) \ll 1 \tag{7-51}$$

then the error introduced by this assumption is negligible, as is often the case.

If we require the crystal to operate at series resonance ($X_e = 0$), then we can design the oscillator circuit as follows by the manipulation of equations (7-47), (7-48), and (7-50).

Step 1. Calculate R_T using g_{fb} approximately one-third the actual g_{fb} of the transistor. This gives a loop gain of 3 to ensure saturation:

$$R_T = \frac{4(R_e + R_{in})}{(R_{in}\, g_{fb})^2}. \tag{7-52}$$

Step 2. Calculate (X_L/X_2) using the equation,

$$\frac{X_L}{X_2} = -\left(\frac{R_T}{R_e + R_{in}}\right)^{1/2}. \tag{7-53}$$

Note that

$$\frac{C_2}{C_1} = -\left(\frac{X_L}{X_2} + 1\right).$$

Step 3. Calculate X_1 (using b_{fb} approximately one-third the actual b_{fb} if one-third the actual g_{fb} was used in step 1):

$$X_1 = \frac{b_{ib}}{g_{ib}}\left[R_e\left(\frac{X_L}{X_2}\right) + R_T\left(\frac{X_2}{X_L}\right)\right] - \frac{b_{fb}}{g_{ib}}R_T. \tag{7-54}$$

This equation must be used with judgment. If $g_{fb} < b_{fb}$ and R_T is fairly large, the calculated value of X_1 will be very large (small C_1). This results because of the assumption $X_1 + X_2 + X_L = 0$. If the transistor phase lag is large, it may require that a considerable phase shift be obtained in C_2. This causes the tank to look capacitive if $X_1 + X_2 + X_L = 0$, producing even more lagging phase shift and requiring C_1 to be extremely small. It may be better to keep C_1 a little larger and tune the tank to actual resonance (so that Z_T is real).

At low frequencies, the calculated value of X_1 may come out very small (C_1 extremely large) or negative. This results it the phase shift at the transistor input is sufficient to cancel the phase lag through the transistor so that no phase shift is required from the capacitive tap. If this occurs, it may be better to let

$$X_1 = \frac{R_e + R_{in}}{\text{approximately 5 or 10}}\left[\frac{X_L}{X_2} + 1\right] \tag{7-55}$$

and tune the tank slightly capacitive.

Step 4. Calculate X_2 by

$$X_2 = -\frac{X_1}{(X_L/X_2) + 1}. \tag{7-56}$$

Step 5. Calculate X_L by

$$X_L = -(X_1 + X_2). \tag{7-57}$$

If the parameters of the transistor are accurately known, then the application of equations (7-52) to (7-57) may lead to values for C_1, C_2, L, and R_T close to the final values in the optimized circuit. Since the equations assume linearity, they give no information concerning crystal drive level or output power. They predict starting conditions only. The power gain approach described in Chapter 3 may be useful when designing a grounded-base oscillator. If it is used, the transformation ratio $R_{fb}/(R_{in} + R_e)$, should be set equal to the transforma-

tion ratio of the tank circuit which is given by $[(C_1 + C_2)/C_1]^2$. This can be solved for the ratio

$$\frac{C_2}{C_1} = \left(\frac{R_{fb}}{R_{in} + R_e}\right)^{1/2} - 1. \tag{7-58}$$

Regardless of which design approach is used, it will be necessary in general to optimize the circuit experimentally. Therefore, a general discussion for the experimental approach is given here.

Basically, there are three considerations which must be kept in mind in designing a grounded-base oscillator. First, the impedance transformation $[(C_2/C_1) + 1]^2$, should be approximately equal to the ratio $R_T/(R_{in} + R_e)$ for optimum gain conditions. R_{in} is the input resistance of the transistor and is generally quite low (in the range from 20 to 100 Ω). R_e is the crystal resistance and in the VHF range usually falls between 20 and 60 Ω. R_T is the collector load resulting from the load resistor and the tank circuit. If high output is required, it is desirable to make the ratio C_2/C_1 fairly large. This reduces the crystal dissipation for a given output voltage. It also reduces the stability; therefore, if the additional output power is not required and crystal dissipation is excessive, the emitter current should be reduced. If the emitter current is high and the ratio of C_2/C_1 is very large, outputs in excess of 50 mW can be obtained. However, outputs below 5 mW are more common for stable oscillators.

The second consideration in designing a grounded-base oscillator is the adjustment of C_1 and C_2. They should be adjusted so that the crystal is on frequency when the tank is tuned for maximum output (resonance). If there is too much phase lag in the transistor, the crystal will operate below series resonance. This usually can be corrected by decreasing C_1 and C_2 (the ratio C_2/C_1 may remain unchanged). The amount of phase shift that can be compensated for in this manner is somewhat limited. For this reason, the grounded-base oscillator is not desirable for use with complicated crystal switches above about 75 MHz. On occasions it may be desirable to insert a capacitor in series with the crystal to get the frequency up to series resonance.

A third consideration in designing a grounded-base oscillator is preventing unwanted oscillations. They may occur simultaneously with the crystal oscillation or they may be sufficiently severe to kill the crystal-controlled oscillation altogether. There are generally two types of free-running oscillation which may occur in the grounded-

base oscillator. The first is oscillation through the shunt capacitance C_0 of the crystal rather than through the motional arm of the crystal. This usually can be prevented by resonating out C_0 by the addition of an inductor across the crystal, as shown in Figure 7-20 (see section 7.5.2 below). A second source of instability is the internal feedback of the transistor, which may cause parasitic oscillations. (Refer to Chapter 6.) These oscillations usually can be detected by a jump in the output voltage as the oscillator is tuned. The best remedy for such oscillations is to use a fairly small resistance value for R_T. Only if the actual load is resistive over a wide frequency range can resistor R_T be eliminated. The importance of using some real resistance to load the tank for stabilization cannot be overemphasized. In some cases, it may be desirable to load the emitter for stabilization also, as is done on the oscillator of Figure 7-19.

Some transistors have a considerably greater tendency than others to develop parasitic oscillations. Therefore, if the problem persists, it may be advantageous to try several other transistor types.

The grounded-base oscillator is sometimes used with an inductive tap rather than a capacitive tap for low-frequency crystals. This may make it easier to get the crystal down to its series resonant frequency. Adding a capacitor from emitter to ground also may be helpful in accomplishing this. Generally, the inductive tap should not be used above 30 MHz because it aggravates the lagging phase shift problem.

Several practical grounded-base oscillator circuits are presented in Figures 7-19 through 7-22.*

7.5.1. 25-MHz Grounded-Base Oscillator

L = 0.65–1.5 μH, 14 turns of #28 wire close-wound on 0.211-inch-o.d. coil form. Slug: Carbonyl W, $\frac{3}{8}$ inch long.

C_1 has a negative temperature coefficient of 200 ppm/°C to compensate for temperature changes in the oscillator circuitry.

a. Crystal: Similar to CR-67/U.
b. Load capacitance: Series resonance.
c. Drive level: Nominally 2 mW.
d. Factors affecting frequency stability are as follows:
   1. Temperature coefficient of crystal: ±0.0025 percent from −55°C to +105°C.

*See footnote p. 66.

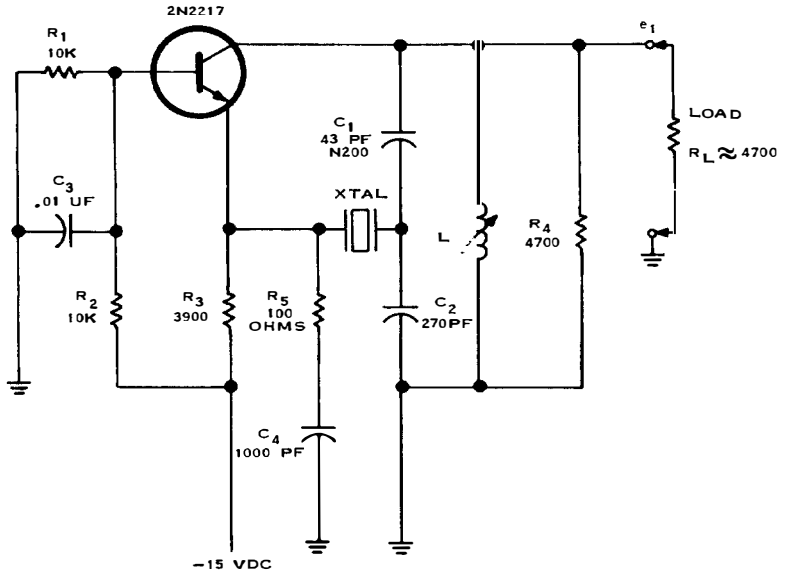

Figure 7-19. 25-MHz grounded-base oscillator: schematic diagram.

2. Aging rate of crystal: ±0.0005 percent/month to several parts in 10^8/month, depending on crystal. See section 5.7.
3. Temperature coefficient of oscillator circuitry: 1 part in 10^8/°C.
4. Voltage coefficient of oscillator: 7 parts in 10^7 for a 10-percent change in supply voltage.

e. Permissible load: 4.7 kΩ $\leqslant R_L < \infty$.

f. Output: e_1 is approximately 2 V for R_L = 4.7 kΩ. Change in output with temperature is approximately 3 percent from -55°C to +100°C. A low impedance output may be obtained by using a capacitive divider in place of C_2.

NOTE. R_4 is used for stabilization and should not be included in the load.

g. Power input: 40 mW.

7.5.2. 50-MHz Grounded-Base Oscillator

L_1 = 0.92–2.1 μH, 15 turns #28 wire close-wound on 0.211-inch-o.d. coil form. Slug: Carbonyl W, $\frac{3}{8}$ inch long.

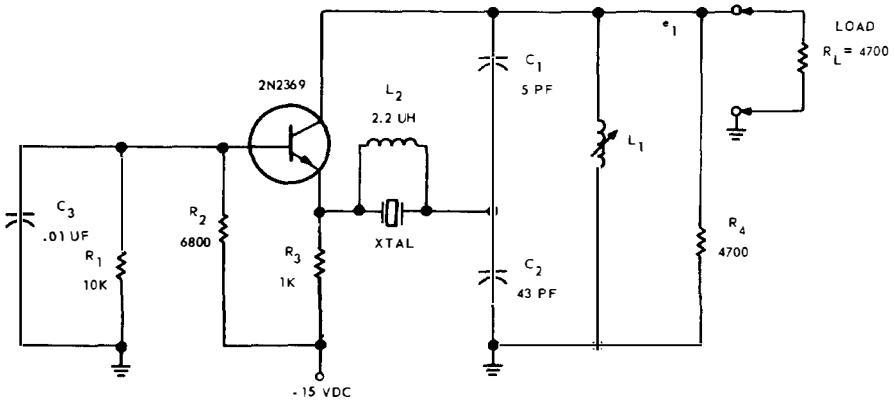

Figure 7-20. 50-MHz grounded-base oscillator: schematic diagram.

a. Crystal: Similar to CR-67/U.
b. Load capacitance: Series resonance.
c. Drive level: Nominally 2 mW.
d. Factors affecting frequency stability are as follows:
   1. Temperature coefficient of crystal: ±0.0025 percent from -55°C to +105°C.
   2. Aging rate of crystal: See section 5.7.
   3. Temperature coefficient of oscillator circuitry: 1 part in 10^8/°C.
   4. Voltage coefficient of oscillator: 3 parts in 10^7 for a 10-percent change in supply voltage.
e. Permissible load: 4.7 kΩ $\leqslant R_L < \infty$.
f. Output: e_1 is approximately 7 V for a load of 4.7 kΩ. Change in output with temperature is approximately 5 percent from -55°C to +100°C. A low impedance output may be obtained by using a capacitive divider in place of C_2. Distortion is approximately 5 percent.

NOTE. R_4 is used for stabilization and should not be included in the load.

g. Power input: 85 mW.

NOTE. L_2 is chosen to be antiresonant with the C_0 of the crystal and any stray capacitance in parallel with it.

7.5.3. 75-MHz Grounded-Base Oscillator

L_1 = 0.27–0.52 μH, 7 turns #28 wire close-wound on 0.211-inch-o.d. coil form. Slug: Carbonyl E, $\frac{5}{16}$ inch long.

L_2 = This inductance is chosen to be antiresonant with the C_0 of the crystal and any stray capacity in parallel with it.

a. Crystal: Similar to CR-56A/U.
b. Load capacitance: Series resonance.
c. Drive level: Approximately 0.5 mW.
d. Factors affecting frequency stability are as follows:
   1. Temperature coefficient of crystal: ±0.005 percent from -55°C to +105°C.
   2. Aging rate of crystal: See section 5.7.
   3. Temperature coefficient of oscillator circuitry: 1 part in 10^8/°C.
   4. Voltage coefficient of oscillator: 8 parts in 10^7 for a 10-percent change in supply voltage.
e. Permissible load: 3.3 kΩ $\leqslant R_L \leqslant \infty$.
f. Output: e_1 is approximately 2 volts for a load of 3.3 kΩ. Change in output with temperature is approximately 5 percent from -55 to +100°C. A low impedance output may be obtained by using a capacitive divider in place of C_2. Distortion is approximately 10 percent.

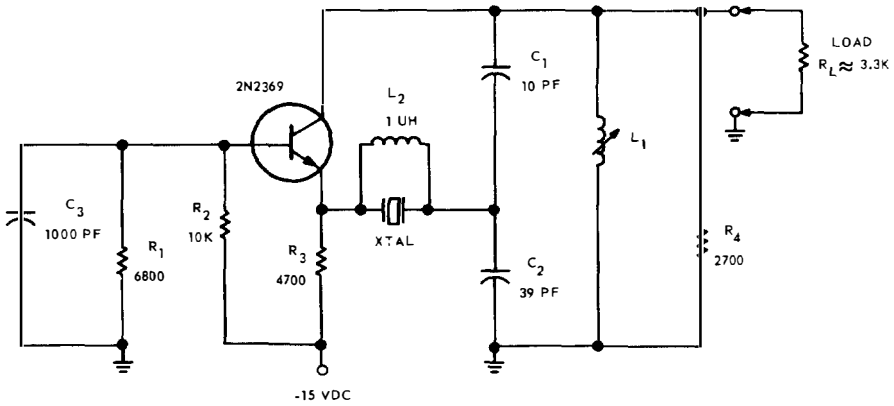

Figure 7-21. 75-MHz grounded-base oscillator: schematic diagram.

NOTE. R_4 is used for stabilization and should not be included in the load.

g. Power input: 40 mW.

7.5.4. 110-MHz Grounded-Base Oscillator and Doubler

L_1 = 0.20–0.40 μH, 7 turns #26 wire close-wound on 0.162-inch-o.d. coil form. Slug: Carbonyl SF, $\frac{3}{8}$ inch long.

L_2 is chosen to be antiresonant with the C_0 of the crystal and any stray capacitance in parallel with it.

L_3, C_4: Omit if transistors with a higher f_t are used.

L_4: 2 $\frac{1}{2}$ turns #18 wire, $\frac{3}{16}$-inch-i.d., $\frac{9}{64}$ inch long.

C_1 has a negative temperature coefficient of 470 ppm/°C to compensate for temperature changes in the inductor, L_1 and in the remaining oscillator circuitry.

a. Crystal: Similar to CR-56A/U.
b. Load capacitance: Series resonance.
c. Drive level: Nominally 2 mW.
d. Spurious responses: 3 : 1 or 120 Ω, whichever is greater.
e. Pin-to-pin capacitance: 4.5 pF maximum.
f. Factors affecting frequency stability are as follows:
   1. Temperature coefficient of crystal: ±0.005 percent from -55°C to +105°C.

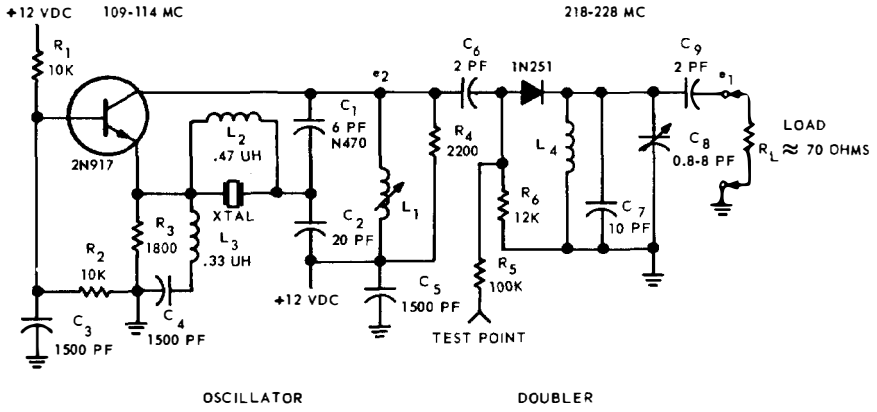

Figure 7-22. 110-MHz grounded-base oscillator and doubler: schematic diagram.

2. Aging rate of crystal: See section 5.7.
3. Temperature coefficient of oscillator circuitry: 2 parts in 10^8/°C.
4. Voltage coefficient of oscillator: 8 parts in 10^7 for a 10-percent supply in voltage change.

g. Output: For R_L = 70 Ω, e_1 is approximately 0.15–0.25 V at 220 MHz.

7.6. GATE OSCILLATORS

The use of logic gates in crystal oscillators is common in systems where the oscillator output must drive digital hardware. These oscillators are generally of lesser stability than those discussed previously in this chapter; however, they are very useful and a large variety of such oscillators have been used. Nearly all types of gate oscillators are prone to problems with respect to free running and spurious oscillations, and it is recommended that the oscillators be thoroughly tested in accordance with the procedures outlined in the following chapter prior to committing them to production. Several types of gate oscillators which have been found to work satisfactorily in some applications are discussed in the following paragraphs.

7.6.1. Single-Gate Oscillators

The single-gate oscillators, particularly in the lower frequency range using CMOS gates, have proven to be satisfactory in many applications. The frequency stability is generally not as good as that obtained with the transistor oscillators discussed earlier such as the Pierce and Colpitts circuits. As a result, gate oscillators are usually not used in temperature-compensated applications or oven frequency standards. When a frequency stability degradation of several parts per million from that of the crystal can be tolerated, the use of a single-gate oscillator is often a good choice.

A basic low-frequency gate oscillator circuit is shown in Figure 7-23 and consists of the gate *U1* followed by a resistance R_2 to raise the effective output impedance of the gate. This combination of the gate and resistor may be thought of as replacing the transistor in a Pierce oscillator. Refer to Figure 7-1.

The gate provides the necessary gain and produces a phase shift of 180 degrees. The π-network, consisting of C_1, C_2, and the crystal, produces an additional 180 degrees of phase shift, thus satisfying the 360-degree phase shift requirements for oscillation.

The crystal looks inductive and is resonant with capacitors C_1 and C_2. The frequency of oscillation automatically adjusts itself so that this is true; therefore, the combination of the crystal and C_1 alone has a net inductive reactance at the operating frequency.

Current I_1 lags voltage e_2 by 90 degrees. Voltage e_1 being developed across capacitor C_1 lags current I_1 by 90 degrees, making it 180 degrees behind voltage e_2. Since the combination of C_1 and the crystal is resonant with C_2, the gate, through R_2, sees a resistive load.

This explanation is valid only at low frequencies where the gate produces no phase shift, and if the input impedance of the gate is negligible compared to the output impedance of the π network. In the more usual case some phase compensation for these effects is necessary and occurs at the input of the π network due to the presence of R_2 which then looks into a somewhat reactive load. The capacitors C_1 and C_2 are then not exactly resonant with the crystal. In some gate oscillators the input impedance of the gate significantly loads the π network which also reduces the maximum resistance that the circuit can accommodate. At low frequencies, the single gate oscillator can usually be designed to accept the maximum crystal resistance with no difficulty. A more difficult aspect of the design seems to be the elimination of spurious and relaxation type oscilla-

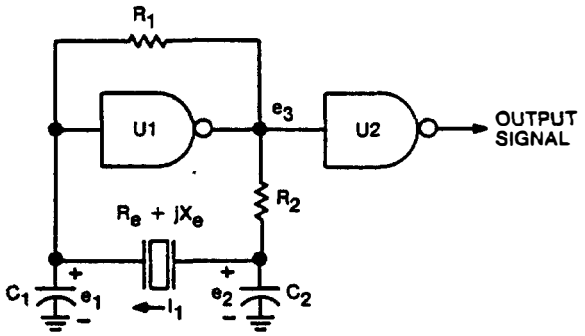

Figure 7-23. Basic low-frequency gate oscillator.

tion. In some cases during the design the circuit may actually fail to oscillate on the crystal frequency but produce relaxation type oscillation at some other frequency. In other cases the circuit will oscillate on the crystal frequency with an envelope at another frequency appearing on the signal. In other cases, and this is perhaps the most evasive, the circuit will operate satisfactorily with a typical crystal but will cause spurious oscillations with a high resistance crystal or if the crystal is removed. These conditions should be evaluated prior to completing the design and if not permissible in a particular application they must be eliminated.

It is often rather difficult to completely eliminate the tendency for these free running oscillations and a great deal of component value modification may be necessary, as well as layout changes and improvements in the supply voltage bypassing. It has been found that in some cases that the use of a second gate for load isolation, as shown in Figure 7-23 may result in relaxation oscillation tendencies and the choice of which gate on the chip is used may have an impact on the performance.

Even though the gate oscillators are plagued with these spurious tendencies they are widely used and have proven to be satisfactory in many applications. The designer must be aware of the potential problems and even though the circuits appear simple and straight forward to design, the design effort should not be terminated when the circuit first starts to oscillate.

The circuit can be analyzed analytically by substituting the Y-parameters of the gate with the resistor R_2 on its output into the equations for the Pierce oscillator given in section 7.2.

In section 7.2 it is shown that for oscillation to take place,

$$g_{fe} X_1 X_2 \geqslant R_e + K_1 \tag{7-59}$$

and

$$X_1 + X_2 + X_e = 0 + K_2, \tag{7-60}$$

where K_1 and K_2 are second-order corrections given by:

$$K_1 = -X_1(X_2 + X_e)g_{ie} - X_2(X_1 + X_e)g_{oe} - R_e X_1 X_2 (g_{ie} g_{oe} + b_{fe} b_{re}) - b_{re} g_{fe} X_1 X_2 X_e \tag{7-61}$$

and

$$K_2 = b_{fe}X_1X_2 + X_1X_2X_eg_{ie}g_{oe} - R_e(X_1g_{ie} + X_2g_{oe}) + b_{re}X_1X_2 + b_{re}b_{fe}X_1X_2X_e - b_{re}g_{fe}X_1X_2R_e. \quad (7\text{-}62)$$

Assuming that the Y-parameters of the gate are known, we can determine the Y-parameters of the combination of the gate and a series output impedance Z. (Refer to Figure 7-24.)

We find that

$$y_i = y_{11} - \frac{y_{12}y_{21}Z}{1 + y_{22}Z}, \quad (7\text{-}63)$$

$$y_r = y_{12} - \frac{y_{12}y_{22}Z}{1 + y_{22}Z}, \quad (7\text{-}64)$$

$$y_f = \frac{y_{21}}{1 + y_{22}Z}, \quad (7\text{-}65)$$

and

$$y_o = \frac{y_{22}}{1 + y_{22}Z}. \quad (7\text{-}66)$$

If the reverse transfer admittance is negligible and $y_{22}Z = y_{22}R_2 >> 1$, then equations (7-63) through (7-66) simplify to

$$y_i = y_{11} \quad (7\text{-}67)$$

$$y_r = 0 \quad (7\text{-}68)$$

$$y_f = \frac{y_{21}}{y_{22}R_2} \quad (7\text{-}69)$$

$$y_o = \frac{1}{R_2} \quad (7\text{-}70)$$

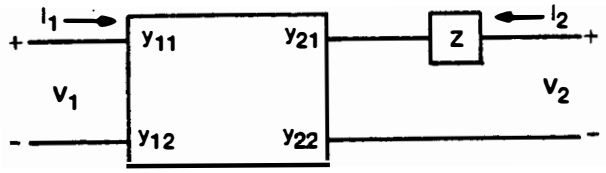

Figure 7-24. Gate with external output impedance.

We note also that the open-loop gain of a two-port is given by

$$A = -\frac{y_f}{y_o} \doteq -\frac{y_{21}}{y_{22}}; \tag{7-71}$$

hence $y_f \doteq -A/R_2$. The gain of a typical CMOS gate is on the order of 20. The values used for R_2 may vary from perhaps 300 kΩ at 30 kHz to 10 kΩ at 300 kHz. The value of R_1 (Figure 7-23) is usually chosen in the 10- to 20-MΩ range to bias the gate in its active region. Circuit values for a 200 kHz oscillator constructed by the author are listed in Table 7-2.

Table 7-2. Circuit Values for Low-Frequency Gate Oscillator.*

Frequency (kHz)	Gate type	R_1 (MΩ)	R_2 (kΩ)	C_1 (pF)	C_2 (pF)
200.0	4049	22	12	120	24

*See footnote p. 66.

The 200-kHz circuit uses a 20-pF crystal. The voltage coefficient for this circuit was in the order of 3 pp 10^7 per percent of supply voltage change. The gate pulls the frequency approximately 7 pp 10^8/°C. Power supply current including the buffer is 1.7 mA from a 5-V supply.

At higher frequencies, above approximately 1 MHz, the circuit of Figure 7-23 is not entirely satisfactory because of lagging phase shift in the gate, and it is necessary to replace resistor R_2 with a capacitor C_3, as shown in Figure 7-25. Equations (7-59) and (7-60) may still be used to analyze the circuit; however, equations (7-63) through (7-66) should be used to determine the Y-parameters of the gate with capacitor C_3 on the output. Z in this case is $-j/\omega C_3$. It should be noted that in the derivation of the equations for the Pierce oscillator, it was assumed that the input and output susceptances of the transistor were lumped into C_1 and C_2 so that b_{ie} and b_{oe} do not appear in the equations for oscillation. Here also b_{ie}/ω should be added to C_1; b_{oe}/ω to C_2.

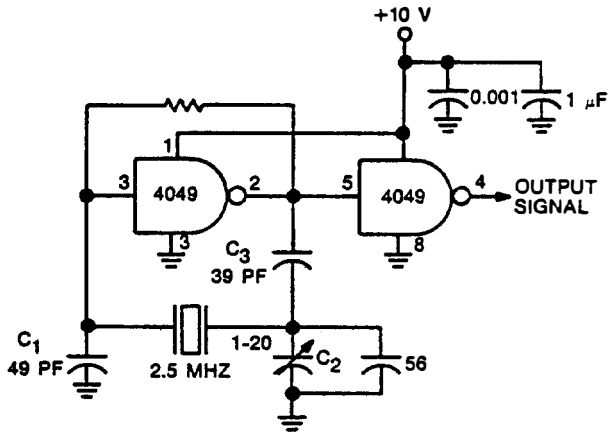

Figure 7-25. 2.5-MHz gate oscillator.

The circuit shown in Figure 7-25 uses a 32-pF parallel resonant crystal.

The voltage coefficient of the oscillator is on the order of 6 parts in 10^8/percent of supply voltage change. The voltage coefficient is somewhat dependent on the value of C_3 which should not be made smaller than perhaps 20 pF. The current drawn by the circuit is 6.5 mA from a 10-V supply or 1.5 mA from 6 V dc. The voltage at the gate output is 10 V peak to peak for 10 V supply and 6–10 V peak to peak at the gate input, depending on the crystal resistance. The gate pulls the frequency approximately 5 parts in 10^8/°C.*

For frequencies higher than a few MHz, it is necessary to use TTL gates for satisfactory operation. Unfortunately the large resistor R_1 is not adequate to bias a TTL gate into the active region. Low values of R_1 produce a considerable signal feedback and reduce the gain to an unacceptable level. The arrangement shown in Figure 7-26 is reasonably acceptable, however, there may be some tendency for free running and relaxation oscillation, which is a function of the gate and the circuit layout. The designer should particularly watch for these if he elects to use this type of circuit.

For the circuit of Figure 7-26, the gate pulls the frequency of the crystal less than 1 ppm over the temperature range from -40°C-

*See footnote p. 66.

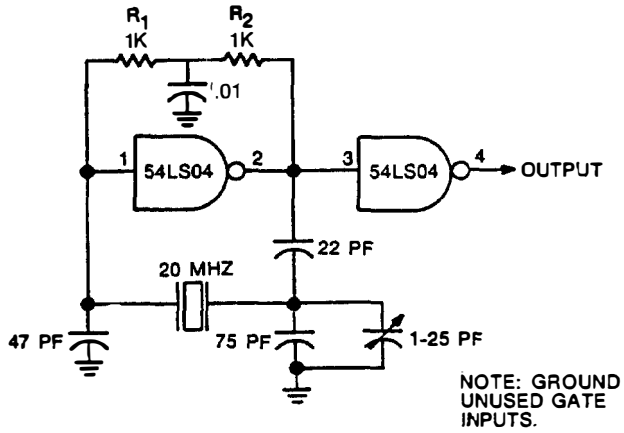

Figure 7-26. 20-MHz gate oscillator.

+65°C. This should be added to the basic crystal frequency tolerance, which is usually 25–50 ppm, depending on the crystal used.

The voltage coefficient was found to be 2–10 parts in 10^7 for a 20-percent supply voltage change.*

If the circuit is used at lower frequencies, C_1, C_2, and C_3 should be increased to ensure operation on the fundamental mode of the crystal. A series capacitor can then be used with the crystal to tune it to frequency. Since this circuit is quite prone to free-running oscillation, particularly with small values of C_1, it should be thoroughly tested with maximum-resistance crystals and limit-of-tolerance parts.

7.6.2. Multiple-Gate Oscillators

Multiple-gate oscillators, usually using two gates, are less stable than single-gate oscillators and are also prone to oscillation on the wrong mode if improperly designed. They have nevertheless been widely used, perhaps because of their (theoretically, at least) minimum number of external components. A dual-gate oscillator which has been found to work satisfactorily in some applications (see Figure 7-27) uses a series resonant crystal. It can be used up to about 20 MHz with TTL gates. In many applications this oscillator has been used without the series resonant circuit consisting of L_1 and C_2 between the two gates. The inductor L_1 is simply omitted and C_2 is replaced by a bypass capacitor. The series resonant circuit contributes nothing at

*See footnote p. 66.

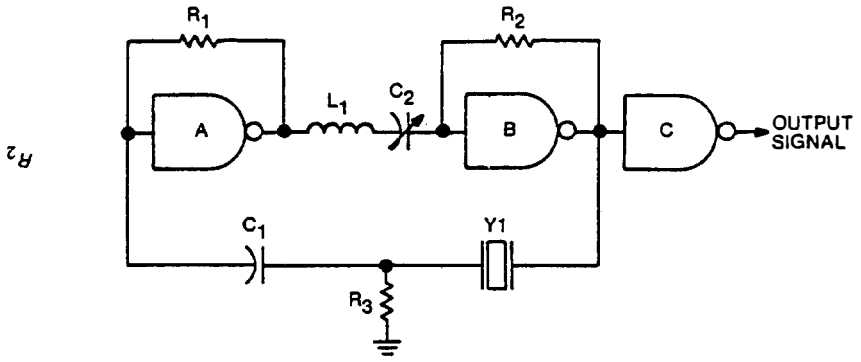

Figure 7-27. Basic dual-gate oscillator circuit.

the desired frequency of oscillation; rather, it provides protection against oscillation on the wrong mode. In some applications, particularly at low frequencies, R_3 and C_1 have been successfully omitted as well.

The two gates, *U-A* and *U-B*, are biased into the active region by resistors R_1 and R_2 to provide an amplifier with a gain A at a phase angle of approximately 360 degrees.

The feedback network is composed of the crystal, represented by an impedance $(R_e + jX_e)$, R_3, and C_1. At low frequencies the amplifier presents no phase shift, and C_1 is not required to correct for lagging phase shift in the gates. R_3 may be used to stabilize the input impedance of *U-A* and generally to present a lower resistance into which the crystal may work.

The oscillator may be analyzed by the use of equation (3-1) (Chapter 3) if the amplifier is represented by its Y-parameters and the feedback network by its Z-parameters. The Z-parameters may be written from inspection and are:

$$Z_{11} = (R_e + R_3) + jX_e \tag{7-72}$$

$$Z_{12} = Z_{21} = R_3 \tag{7-73}$$

$$Z_{22} = R_3 + jX_{C1} \tag{7-74}$$

where $X_{C1} = -1/\omega C_1$. (7-75)

Also defining $\Delta Z = Z_{11} Z_{22} - Z_{12} Z_{21}$, we have (7-76)

$$\Delta Z = (R_3 R_e - X_e X_{C1}) + j[R_3 X_e + (R_e + R_3) X_{C1}]. \tag{7-77}$$

The analysis may be considerably simplified by assuming that the input and output admittances of the amplifier are real and that the reverse transfer admittance is negligible. Then $y_{11} = g_{11}$, $y_{12} = 0$, $y_{21} = g_{21} + jb_{21}$, and $y_{22} = g_{22}$. Also defining $\Delta y = y_{11}y_{22} - y_{12}y_{21}$, we have $\Delta y = g_{11}g_{22}$.

The general equation for oscillation given in Chapter 3 requires that:

$$y_{21}Z_{21} + y_{11}Z_{22} + y_{22}Z_{11} + y_{12}Z_{12} + \Delta y \Delta Z + 1 = 0. \quad (7\text{-}78)$$

Substituting the values for this oscillator, we have

$$(g_{21} + jb_{21})R_3 + g_{11}(R_3 + jX_{C1}) + g_{22}[(R_e + R_3) + jX_e]$$
$$+ g_{11}g_{22}(R_3R_e - X_eX_{C1}) + jg_{11}g_{22}(R_3X_e + R_eX_{C1} + R_3X_{C1}) + 1 = 0. \quad (7\text{-}79)$$

The imaginary part of the equation is given by

$$X_e = \frac{-b_{21}R_3 - X_{C1}g_{11}(1 + g_{22}R_e + g_{22}R_3)}{g_{22}(1 + g_{11}R_3)}. \quad (7\text{-}80)$$

The value of X_{C1} required to operate the crystal at series resonance is found by setting $X_e = 0$ and solving for X_{C1}.

$$X_{C1} = \frac{-b_{21}R_3}{g_{11}[1 + g_{22}(R_e + R_3)]}. \quad (7\text{-}81)$$

In the low-frequency case, when $b_{21} = 0$, we see that $X_{C1} = 0$ and R_3 is unnecessary. If b_{21} is not zero, we see that since the product R_3b_{21} occurs in equation (7-80), smaller values of R_3 result in a more stable oscillator so long as the crystal drive level is not excessive.

At higher frequencies the required value of C_1 may be quite small, and this may lead to unstable operation because of other potential modes of operation. It may therefore be desirable to place a 20- to 30-pF capacitor directly in series with the crystal to bring it up to frequency rather than to make C_1 too small.

Referring now to equation (7-79), we see that the real terms result in the equation

$$\frac{g_{21}}{g_{22}} + \frac{g_{11}}{g_{22}} + \frac{R_e + R_3}{R_3} + g_{11}R_e - \frac{g_{11}X_eX_{C1}}{R_3} + \frac{1}{g_{22}R_3} = 0.$$

Now representing the open-loop voltage gain of the amplifier by $A = -g_{21}/g_{22}$ and assuming that C_1 is adjusted so that crystal reactance $X_e = 0$, we have

$$A \geqslant \left(\frac{R_e + R_3}{R_3}\right) + g_{11}\left(R_e + \frac{1}{g_{22}}\right) + \frac{1}{g_{22}R_3} \tag{7-83}$$

for oscillation to start.

A few comments may be appropriate regarding the Y-parameters of the two gates in cascade. It is desirable simply to measure the admittance parameters of the amplifier. If, however, the Y-parameters of the individual gates are known, then it can be shown that the presence of a biasing (feedback) resistor modifies the Y-parameters according to the following relationships:

$$y_{11} = y_i + \frac{1}{R_1}, \qquad y_{12} = y_r - \frac{1}{R_1}$$

$$y_{21} = y_f - \frac{1}{R_1}, \qquad y_{22} = y_o + \frac{1}{R_1},$$

where y_i, y_r, y_f, and y_o are the Y-parameters of an individual gate. It can also be shown that placing two gates in cascade results in a final set of Y-parameters:

$$y_{11} = y_{11a} - \frac{y_{12a}y_{21a}}{y_{11b} + y_{22a}} \tag{7-84}$$

$$y_{12} = -\frac{y_{12a}y_{12b}}{y_{11b} + y_{22a}} \tag{7-85}$$

$$y_{21} = -\frac{y_{21a}y_{21b}}{y_{11a} + y_{22b}} \tag{7-86}$$

$$y_{22} = y_{22b} - \frac{y_{12b}y_{21b}}{y_{11b} + y_{22a}}. \tag{7-87}$$

As a practical matter, it may be satisfactory to experimentally optimize component values from typical gate oscillators in the same frequency range. Table 7-3 gives typical values for the components of gate oscillators at 7 MHz, 9 MHz, and 20 MHz.

As noted earlier, the frequency stability of the dual-gate oscillators

Table 7-3. Typical Values for Dual-Gate Oscillator.*
(See circuit diagram of Figure 7-27)

7	54LS04	1	3.9	none	none	1000	none
9	5404	0.680	0.680	100	470	20	15
20	54LS04	0.680	2.2	100	100	10	12

*See footnote p. 66.

is poor compared to the oscillators discussed previously. For the 20-MHz oscillator, typical gates pull the crystal about 5 ppm over a 70°C temperature range. This varies greatly from gate to gate and may be as high as 50 ppm. The frequency of the test oscillator also changed from 1 to 3 ppm for a 0.1-V supply voltage variation, which is about 2 orders of magnitude worse than for the single-gate circuit of Figure 7-26.

The 20-MHz crystal operates about 500 Hz below series resonance, which can be corrected by placing a 27-pF capacitor in series with it. The frequency can also be raised by making C_1 = 27 pF; however, with this value of C_1, the circuit is bordering on instability and must be carefully checked in the final mechanical configuration.

The voltage coefficient of the 7-MHz dual-gate circuit was found to be 4.6 ppm for a 0.1-V supply voltage change. The crystal operates about 2 kHz below series resonance.

It should be noted that the dual-gate oscillators, like the single-gate units, are prone to free-running oscillations, particularly if the crystal is not present; this must be considered in making the choice to use a gate oscillator.

Performance of the 9-MHz oscillator is much the same as that of the 20-MHz circuit. If a 54LS04 is used, the waveform is slightly improved by increasing R_2 to 2.2 kΩ.

7.7. INTEGRATED-CIRCUIT OSCILLATORS

A large number of integrated circuits (ICs) are available which can be used as crystal oscillators or which include a crystal oscillator. The information presented here regarding these circuits is related both to the design and the application of the devices, although it

is somewhat slanted toward the application. Many existing ICs require only the attachment of an external crystal, while some require other components as well. The circuits at the time of this writing tend to fall into three categories. The first provides a single bipolar or field effect transistor to which the external crystal and feedback network can be attached. For this class of circuits the design equations developed for transistor oscillators earlier in the section are directly applicable, and the frequency stability is generally quite good.

A second class of circuits, often using MOS technology, provide a gate which can be used as a crystal oscillator. The design techniques developed in section 7.6 for gate oscillators are then directly applicable and the frequency stability is generally equivalent to that of oscillators using discrete gates of the same type.

The third class of circuits is designed with a multistage amplifier on the chip and the external crystal either closes the feedback path from the amplifier output to its input or it serves as a frequency-selective bypass at some point in the amplifier. Many of these circuits are used as clock drivers for microprocessors (or on microprocessors), as frequency synthesizers, modems, TV circuits, phase-locked loops, and the like. As might be expected, the frequency stability varies greatly with the design, and while some are good, others are very poor indeed.

Because of the large number of circuits being introduced and/or available, a detailed treatment of specific circuits is impractical. A number of general comments and principles apply, however, which are helpful. It should be obvious that in most cases the application of sound design principles will result in an oscillator of increased stability at essentially no difference in cost from a poorly designed circuit and may make the product more useful. For example, a microprocessor may use a crystal to stabilize the clock frequency on the chip. A frequency error of 1 percent may be almost inconsequential with respect to operation of the processor; however, if the oscillator is designed well, the inherent stability may be ±0.0025 percent or better. The clock can then be used as the reference oscillator to control the carrier of a radio transmitter, the time base for a digital clock, or some other function as required. In such equipments the applications engineer may wish to examine the stability of several circuits to find a suitable unit for his purpose.

Since a considerable variety of amplifier configurations is possible on a chip, no attempt is made here to analyze specific circuits. An analytic treatment is developed based on the terminal parameters of the circuits. Several general comments can also be made regarding the design of multistage integrated oscillators. Since an oscillator is sensitive to both the amplitude and phase of the amplifier, circuits with a considerable amount of phase shift will cause the crystal to operate well below (or in some cases above) series resonance. To operate on frequency the oscillator must be designed to require the same reactance for which the crystal was calibrated when manufactured (see Chapter 5). This can be determined by measuring the frequency of the crystal at series resonance (see Chapter 5), or the desired load point, and adjusting the oscillator components to obtain that frequency. If the phase shift is not too severe a series capacitor can often be used to raise the crystal frequency. Very small values of capacitance may indicate that the amplifier is unsuitable, and may also result in a tendency for the oscillator to free-run through the C_0 of the crystal (see Chapter 5) rather than at the piezoelectric resonance. If sufficient gain and phase shift are present, free running may take place through C_0 even though no external capacitor is used.

It should be noted that the crystal can oscillate on odd mechanical overtones as well as on the fundamental frequency. If the gain is higher at the overtone frequency than on the fundamental, and if no tuned circuit is used, oscillation on the overtone will result. Conversely, if operation on an overtone is desired, it will in general be necessary to provide a tuned circuit which limits the region of gain to the vicinity of the desired overtone.

If the oscillator being designed may be operated over a large range of frequencies, it is important to check it at all frequencies in the band to ensure, first, that oscillation will always occur, and secondly, that free-running oscillations will not occur. A 20-MHz crystal may have a resistance of 10–20 Ω, while a 100-kHz crystal may have a 100-kΩ series resistance. It does not follow that oscillation at 20 MHz guarantees oscillation with a 100 kHz crystal as well.

Extensional and flexural mode crystals in the low-frequency region may have active spurious responses near the desired response. Excess gain in the oscillator may in some cases result in oscillation

on these spurious modes rather than on the desired frequency. When the circuit is turned on, oscillation builds up on all frequencies for which the phase requirement of 360 degrees occurs and the gain is greater than unity. The mode reaching the saturation amplitude first or having the most gain generally will survive and suppress the others (although it is possible to sustain multiple oscillations in some oscillators with high gain). The circuit should be carefully examined under as many conditions as possible to ensure that spurious oscillations will not occur. It is also good practice to check the frequency over the required temperature range as well as the frequency change due to supply voltage variation and load changes. The frequency drift over temperature caused by the IC can be determined approximately by connecting the crystal to the oscillator with the crystal external to the temperature chamber. A high-impedance balanced transmission line may be suitable for the connection. In some cases it may be necessary to use a small blower on the crystal to prevent temperature changes resulting from thermal conduction in the transmission line. A more accurate procedure is to measure the crystal temperature coefficient with a CI meter, Vector Voltmeter test set, or bridge, and subtract the crystal frequency drift from the total temperature coefficient. In a good oscillator the frequency change caused by the active circuit will be insignificant compared to that caused by the crystal.

While it is desirable in the design of integrated-circuit oscillators to use a set of analytic tools, the detailed equations for oscillation are generally too complex to be useful. Two approaches are presented here based on the terminal parameters of the integrated circuit. In those circuits where the crystal acts as a frequency selective bypass in the amplifier which is internally crosscoupled, it may be convenient to think of the circuit as a negative-resistance element in series with an inductance. An approximate equivalent circuit is shown in Figure 7-28. A series compensating capacitor C is shown in series with the crystal. For on-frequency operation with a series resonant crystal, C should be resonant with L_0 at the nominal frequency of the crystal. The resistance R_n is a negative value and must be larger in magnitude than the equivalent resistance of the crystal for oscillation to take place.

It is possible to determine the magnitude of R_n in several ways.

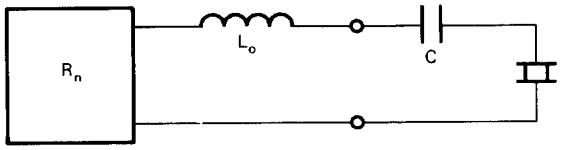

Figure 7-28. Negative-resistance oscillator with series compensating capacitor.

Perhaps the most obvious is to place a crystal between the appropriate terminals of the IC and add series resistance until oscillation will no longer occur. The magnitude of the negative resistance is then given by the sum of the crystal resistance and the additional series resistance. The magnitude of the oscillator inductance can be found by noting the difference between the frequency of oscillation and the series resonant frequency of the crystal (without C or the series resistance) and calculating*

$$L_0 = \frac{1}{(2\pi f_s)^2 \left(\frac{C_1}{2\Delta f/f} - C_0\right)}. \tag{7-88}$$

It can also be found experimentally by selecting C to obtain the series resonant frequency of the crystal. Then

$$L_0 = \frac{1}{(2\pi f_s)^2 C}. \tag{7-89}$$

Since the equivalent inductance will in general vary as a function of frequency it should be computed near the nominal frequency of the crystal to be used.

It is desirable to minimize the equivalent inductance of an oscillator for several reasons. First, the equivalent inductance will change with temperature and supply voltage, causing the oscillator frequency to drift. Secondly, it may result in free-running oscillations through the C_0 of the crystal.

The equivalent inductance is a result of phase shift in the amplifier and can be minimized in the design by using as few stages as possible

*See Figure 5-1 for definition of terms.

and by increasing the bandwidth of the amplifier. The negative resistance will, of course, be a function of the gain of the amplifier and the impedance level where the crystal is placed.

In general the circuit may have a negative impedance characteristic such as that shown in Figure 7-29. The negative-resistance region is restricted to a portion of the voltage current characteristic. As oscillation builds up, the voltage swings beyond the negative-resistance region and the equivalent resistance becomes less negative. Finally at saturation (or equilibrium if AGC is used) the equivalent negative resistance equals the positive resistance of the crystal. It can be shown[13] that the crystal current builds up according to the equation:

$$i(t) = Ke^{-at} \sin(\omega t + \theta) \tag{7-90}$$

where

$a = (R_1 + R_n)/2L$, and

$\omega = \sqrt{(1/LC) - a^2}$.

Here L is the sum of the crystal inductance and L_0. C_0 was neglected in the analysis. So long as R_n is negative and larger than R_1, the amplitude continues to build up. Finally when $R_1 = -R_n$ an equilibrium condition is reached. Equation (7-90) also shows that the frequency of oscillation is lowest initially and increases slightly as the circuit stabilizes.

Test data on several ICs of the crosscoupled type shows a wide variation in equivalent inductance, from approximately 1–2 μH to greater than 250 μH over the frequency range from 1 to 20 MHz. Therefore, while some ICs operate with the crystal near series resonance, others operated as much as 1 percent low in frequency.

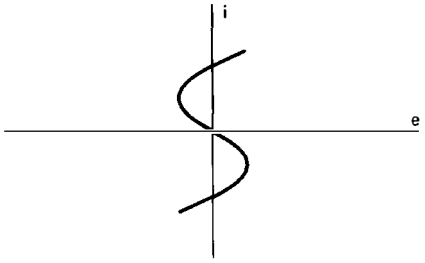

Figure 7-29. Negative-resistance characteristic of oscillator.

Some manufacturers provide excellent data sheets which not only characterize the equivalent circuit but also provide data on the environmental stability, and in some cases on the noise level as well. Others provide little more than a pin connection diagram showing where to connect the crystal. To achieve maximum versatility of the product, designers are encouraged to provide complete information on their oscillators. Conversely, if such information is not provided, the applications engineer should run complete tests on an IC prior to committing the circuit to production, particularly if a frequency stability approaching that of the crystal is required. Typical temperature coefficients for the better ICs of the cross-coupled type are 10–15 parts in 10^8/°C exclusive of the crystal temperature change.

As indicated earlier, a number of ICs use an amplifier on the chip and connect an external crystal between the output and input of the amplifier. While these circuits can be thought of as negative-resistance oscillators, it may be desirable to analyze them as amplifiers with a feedback network composed solely of the crystal. Such a circuit is shown in Figure 7-30. Here as before, the Y-parameters are used for the amplifier. From the definition of these parameters (see Appendix A) we may write the equations:

$$I = y_{11} V + y_{12} V' \tag{7-91}$$

$$-I = y_{21} V + y_{22} V'. \tag{7-92}$$

We also not that

$$V = V' - I(R_e + jX_e). \tag{7-93}$$

Solving the simultaneous equations for V gives:

$$V = \frac{\begin{vmatrix} 0 & -y_{12} & 1 \\ 0 & -y_{22} & -1 \\ 0 & -1 & R_e + jX_e \end{vmatrix}}{\begin{vmatrix} -y_{11} & -y_{12} & 1 \\ -y_{21} & -y_{22} & -1 \\ 1 & -1 & R_e + jX_e \end{vmatrix}}$$

Since the numerator is zero, V will be zero unless the denominator is

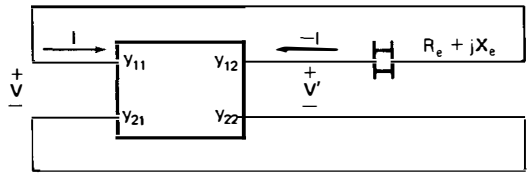

Figure 7-30. Integrated circuit with external crystal.

also zero. The conditions for oscillation may then be found by equating the determinant in the denominator to zero, which gives

$$\sum y + R_e \Delta y + jX_e \Delta y = 0, \tag{7-94}$$

where

$$\sum y = y_{11} + y_{12} + y_{21} + y_{22}, \text{ and}$$

$$\Delta y = y_{11}y_{22} - y_{12}y_{22}$$

If there is no phase shift in the amplifier, the Y-parameters are real and from equation (7-94) we see that the imaginary part is satisfied by the condition $X_e = 0$, which is the desired operating point for a series resonant crystal.

Unfortunately, a multistage amplifier tends to have considerable phase shift, and the crystal normally operates below series resonance where X_e is negative. If the phase shift is not too severe, the frequency can be brought up to series resonance by placing a capacitor in series with it. (A note of caution here is that small capacitors, approaching the value of the holder capacitance C_0, may lead to free-running oscillations above the crystal frequency.)

An amplifier which has a considerable amount of phase shift at the operating frequency is undesirable from another consideration. The phase shift of any amplifier tends to change with temperature and voltage. An amplifier with a large phase shift will therefore also have a large phase change with temperature and supply voltage variation. The phase changes result in a change in frequency so that the crystal reactance makes up for the phase difference. The crystal reactance changes rapidly with frequency; however, variations of hundreds of parts per million can result particularly if the phase correction being made by the crystal is already approaching 90

degrees. It is apparent, therefore, that the fewer stages in the amplifier, provided the gain requirement can be met, the more stable the oscillator will be. Indeed the circuits using a single transistor with two external feedback capacitors in a π network with the crystal tend to make the best oscillators.

It is possible to plot equation (7-94) in two parts and in some cases obtain a better understanding of the crystal reactance required for oscillation. If a Smith chart is used the curve given by

$$Z = -\sum y/\Delta y$$

can first be plotted at the nominal crystal frequency as a function of input amplitude. A second curve representing $R_e + jX_e$ for the crystal as a function of frequency can then be added and the intersection represents the frequency and amplitude of oscillation.

The oscillator is not limited to operation in the resonant region of the crystal, and a search can also be made for spurious oscillations. This can be done by plotting Im Z as a function of frequency on a rectangular graph along with X_e, which will be a plot of C_0, the holder capacitance, except near piezoelectric resonances. Any intersection of the two reactance curves where Re Z is greater than R_e represents a potential frequency of oscillation and should be searched for during testing of the circuit.

A very serious problem may arise in using the Y-parameters here as equivalent admittances as a function of amplitude, particularly if the output stage of the amplifier performs the limiting function. Since the Y-parameters are measured with the input/output short-circuited, the real limiter will then not be measured. Under these conditions, the oscillator output voltage will normally be close to the peak-to-peak swing of the output amplifier.

Chapter 8 deals with tests which should be performed on any oscillator prior to committing it to production. Although some of the material presented here is duplicated in Chapter 8 it is felt that the designer or user of an integrated-circuit oscillator should be familiar with the tests recommended.