# 3
# Methods of Design

Three methods of design are presented in this book, each of which has its advantages. The first, which is highly experimental, consists of giving a qualitative explanation of how the circuit works and presenting a number of typical schematic diagrams for that oscillator configuration. The second method consists of deriving the equations for oscillation in terms of the $Y$-parameters of the transistor. The third method consists of measuring the gain and input impedance of the transistor as a function of its load impedance. This information is used to calculate component values for the circuit with relatively simple equations. The amplitude of oscillation can then be predicted using the methods of paragraph 3.4.

## 3.1. EXPERIMENTAL METHOD OF DESIGN

The experimental method of design consists of finding a suitable circuit which can be modified and/or optimized to meet a particular set of requirements. To assist in this design approach, Chapter 7 contains a number of laboratory tested oscillator circuits and a qualitative explanation of their operation. The appropriate circuit type most suited for a particular application can be selected with the aid of Table 7-1. The individual circuits have not been designed or optimized with respect to any particular performance characteristic, but sufficient reserve gain has been provided to allow some modification.

The following precautionary items must be presented in regard to the use or modification of any of these circuits:

a. Since the mechanical arrangement of a circuit usually affects its performance, complete testing of the circuit in accordance with Chapter 8 should be accomplished even though the circuit values presented are used.

b. Substitution of transistors or gates for those specified should be within the same basic family and power level. Indiscriminate substitution of active element types may greatly change the performance of a given oscillator circuit.

### 3.2. Y-PARAMETER METHOD OF DESIGN

The second approach to oscillator design consists of using the $Y$-parameters of the transistor (see Chapter 6). The equations for oscillation are derived in the following manner. Using the block diagram of Figure 3-1, the complex equation for oscillation can be shown (see Appendix A) to be:

$$y_f Z_f + y_i Z_o + y_o Z_i + y_r Z_r + \Delta y \, \Delta Z + 1 = 0, \qquad (3\text{-}1)$$

where

$$\Delta y = y_o y_i - y_f y_r, \qquad \Delta Z = Z_o Z_i - Z_f Z_r.$$

> Although any set of parameters may be used for the amplifier and any set for the feedback network, it is convenient to use $Y$-parameters for the amplifier and $Z$-parameters for the feedback network. . . . It is important to note that the use of equation (3-1) implies the assumption that the amplifier is a linear circuit. The application of equation (3-1) therefore can yield no information concerning harmonic generation or the limiting of amplitude as the result of dependence of circuit parameters upon amplitude. The assumption that the amplifier is linear is not valid at large amplitudes. At large amplitudes, the $Y$-parameters therefore must be defined as the ratios of fundamental components of current to fundamental components of voltage![41]

The equations for specific oscillator types are derived by determining the $Z$-parameters of the feedback network and substituting them

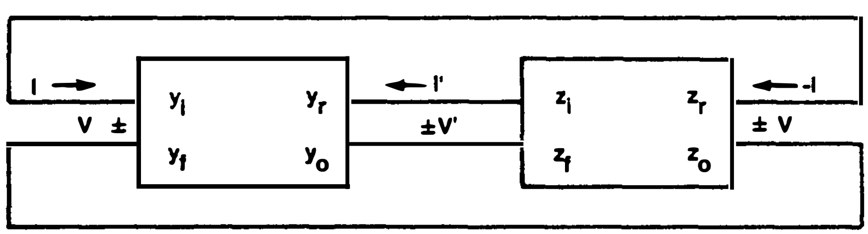


Figure 3-1. Block diagram of a transistorized crystal oscillator.

into equation (3-1). The complex equation is then separated into real and imaginary parts. The real part generally yields an expression for the transconductance $g_f$ required for oscillation while the imaginary part yields an expression for the crystal reactance $X_L$ necessary to satisfy the phase shift requirement. The equations and the assumptions made are presented for the various oscillators in Chapter 7.

Since the equations in general do not give highly accurate results, it is well to use them in connection with the experimental approach (see section 3.1). However, the equations do give an indication of how changing a given component will affect the overall performance and thus are often quite useful. The equations are generally of the form

$$g_f = f_1(a, b, c, d, \ldots)$$
$$X_L = f_2(a, b, c, d, \ldots),$$

where $a$, $b$, $c$, $d$ . . . represent various components and parameters of the circuit; $X_L$ is the crystal reactance; and $g_f$ is the small-signal transconductance required for oscillation to begin. The ratio $g_f$ (transistor)/$g_f$ (required) is a measure of the loop gain, which must be greater than unity for oscillations to build up. Generally, if the loop gain is greater than 2 to 3, satisfactory operation results. If limiting

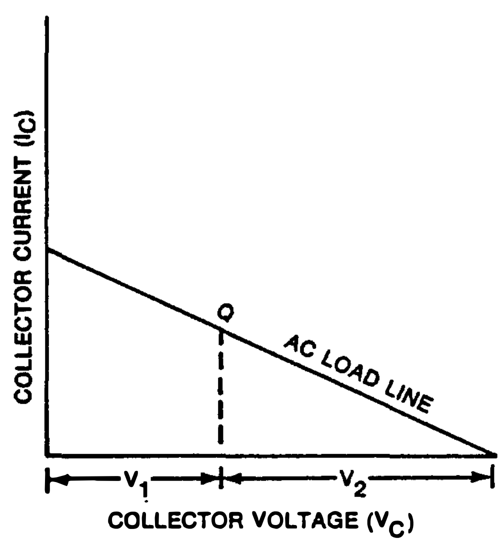


Figure 3-2. Voltage prediction from the $Q$-point and load line.[35]

takes place as a result of the base-to-emitter junction being cut off during part of the cycle, the amplitude of oscillation can be predicted using Figure 3-6. Limiting of this type generally results in good frequency stability. The oscillator may be biased to produce collector limiting. If this is the case, the output voltage can be determined by constructing a load line as shown in Figure 3-2. The peak output voltage will be approximately $V_1$ or $V_2$, whichever is smaller. This is a rule of thumb only and not highly accurate.

The oscillator should be designed to require the same crystal reactance ($X_L$) as that called out by the crystal specification for on-frequency operation. In the case of series resonant crystals, $X_L = 0$.

## 3.3. POWER GAIN METHOD OF DESIGN*

The third approach to oscillator design is basically a power gain analysis. Phase shift considerations are taken care of experimentally by getting the crystal to operate on frequency. The usefulness of this design approach generally is limited to series mode oscillators which can be represented by the block diagram of Figure 3-3.

The power gain required from the transistor must be sufficient to supply the output power, power losses, and the input power required

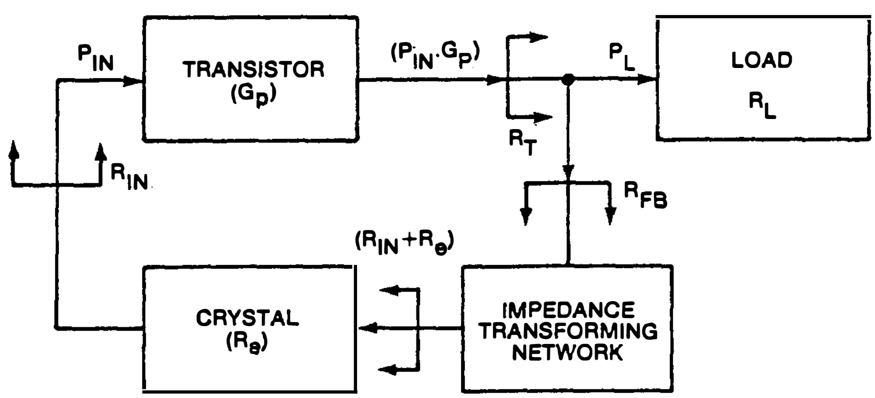


Figure 3-3. High-frequency oscillator elements.

*The results presented here are essentially a summary of the Power Gain Method of design developed under sponsorship of the US Army Electronics Command, see reference 31.

for the transistor:

$$(P_{in}\,G_P) = P_L + P_{in} + P_d, \tag{3-2}$$

where

$P_{in}$ = input power to transistor,
$G_P$ = power gain of transistor,
$P_L$ = output power to an external load, and
$P_d$ = all other power losses within the oscillator circuit.

Using equation (3-2), an oscillator may be designed as follows:

A. *Determine the transistor power gain (experimentally).*

*Step 1.* Connect the transistor as a single-tuned amplifier in the grounded-base or grounded-emitter configuration, whichever is to be used in the type of oscillator being designed. A circuit similar to that of Figure 3-4 may be used. The circuit should be arranged so that it can be mounted on the impedance measuring device such as a network analyzer or *RX* meter with the input near the ungrounded terminal. Provisions should be made for connecting RF voltmeters to the input and output of the transistor.

*Step 2.* Measure the power gain and input impedance as a function of the load resistance $R_T$.*

(a) For various values of load resistance, determine the power gain and the input impedance, increasing the value of the load resistor at each step until instability occurs.
(b) Plot the power gain and input resistance versus load resistance. A graph similar to that of Figure 3-5 should result.
(c) From the power gain graph, select a value $R_T$ giving a gain of 200–300, and note the input resistance $R_{in}$ at the power gain selected.

B. *Calculate the feedback network.* Power gain values determined in A include all circuit losses that will be present in the oscillator

*The maximum input voltage that can be applied to the transistor before nonlinearity occurs is about 10 mV. Since the output of the Boonton *RX* meter is about 100 mV, it must be modified. The addition of an appropriate level control is described fully in the *RX* meter instruction manual. In this discussion, $R_T$ refers to the total load resistance seen by the collector. $R_L$, the external load, is included in $R_T$.

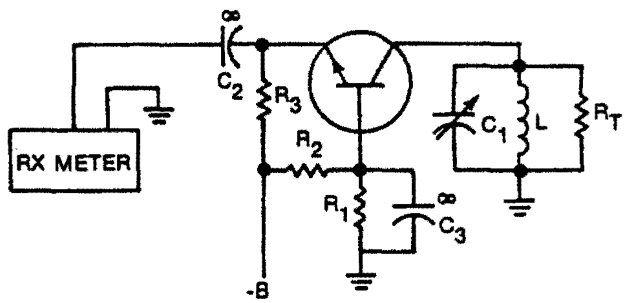


Figure 3-4. Single-tuned amplifier connection.

except the crystal loss. The crystal loss is included in the following manner.

*Step 1.* The ratio of the total feedback power to the transistor input power is given by

$$\frac{P_{\mathrm{FB}}}{\;} \cdot \frac{(R_{\mathrm{in}} + R_e)}{\;}, \qquad (3\text{-}3)$$

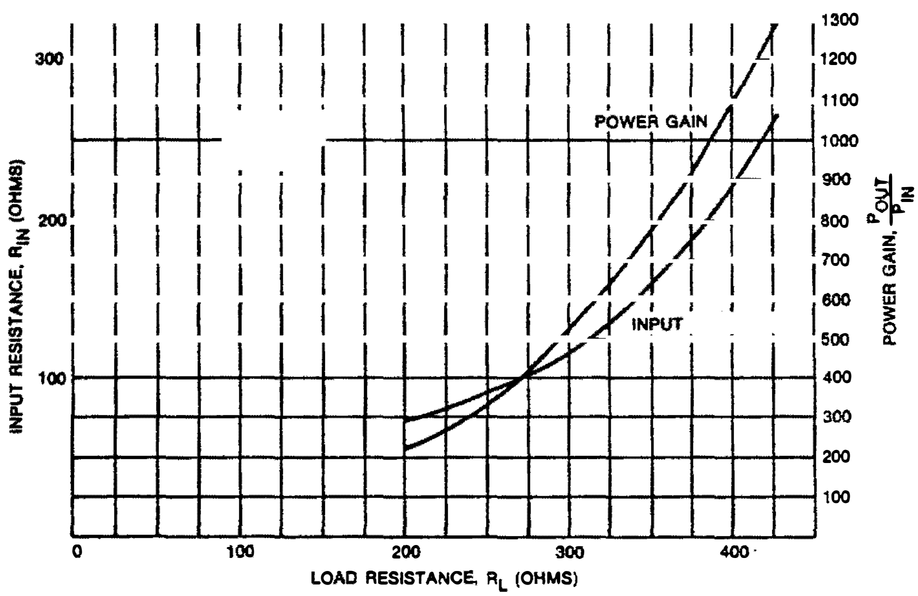


Figure 3-5. Input resistance and power gain versus load for 2N2218 transistor.[28,29]

where

$P_{FB}$ = total feedback power,
$P_{in}$ = the power input to the active device,
$R_{in}$ = the input resistance of the transistor, and
$R_e$ = the series resonant resistance of the crystal.

Incorporating this loss due to the crystal into the input circuit gives the modified power gain $G_p'$ as

$$G_p' = \frac{G_p R_{in}}{(R_{in} + R_e)}. \tag{3-4}$$

*Step 2*. The next step is to determine the ratio of the output power to the feedback power. All losses are accounted for now; therefore,

$$P_o = P_L + P_{FB}. \tag{3-5}$$

The output power also is given by

$$P_o = (P_{FB}\, G_p'). \tag{3-6}$$

Combining equations (3-5) and (3-6) gives

$$(P_{FB}\, G_p') = P_L + P_{FB}, \tag{3-7}$$

or

$$P_{FB} = \frac{P_L}{(G_p' - 1)}. \tag{3-8}$$

$P_{FB}$ can be represented by an equivalent resistor $R_{FB}$ (whose power dissipation is $P_{FB}$ placed in parallel with the external load $R_L$. $R_L$ and $R_{FB}$ are subjected to the same voltage; therefore, the resistance ratio is inverse to the power ratio, and

$$R_{FB} = R_L (G_p' - 1). \tag{3-9}$$

Now $R_T$, the total load resistance, is the parallel combination of $R_{FB}$ and $R_L$; using this with equation (3-9) and rearranging terms gives

$$R_L = \frac{R_T\, G_p'}{(G_p' - 1)} \tag{3-10}$$

and

$$R_{FB} = R_T G'_p. \tag{3-11}$$

Using equations (3-10) and (3-11), the values of $R_{FB}$ and $R_L$ can be determined. The use of a $G'_p$ of one-third to one-half the value determined from equation (3-4) should provide an adequate feedback power safety factor.

*Step 3.* The last step in the procedure is the determination of the required impedance transformation ratio of the feedback circuit. This is the ratio of $R_{FB}$ to $(R_{in} + R_e)$ or

$$\text{Required impedance transformation ratio} = \frac{R_{FB}}{(R_{in} + R_e)}. \tag{3-12}$$

There are several types of impedance transforming networks which can be used, e.g., a capacitive tap on the output tuned circuit, a pi network, or a transformer. The properties of specific networks are treated briefly with the discussion of particular oscillator circuits in Chapter 7. Detailed discussions of several feedback networks are given in references 31, 32, and 35.

The power gain approach to the design of crystal oscillators is one of the few approaches simple enough to be of practical value. Accuracy is only fair and the difference from actual oscillator loop gain normally will not exceed 2 or 3. Also, a considerable amount of component value adjusting usually is necessary to get the crystal to operate on frequency. The approach is of the most value in designing oscillators of high frequency and high output power.

In general, the $Y$-parameter approach is a better design method for low-power oscillators. (If, however, the $Y$-parameters of a transistor are not known, or if from other considerations the reader elects to use the power gain method, it is suggested that reference 31 be consulted, since only the principles of this approach have been outlined here, and a detailed explanation of each step is given in the reference.)

## 3.4. NONLINEAR MODIFICATIONS

The small-signal analysis discussed in section 3.2 is valid until the ac base-to-emitter voltage builds up to about 10 mV. For values greater than this, significant changes occur in the forward transconductance as well as the input and output impedances. The magnitude of these changes is derived in Appendix G for the basic transistor and in Appendix H for a transistor with emitter degeneration. If the initial loop gain determined by $g_f$ (transistor)/$g_f$ (required) is calculated, the result can then be used to predict the base-to-emitter voltage, the input and output impedances, the harmonic current, and the bias shift. The curves of Figure 3-6 illustrate the method.

Suppose that the initial loop gain is 3. After the amplitude of oscillation has built up to its equilibrium value, the actual loop gain will be unity. Therefore the ratio $g_m/g_{m0}$ must be 0.333. From Figure 3-6 we see that $V$, the normalized ac base-to-emitter voltage, will be 5.7. The actual base voltage is then 5.7 $KT/q$ where

$K$ = Boltzman's constant, $1.38 \times 10^{-23}$ J/°K;
$q$ = electron charge, $1.602 \times 10^{-19}$ C; and
$T$ = temperature in °K.

At room temperature $KT/q \doteq 26$ mV; therefore, the actual voltage is $5.7 \times 26 = 148.2$ mV.

Once the base voltage is known, it is normally fairly straightforward to calculate the voltage in any other part of the circuit.

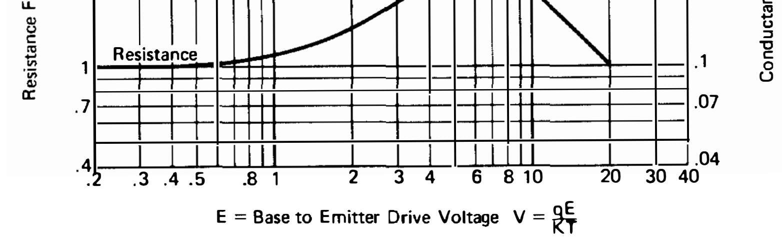


**Figure 3-6. Transistor parameters versus signal voltage.**

It should be noted that the input capacitance is reduced by the same ratio as the small-signal loop gain, which results in a slight increase in frequency.

Curves showing the harmonic currents as well as the bias shift are presented in Chapter 6. They may be useful in predicting the performance of the oscillator if a harmonic of the fundamental frequency is used.

Specific nonlinear equations, based on the principle of harmonic balance, are also derived for the Colpitts oscillator in Appendix I, and the results are presented in section 7.3.