Nano Magnetics
for Data Applications

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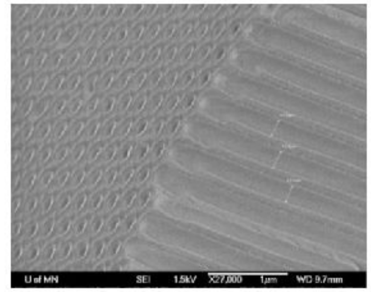
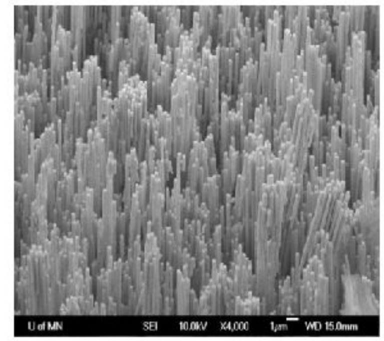
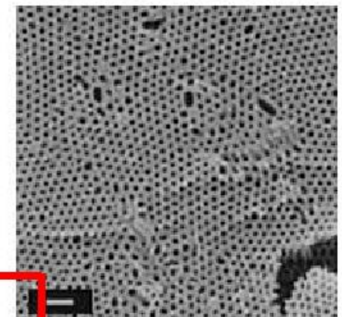
Applications

- § Recording
  - Read Sensors
  - Bit patterned media (BPM)
- § Random Access Memory (RAM)
- § Cilia (NEMS)
- § Biomagnetics







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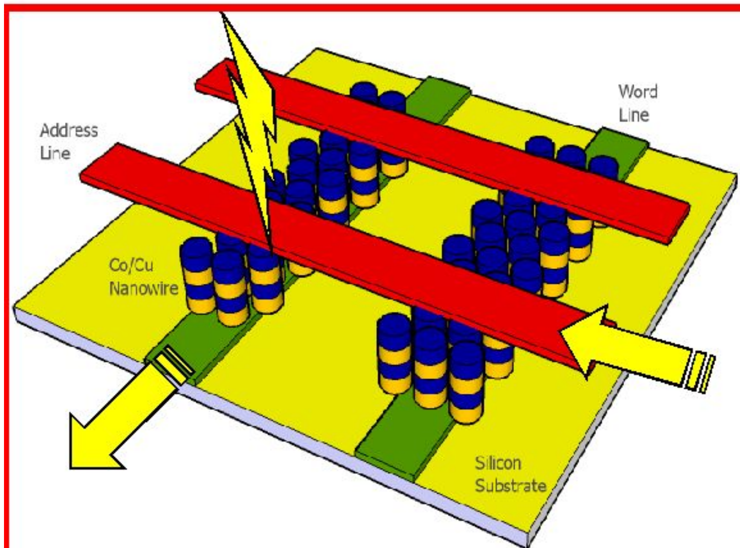
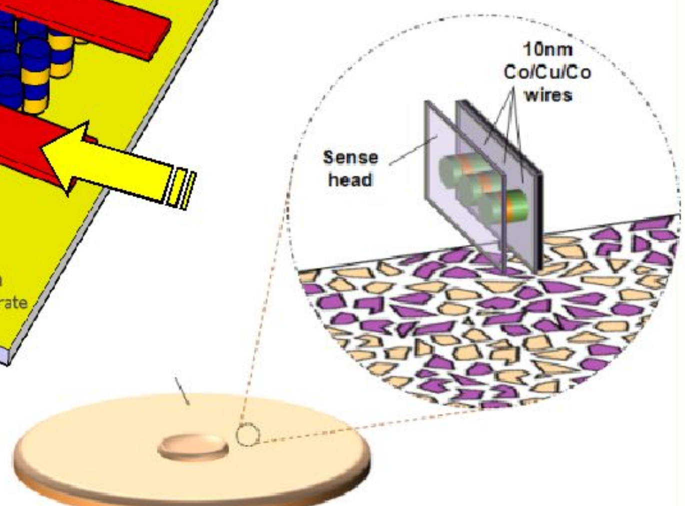
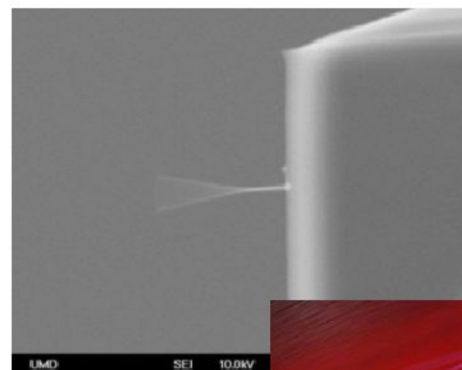
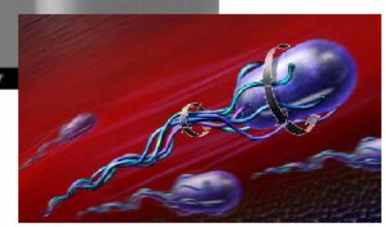








Outine

- Motivation: Memory Applications
    - Hard drives: media and heads
    - Random Access Memories

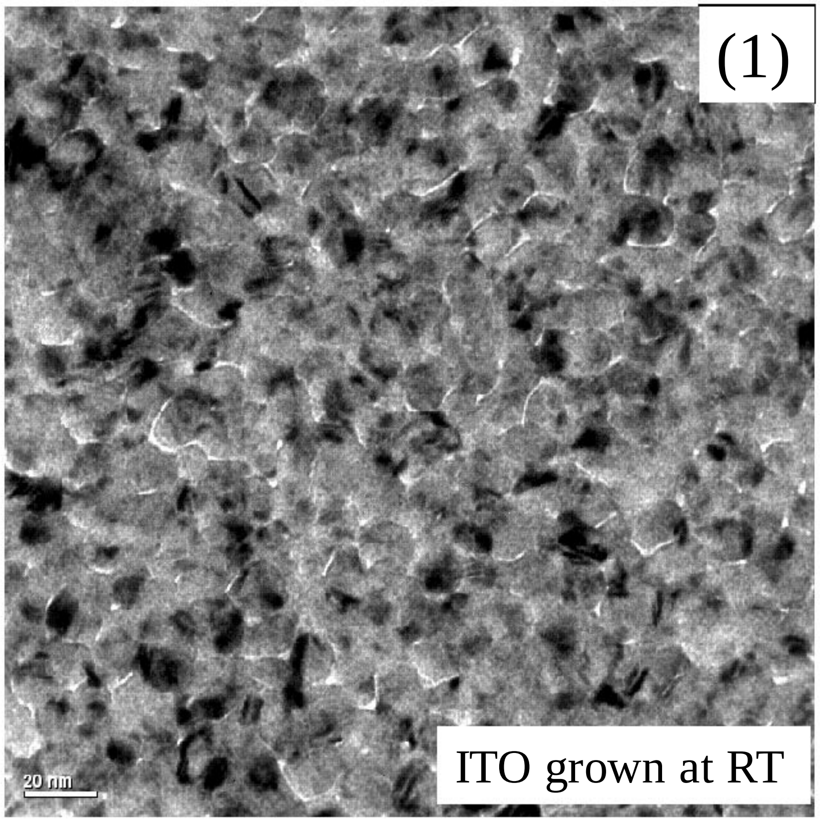
- Fabrication Techniques

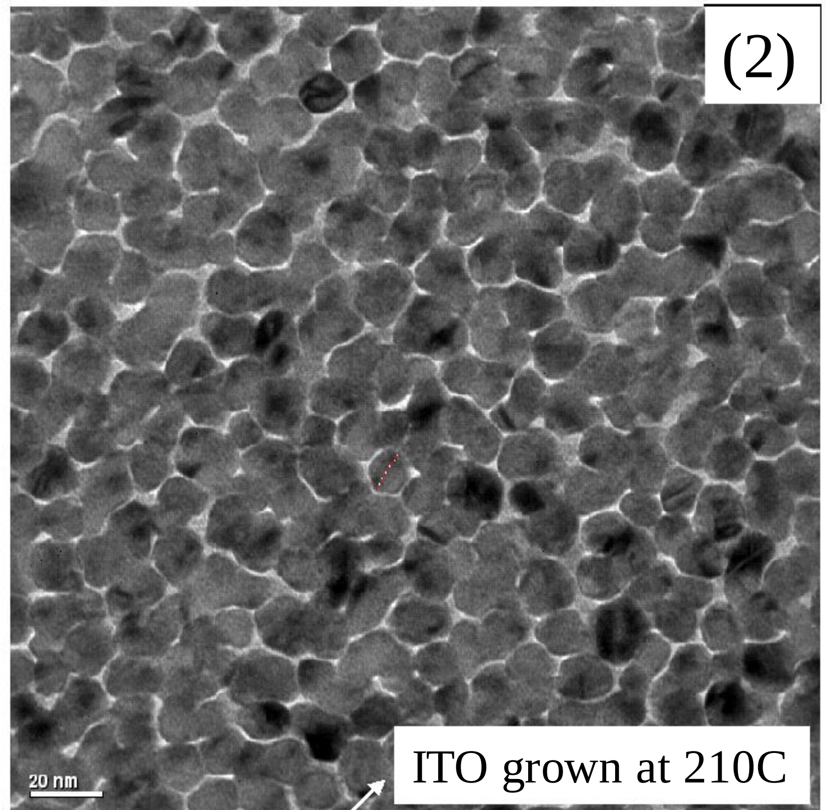
- Measuring Magnetoresistive Elements

Which media is better?

Neal Speetzen- ‘06

ITO(2nm)/Pd(2nm)/13x[Co(0.26nm)/Pd(1.05nm)]





- Smaller grains (each like a nano-sized bar magnet)
- Not coupled (if one switches, the ones around it won’t)
- Bits can have smooth edges (better recording and reading)

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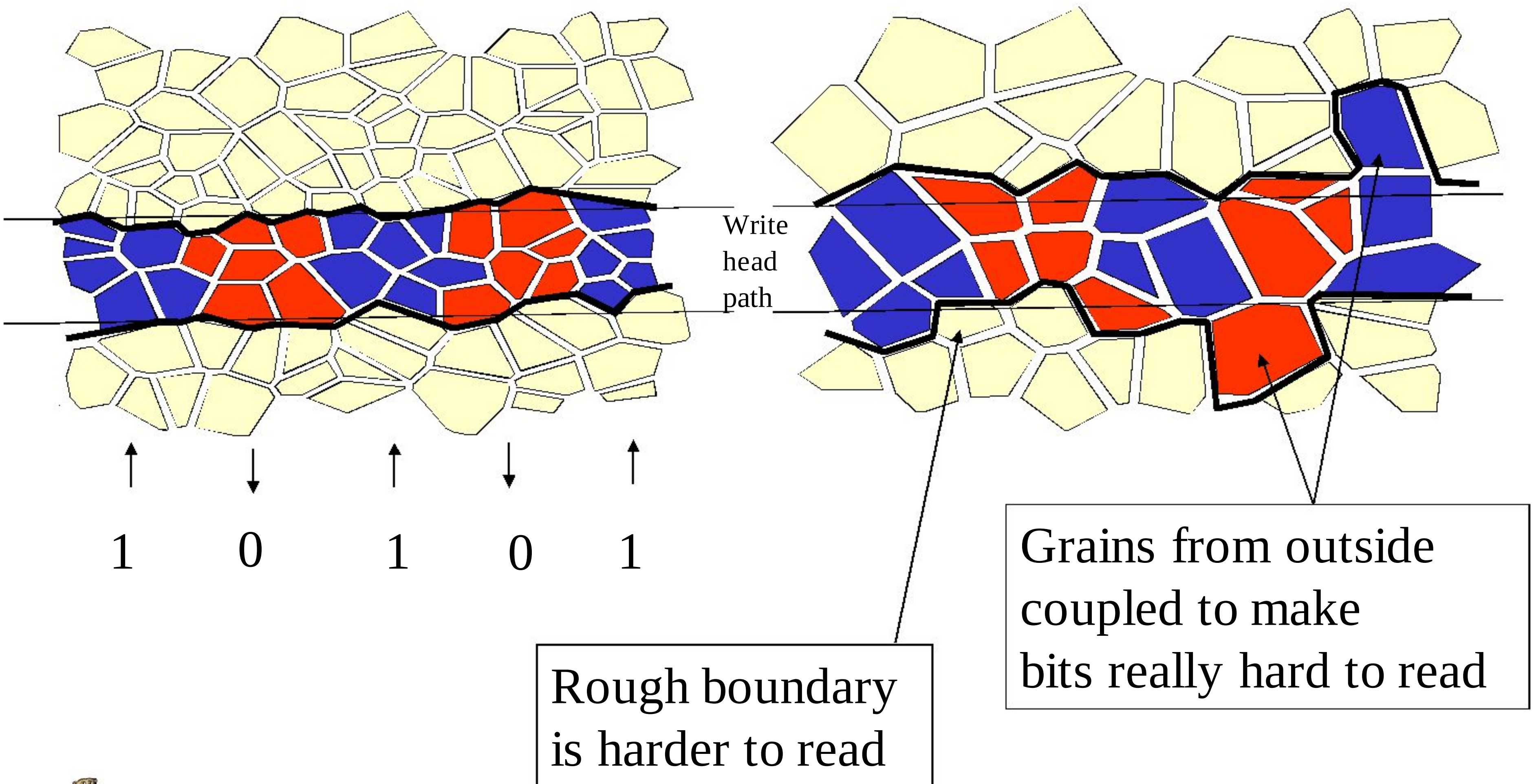
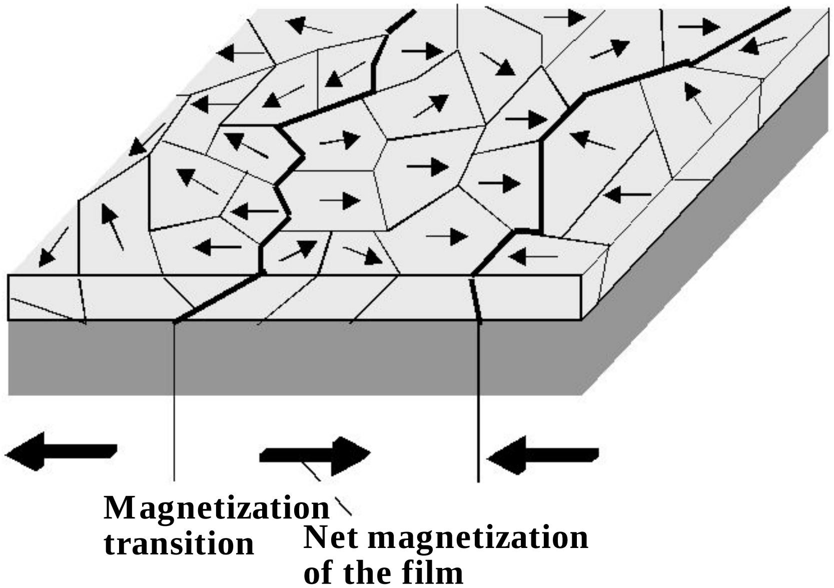
Now which is better?



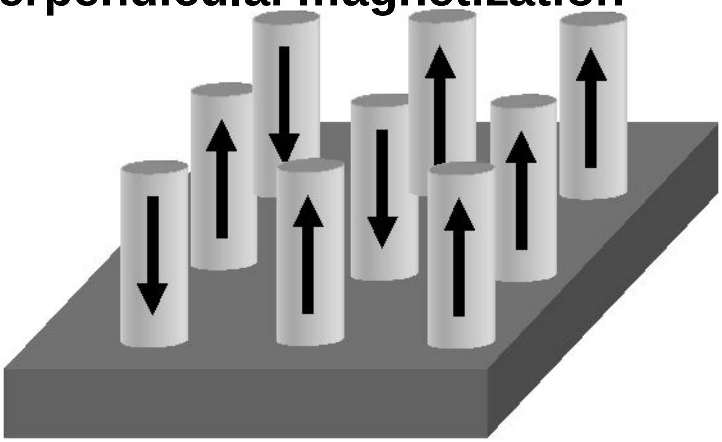
Voronoi structure from Randy Victora

Patterned media may be needed in future

Conventional magnetic thin-film medium

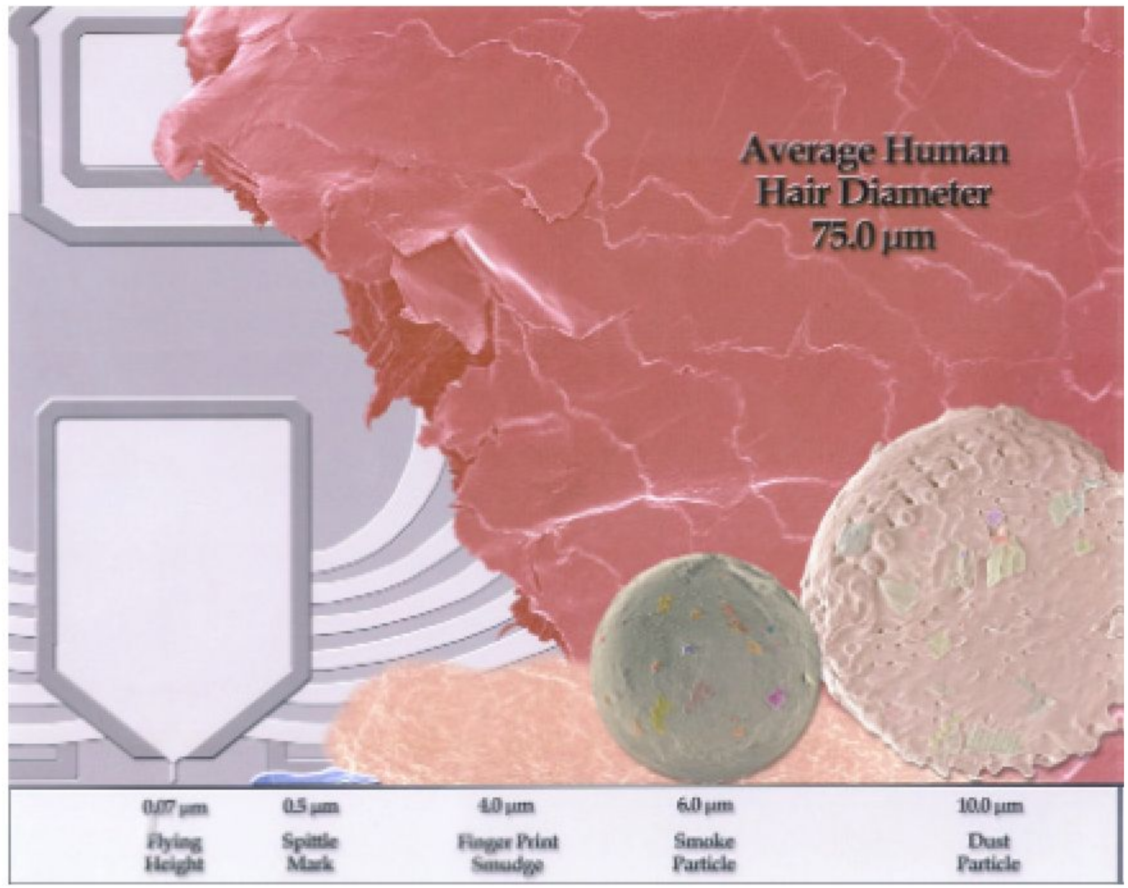


Patterned magnetic medium with perpendicular magnetization



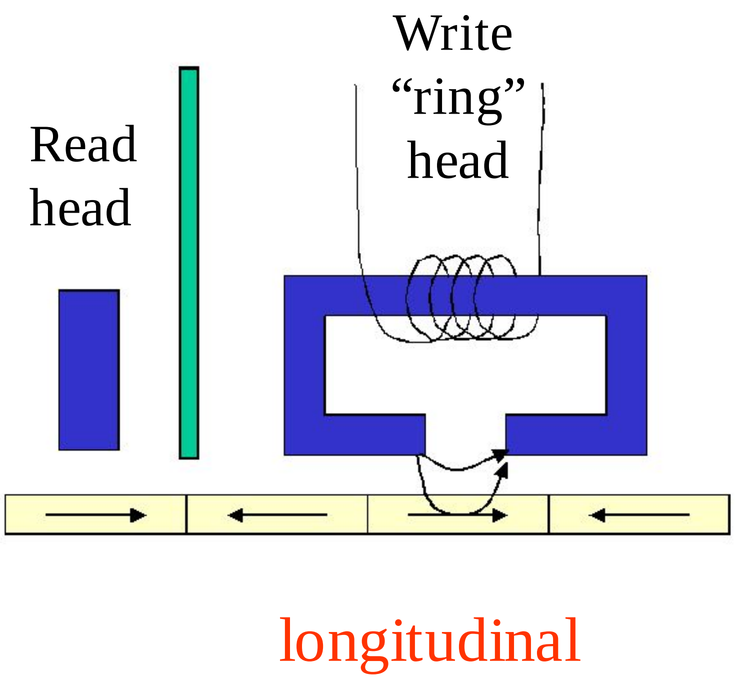
Recording Trilemma

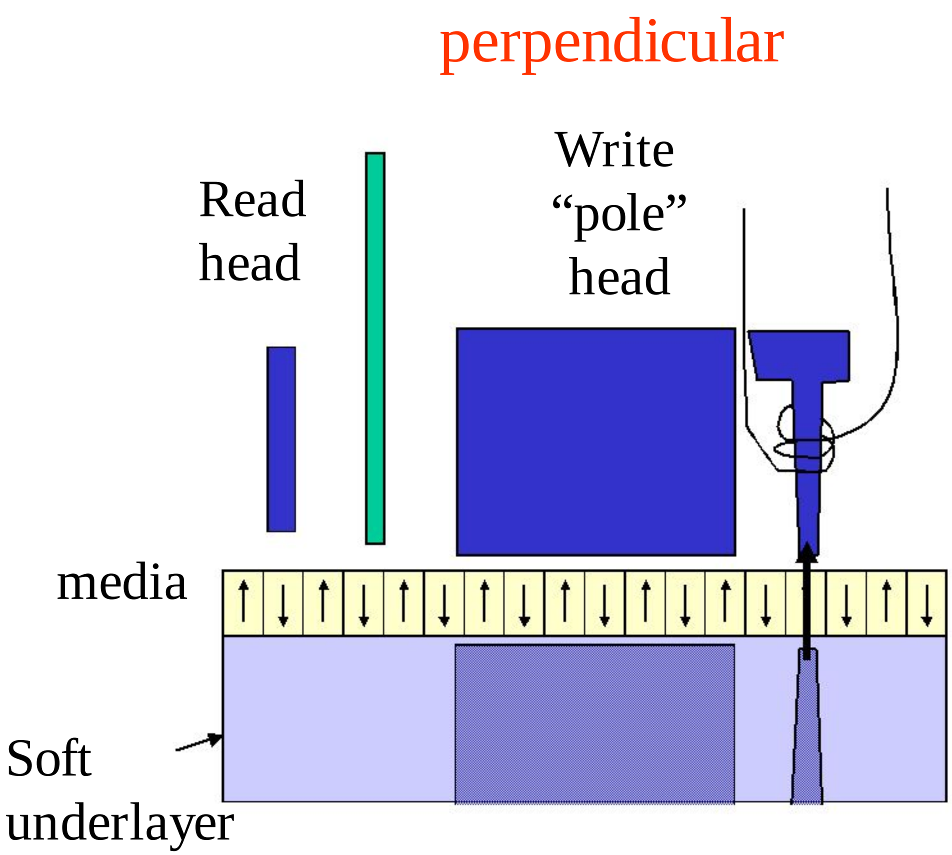
- **Thermal stabilty= K_uV/kT**
- **Coercivity must go up if volume is to go down**
- **But, then hard to write**



Seagate.com

Hard Drives

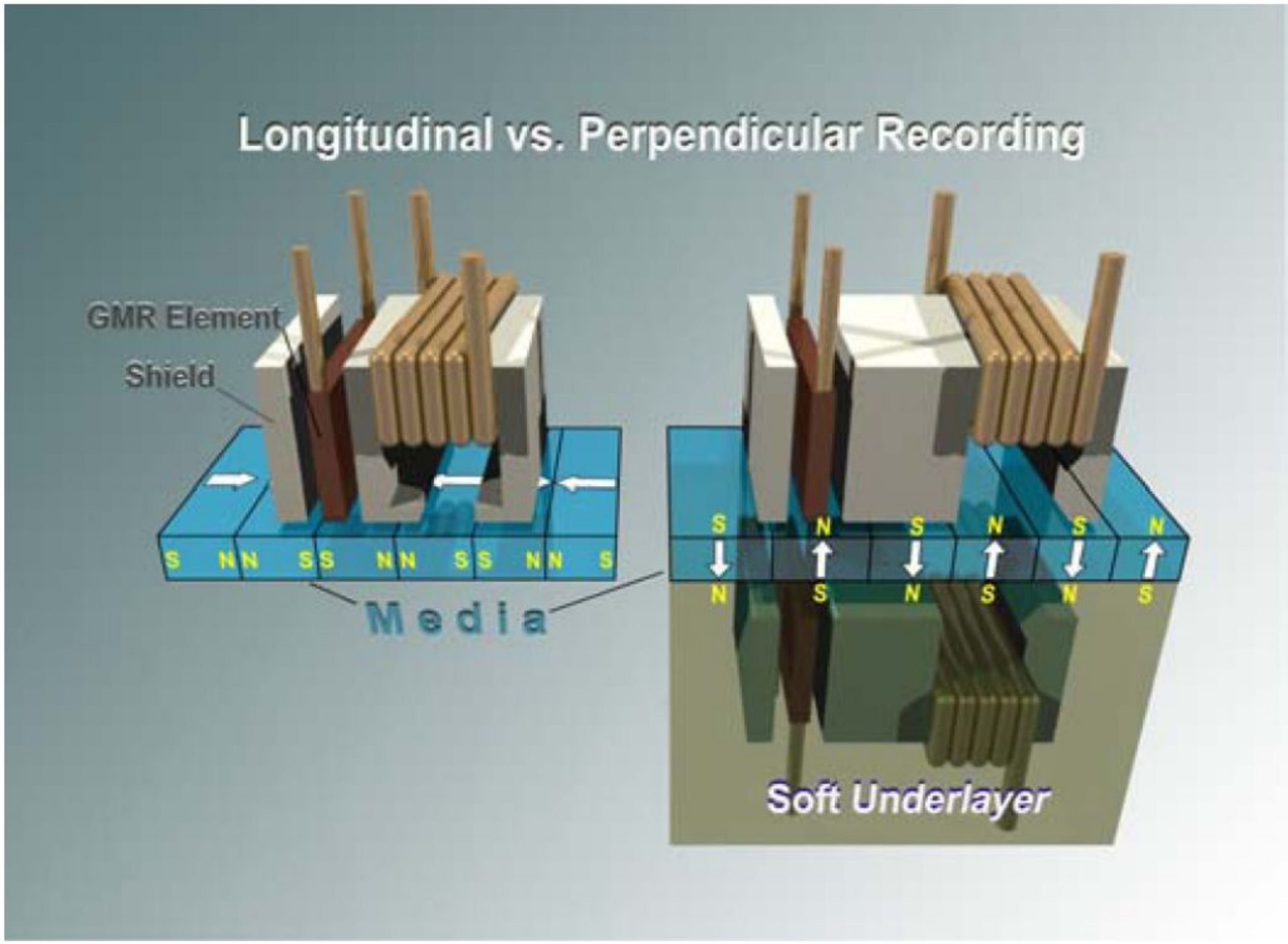




Perpendicular recording media has replaced longitudinal media because the bits can be smaller (in surface area) while maintaining volume, which keeps bits from decaying

http://www.hitachigst.com/hdd/research/recording_head/pr/PerpendicularAnimation.html

Longitudinal vs Perpendicular



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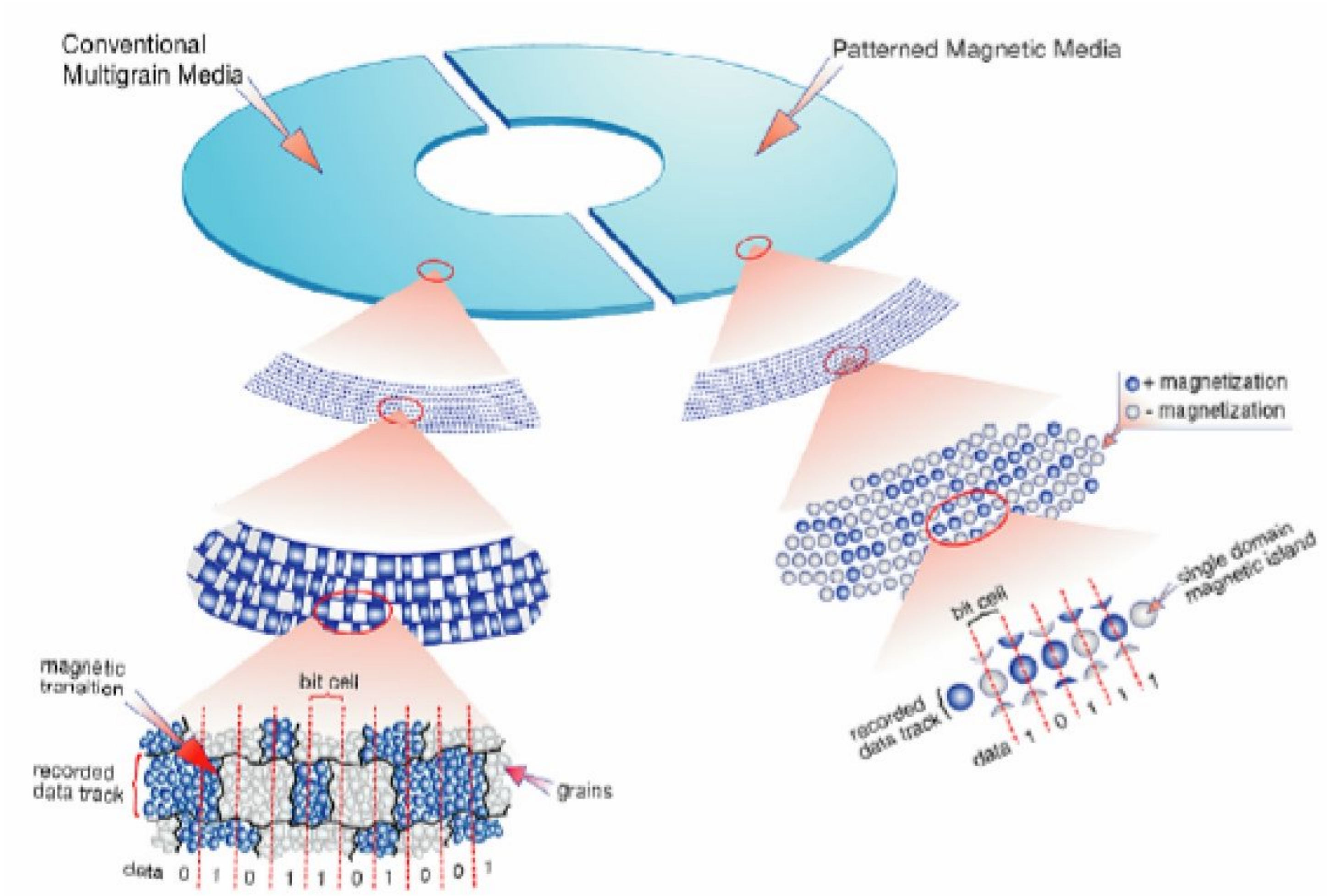
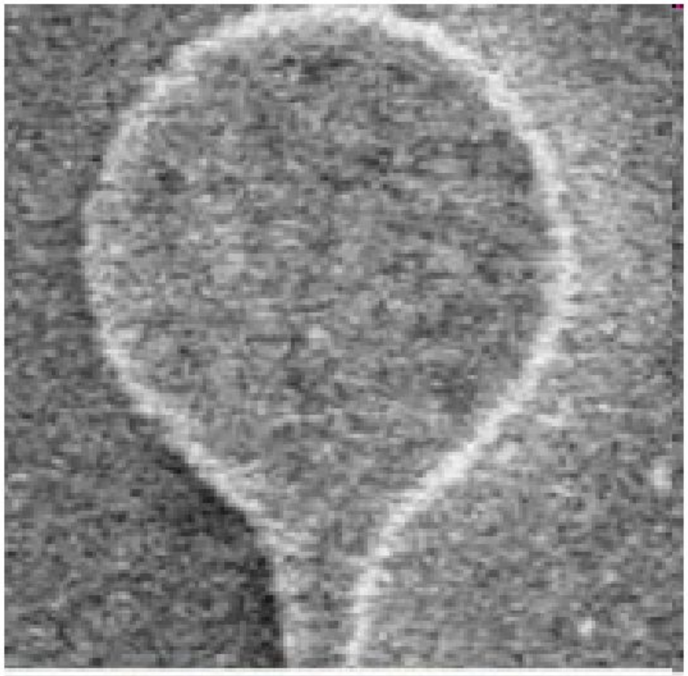
Conventional Media vs. Patterned Media

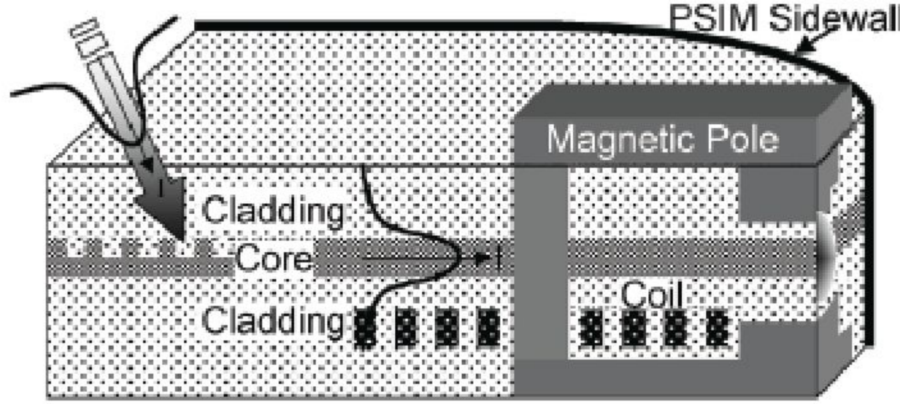
HITACHI
Inspire the Next



Write Heads

Heat-Assisted Magnetic Recording (HAMR)





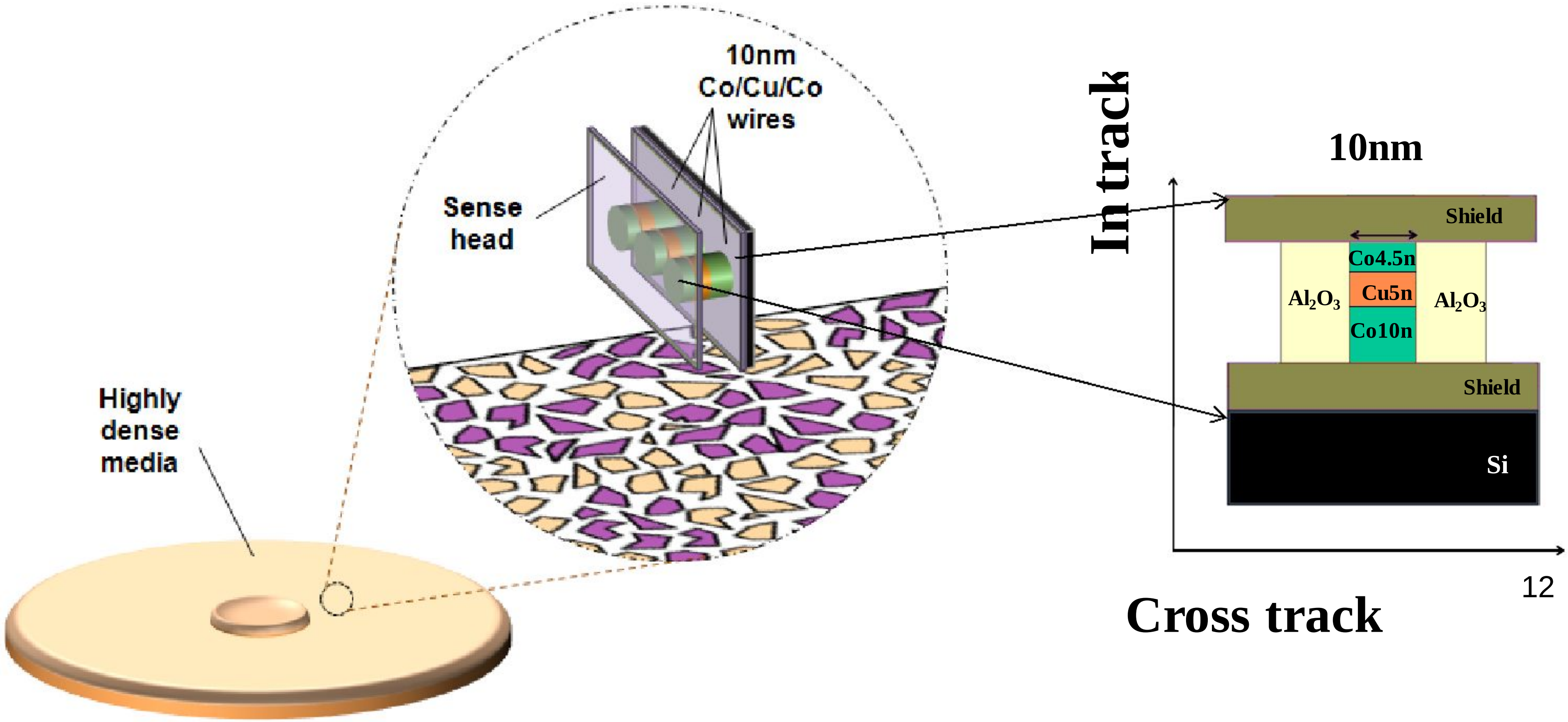
(a)

Seigler et al IEEE-MAG 08

MIT Tech Review

Read Heads

Typically one per slider, but arrays would help 2D MR



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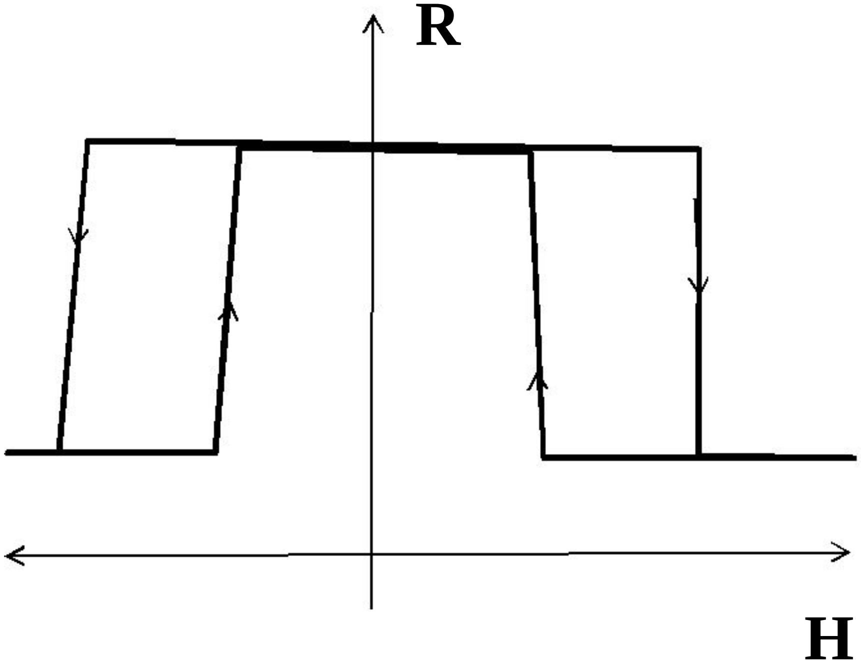
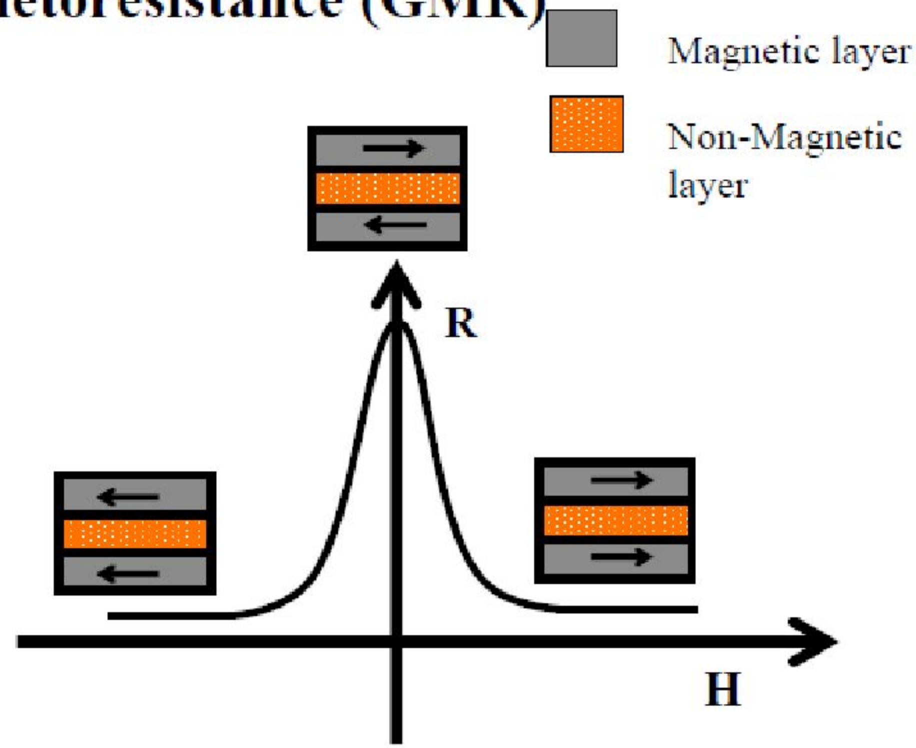
Stadler et al IEEE Transactions on Magnetics (2012). **DOI: 10.1109/TMAG.2011.2174975**

------Giant Magnetoresistance (GMR)

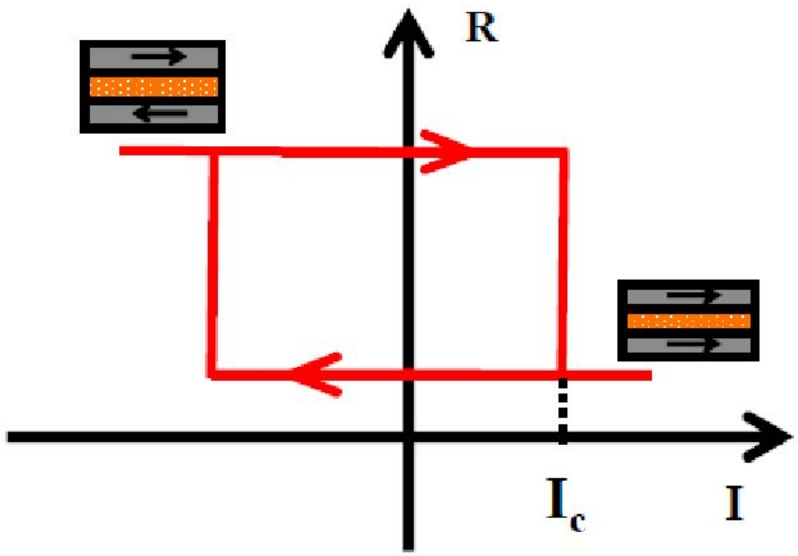


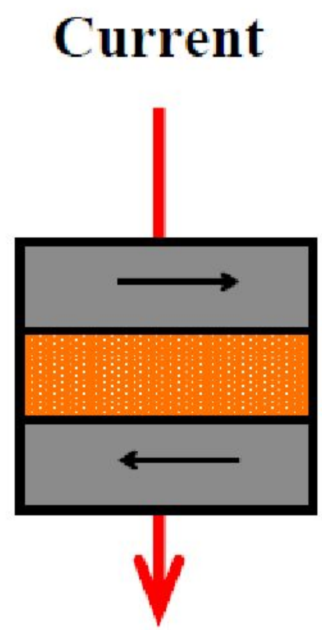


$$GMR(H) = \frac{R(H) - R_{Sat}}{R_{Sat}}$$

The change of resistance of a conductor in an external magnetic field.

----Spin Transfer Torque (STT)





Switching current ,I_c is about $10^7 A/cm^2$

TMR vs GMR

- ***Tunneling*** magnetoresistive (TMR) sensors
  - Good for today: bits ~15 nm x 75 nm
  - Magnetoresistances: MR = ? R_{magnet}/R ~ 70%.
  - Integration prefer resistances (R) below 300 O
  - Resistance-area (RA) must continuously decrease <<1 ? .µm^2
    - signal-to-noise ratios (SNR)
    - RC time
    - Heat dissipation to reduce stochastic shot noise as areas decrease

- Current perpendicular to the plane ***giant*** magnetoresistive (CPP GMR) sensors
  - calculated to have high signal to noise ratios
  - nanoparticle BPM densities (1-10 Tb/in^2)
  - head sizes below 40 nm

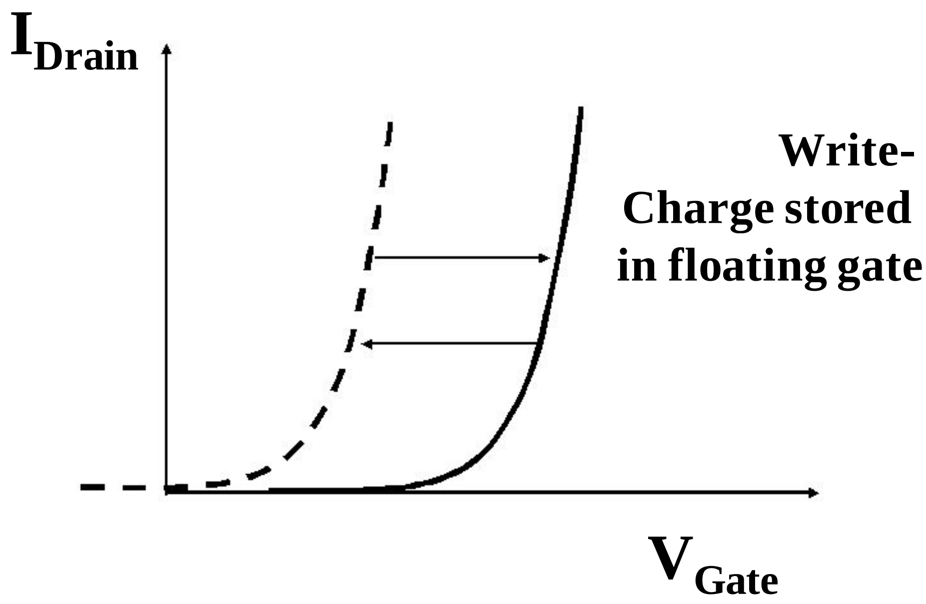
Random Access Memory (RAM)

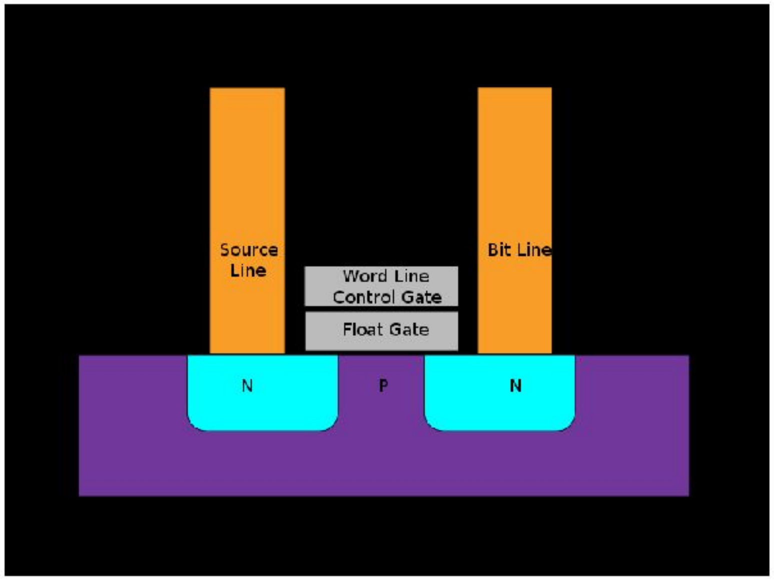
Meet the Competition…

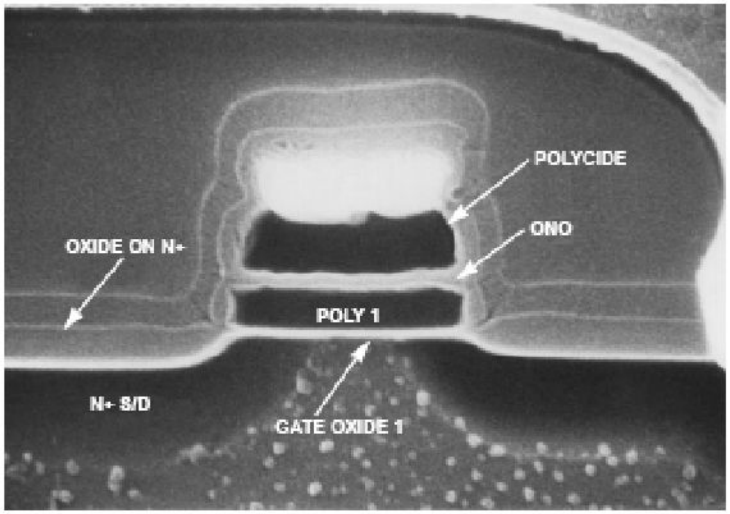
Note: good review in recent ***MRS Bulletin***

Flash

- Flash = EPROM but erase in blocks (in a "flash")
- EEPROM erases individual bits, but slow and 2 transistors are required





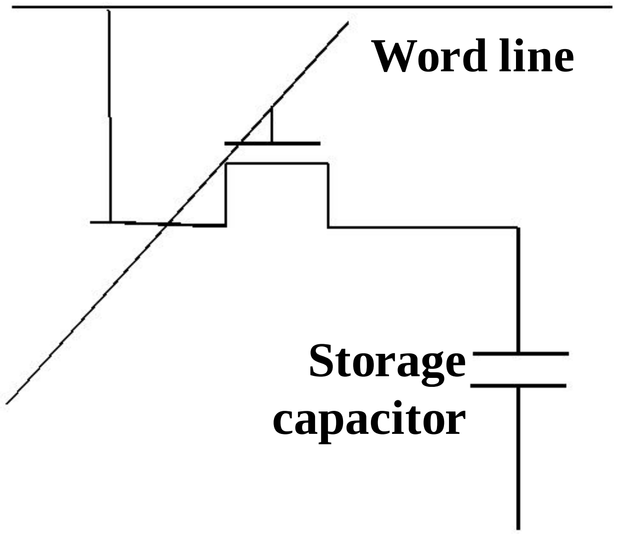


FLASH MEMORY CELL

Photos by ICE, "Memory 1997" 22482

DRAM (dynamic)

- Charge stored in a capacitor



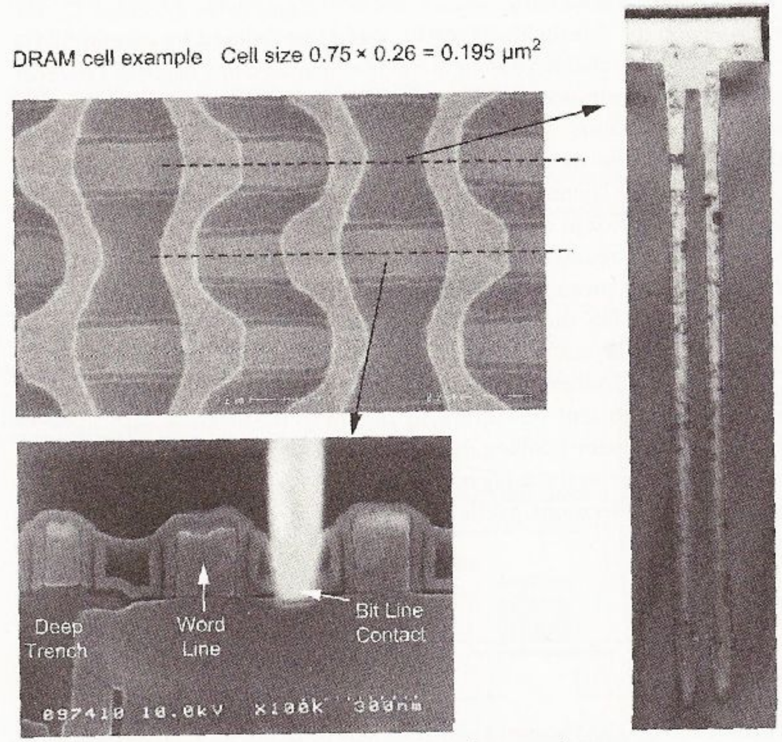


Figure 12.3 Trench capacitor cell. This has a 8 μm-deep trench capacitor and a sidewall storage-node contact for enough storage capacitance and small contact within a small area. (After Yamada, VLSI Tech. Short Course 2003 and Ref. [3]).

Ferro-electric (FeRAM)

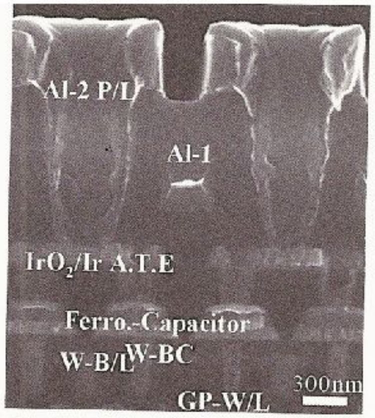


Figure 13.14 A vertical scanning electron microscopy image of the FRAM cell.

carried out. Due to technical difficulties in realizing a ferroelectric film with low thermal budget processes, and of identifying a suitable oxidation barrier metal which is stable above 600 °C, the early FRAMs were developed with a CUB cell structure, thereby sacrificing cell size efficiency.

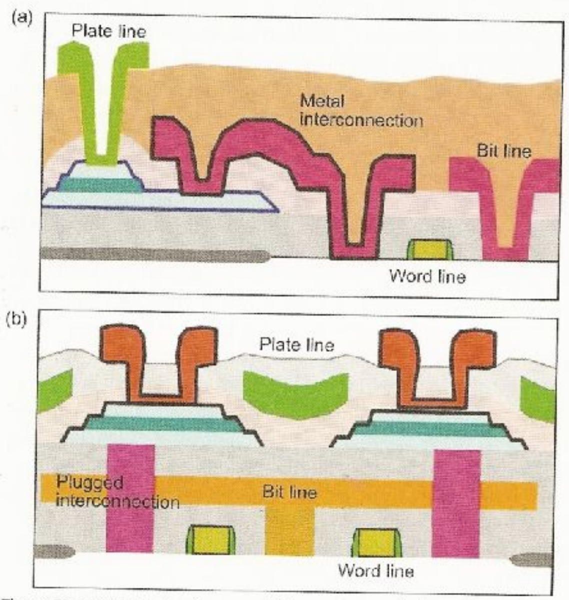
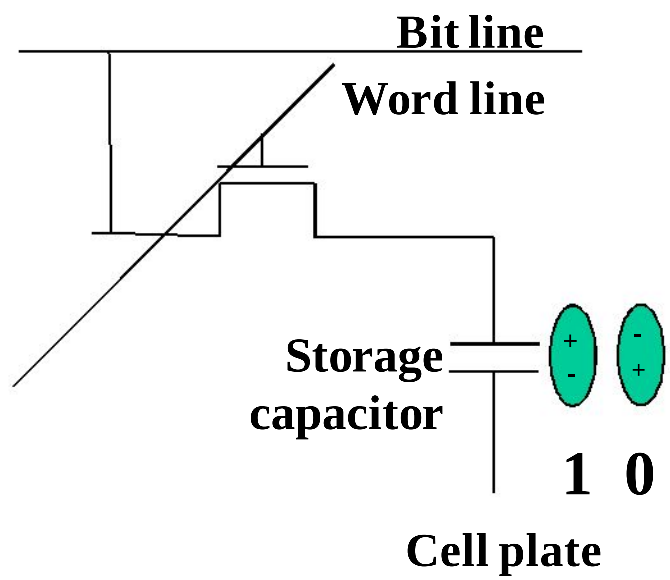


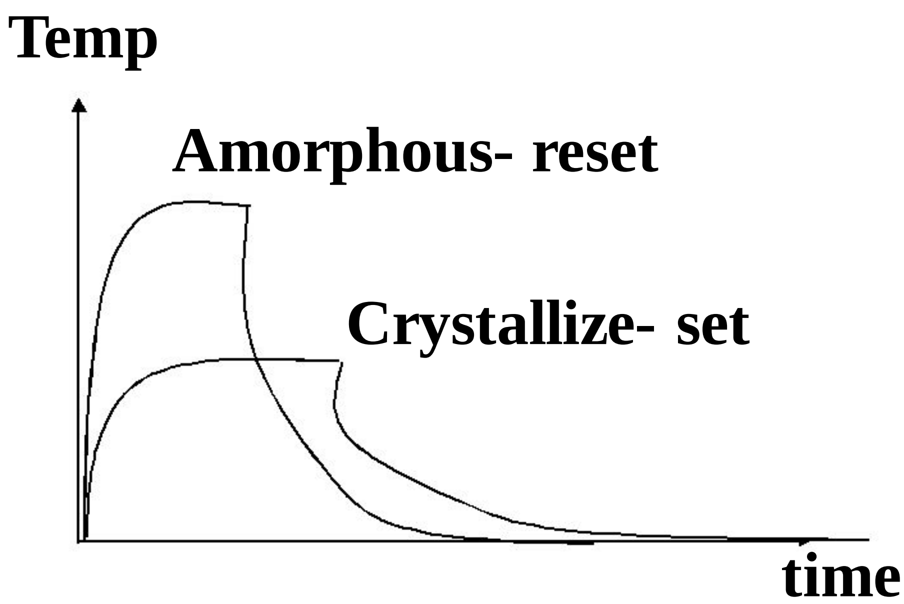
Figure 13.15 Schematic diagram of (a) capacitor under bit line (CUB) and (b) capacitor over bit line (COB) cell structures.

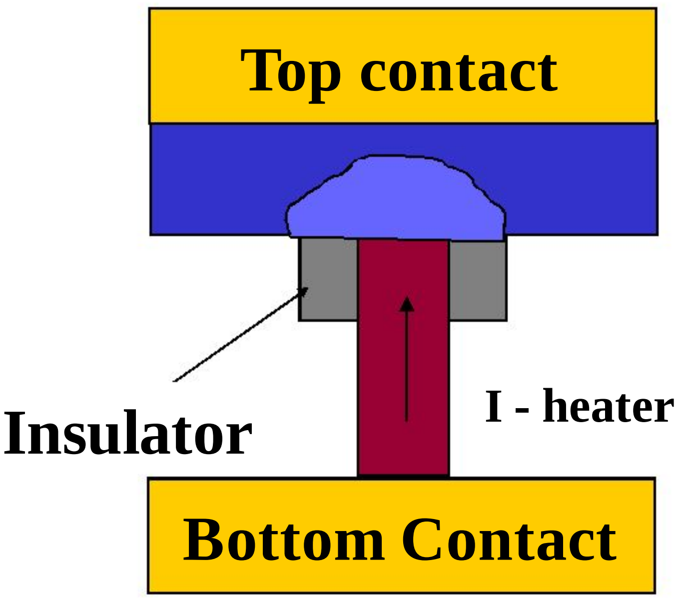
- Non-volatile DRAM
- Non-volatile capacitor



Nanotechnology: Information Technology I (Ed. Waser)

Phase Change Memories

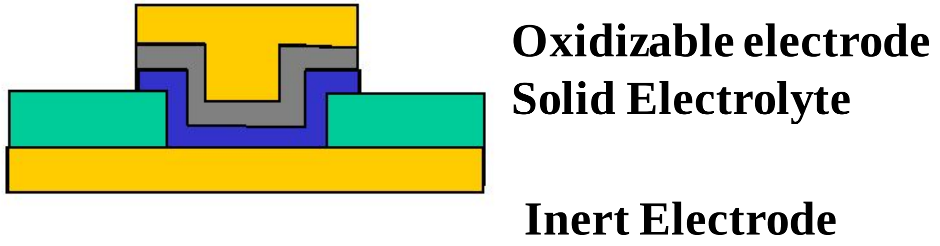




Three orders of magnitude difference in R (cm crystalline, m   cm amorphous)

Solid Electrolyte Memory

- Anode: Ag -> Ag^{+} + e^{-}
- Cathode: Ag^{+} + e^{-} -> Ag
- Metal electrodeposits across electrolyte in “snakes”
- Or redissolves with opposite polarity



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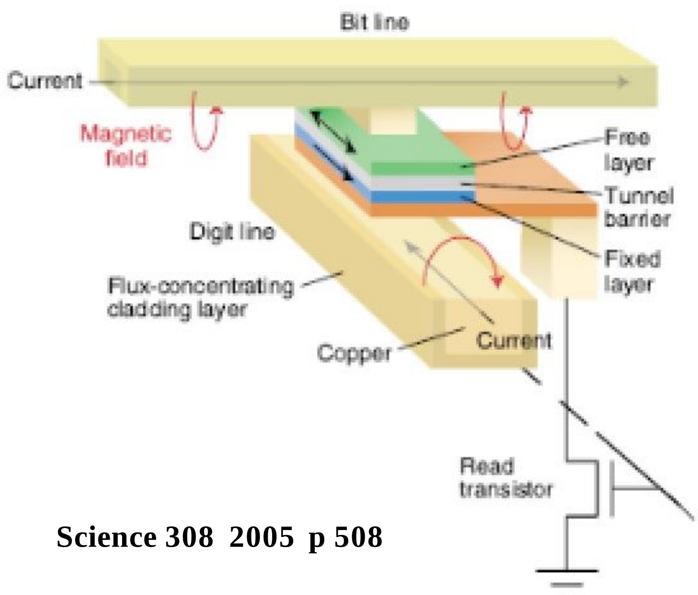
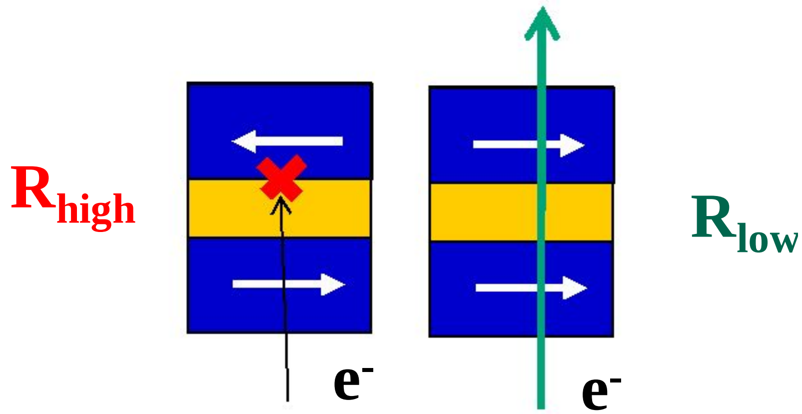
Back to Nano Magnetics…..

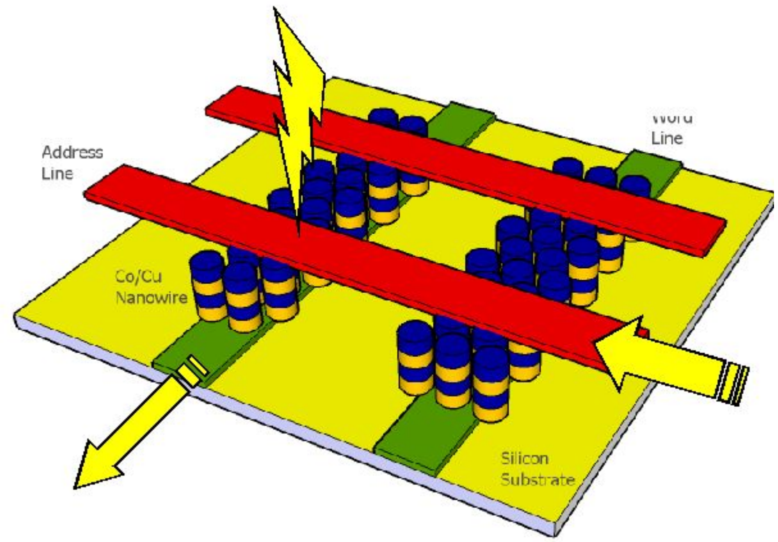
Magnetic (MRAM)

Magnetic field used to switch 1 ? 0



Science 308 2005 p 508





1 ? 0

Spin Transfer Torque (STT RAM)

Simpler structure to switch with current instead of field- also less likely to switch other elements accidentally

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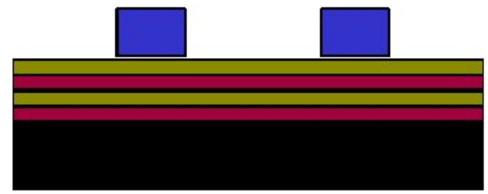
Outine

- Motivation: Memory Applications
  - Hard drives: media and heads
  - Random Access Memories
- Fabrication Techniques
- Measuring Magnetoresistive Elements
- Conclusions

-------Nanostructures by Top-down Technique

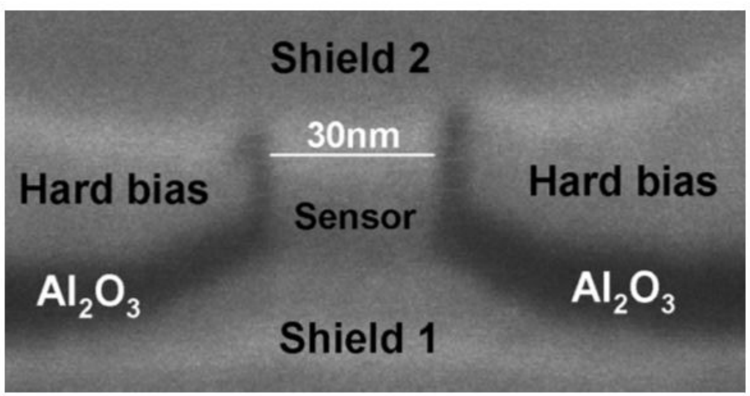
- Good interface
- High-cost and time-consuming
- Definition challenges as dimension scaling down

PVD



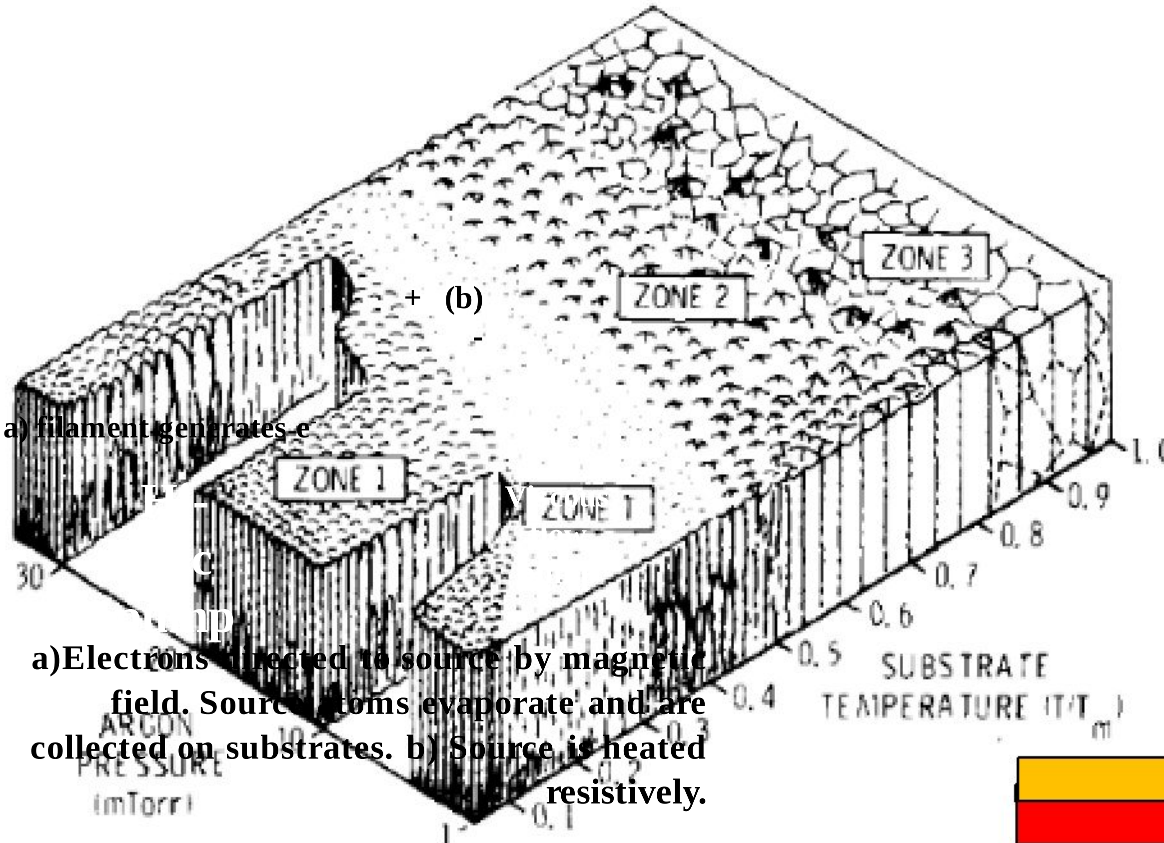
Lithography

RIE or Ion milling



Childress *et al* (2008)

Thin Film Growth (PVD)



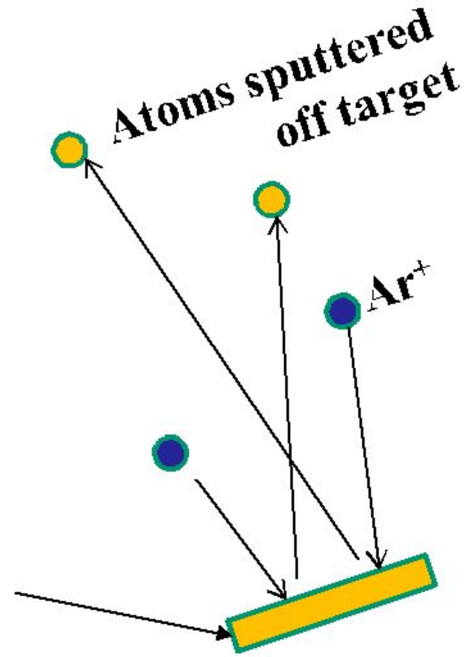
+ (b)

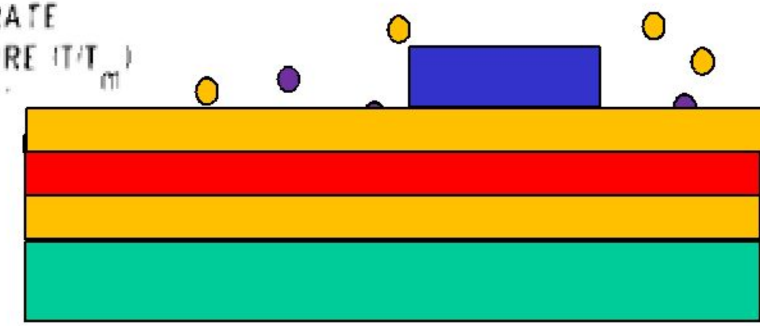
-

a) filament generates e

a)Electrons directed to source by magnetic field. Source atoms evaporate and are collected on substrates. b) Source is heated resistively.

Thorton Diagram

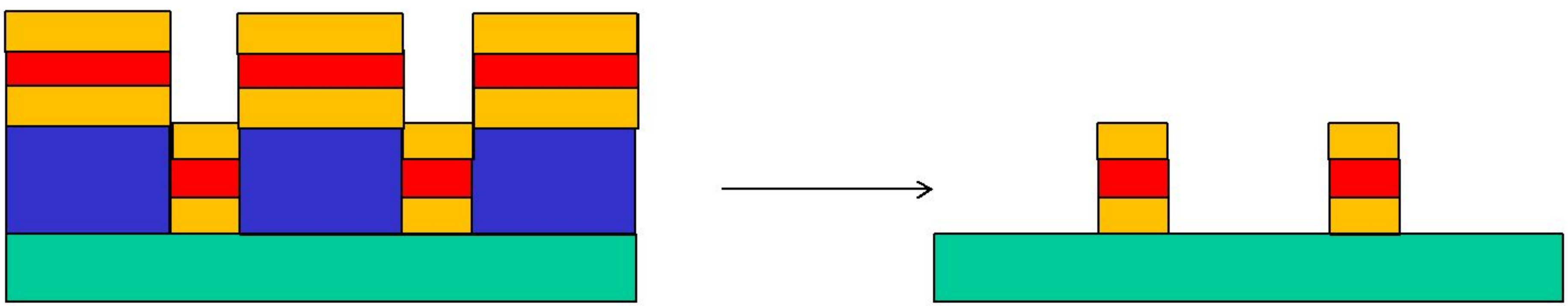




Ion mill film

Top Down- Lift off

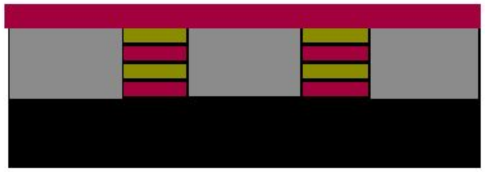
- Pattern resist first
- PVD thin films on top
- Etch resist so film “lifts off” where you don’t want it



Bottom up Nanofabrication

----Nanostructures by Templated Synthesis

Template with nanopores



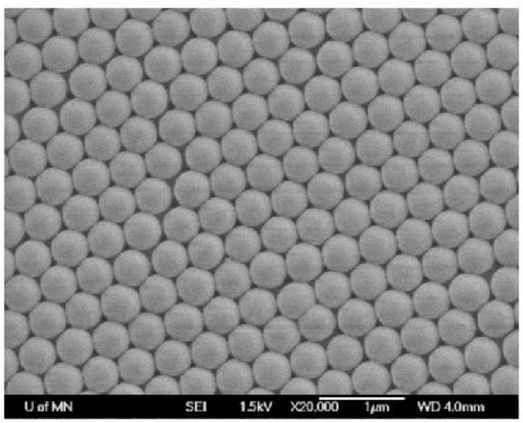
Nanowires deposition

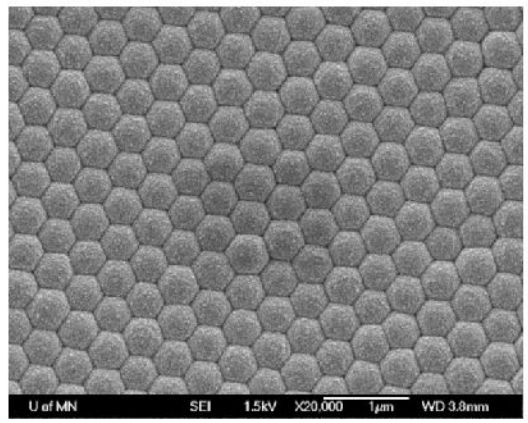
- Low-cost, high through-put and small diameters (~10nm)
- No edge-damage from patterning

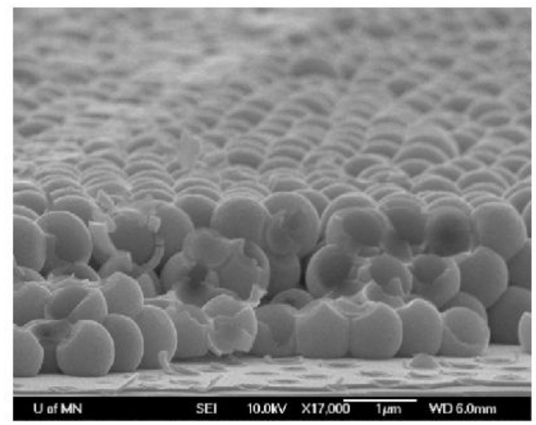
Much more on this later!

Nanoparticle Assembly

- Vacuum and liquid techniques available to make nanoparticles



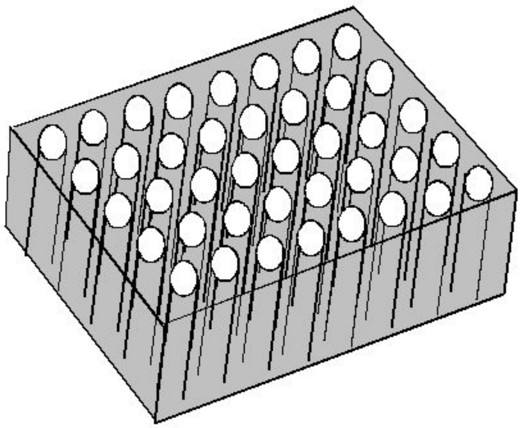




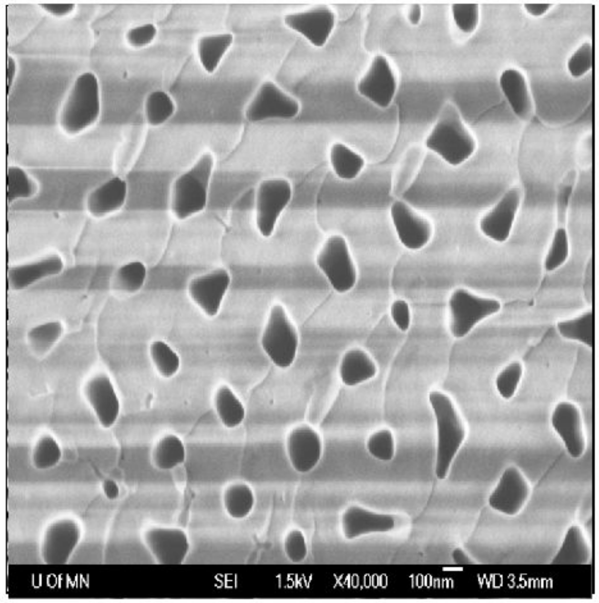
These are mico-particles, but see work for example by Sara Majetich at Carnegie Mellon University for nanoparticles

In all but last case…
masks/templates are needed

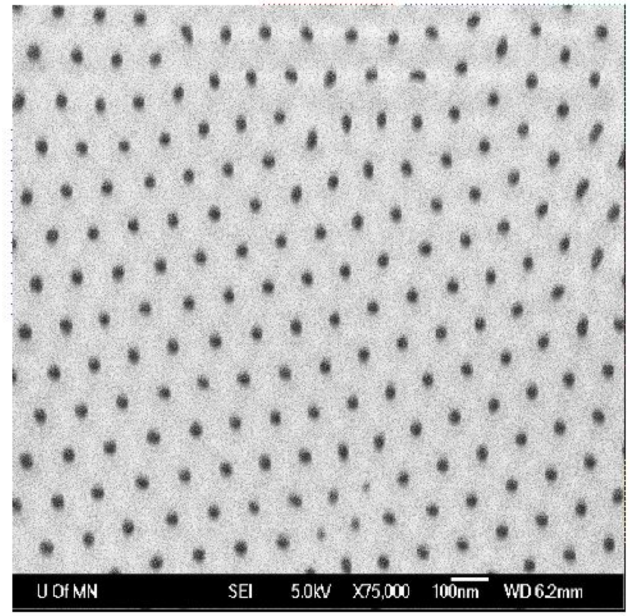
Anodic Alumina Templates- more later



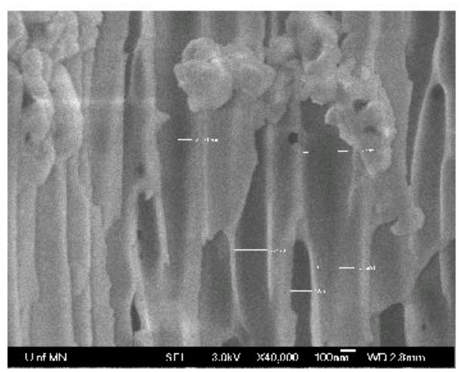
Side View

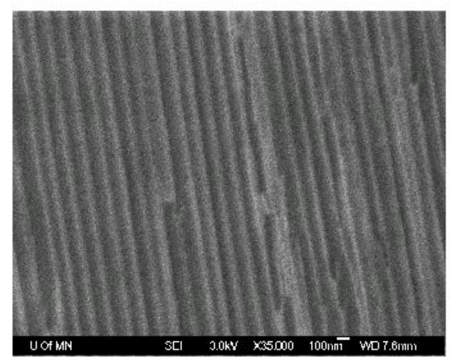


Commercially available alumina template-
- No homogeneity or order



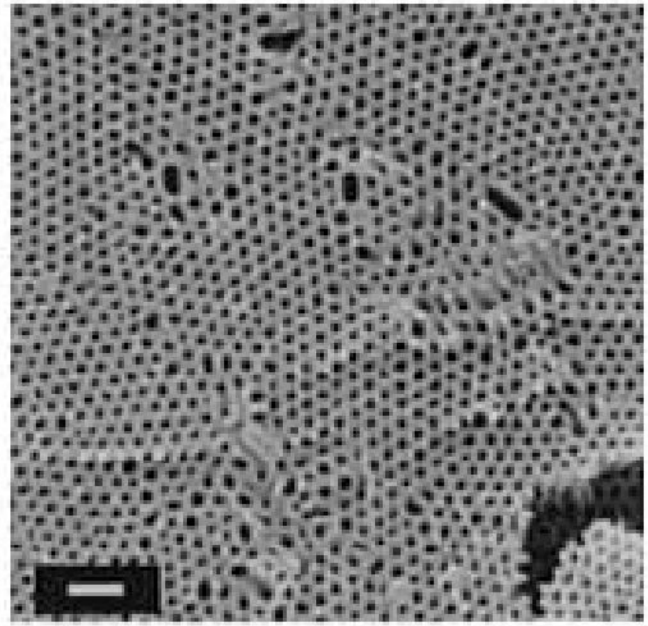
Alumina template from our lab-
- Homogeneity & short range order
- No long range order





Diblock Copolymers- Overview

- Advantages over anodic alumina
  - No barrier layer at the bottom of the as-formed pores
  - Ease of dissolution of the template to expose the wires
- Disadvantages:
  - limited range of possible diameters
    - 14-50 nm
  - competing interactions that make them more difficult to align completely perpendicular to the substrate



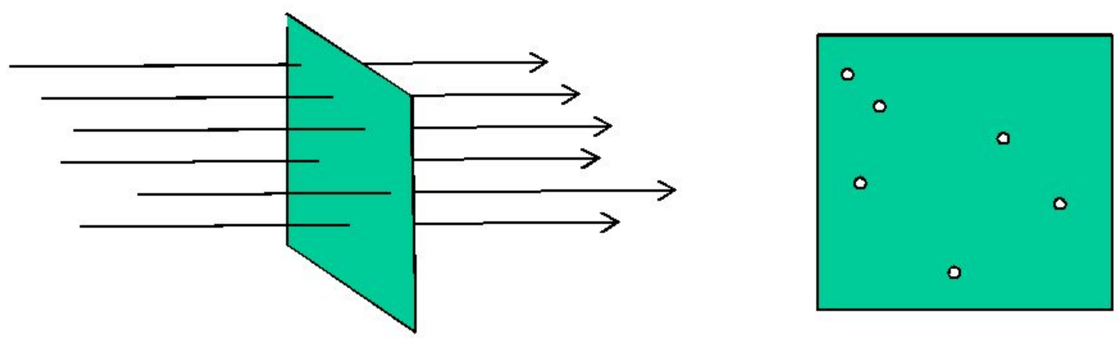
Scanning electron micrograph of a nanoporous block copolymer fracture surface. The PLA block of the PS-PLA copolymer has been degraded to leave behind nanoporous PS. (Marc Hillmyer)

www.nano.umn.edu/omni/research

Etched Ion-Track Polymers

- Advantages: smaller number, or lower density, of nanopores can be fabricated
  - Even down to a single nanopore
  - Measuring single wires possible with microscopic electrical contacts

- Ion-track templates made by irradiating polymer membranes
  - Usually polycarbonate 10-50um thick
  - Heavy ions, such as Ar, Xe, Au or Pb
  - Energies of 8-12 MeV/nucleon for single ion tracks
  - 0.2-2 GeV with fluences between 10^6 and 10^9 ions/cm^2 for multiple tracks
  - Tracks left by ions chemically etched in aqueous NaOH
  - Sometimes UV irradiated first
  - Make pores as small as 15nm



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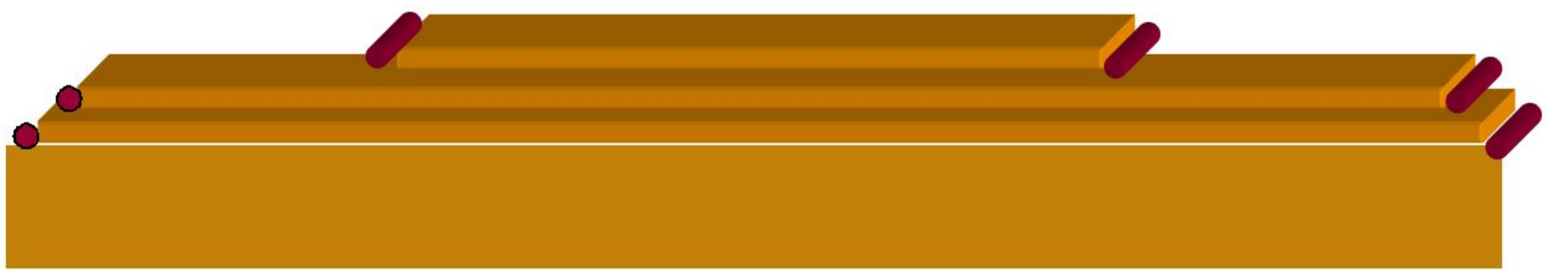
Nanowires Not Discussed Here (1)

- This talk will focus on inorganic nanowires
  - Metals (some ceramics,semiconductors) not carbon nanotubes

- Arrays are usually grown inside predefined pores of nanometer size
  - Usually grown via electrochemical deposition

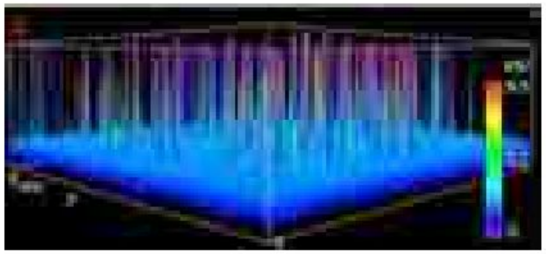
- Other techniques used for individual nanowires (Step Growth)
  - Uses steps on atomically rough substrate & chemical/physical vapor deposition
  - Essential trade-off is deposition rate versus surface diffusion rate
  - Growth morphology: stepped surface with nanowires located in the nook of each step
  - Mostly used for metallic nanowires- adatoms have fast surface diffusion coefficients



Nanowires Not Discussed Here (2)

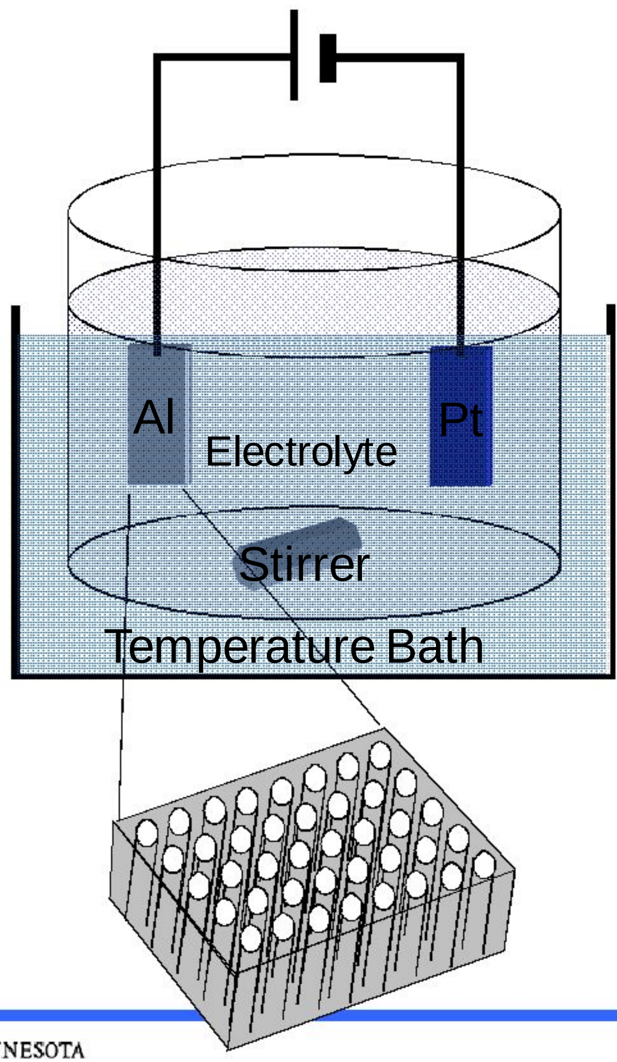
- Other techniques for arrays (VLS approach)
  - Vapor-liquid-solid technique
  - Liquid drops of catalyst are supersaturated with nanowire elements using vapor source
  - Solid wire then crystallizes out of the droplet onto the substrate
  - Vapor can be supplied via chemical vapor deposition, laser ablation, thermal evaporation
  - Mostly used to grow semiconductor nanowires due to solubility in liquid-metal catalysts

Björk *et al.*/*Nano Letters*



Zhong Lin Wang *et al*, *Science*

Anodization



Nanopores self assemble inside of an oxide film when the oxide is grown by anodizing metallic aluminum.

<u>Pore size (diameter)</u>

~ 150nm (anodized in phosphoric acid)

~ 50 nm (anodized in oxalic acid)

~ 20 nm (anodized in sulfuric acid)

<u>Aligned range</u>

~ 1~10 μm

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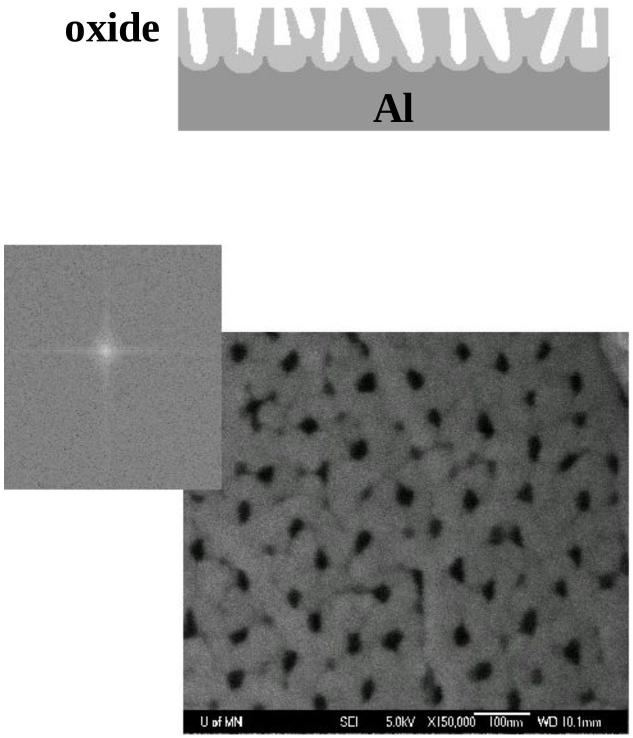
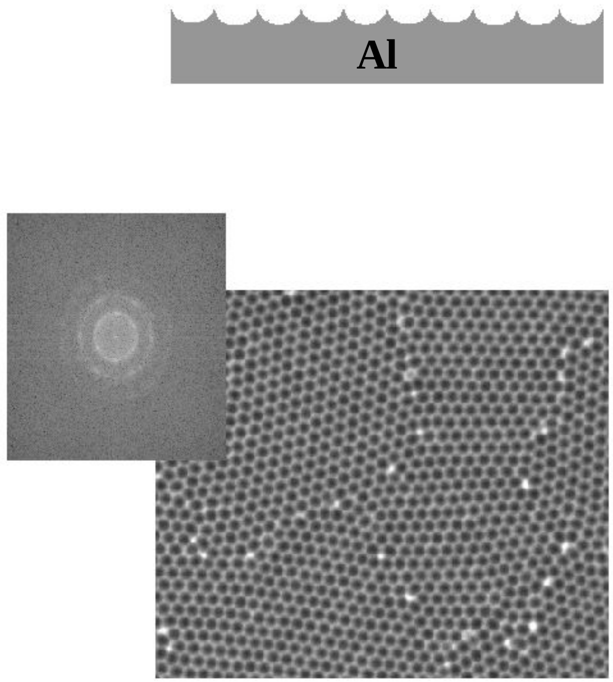
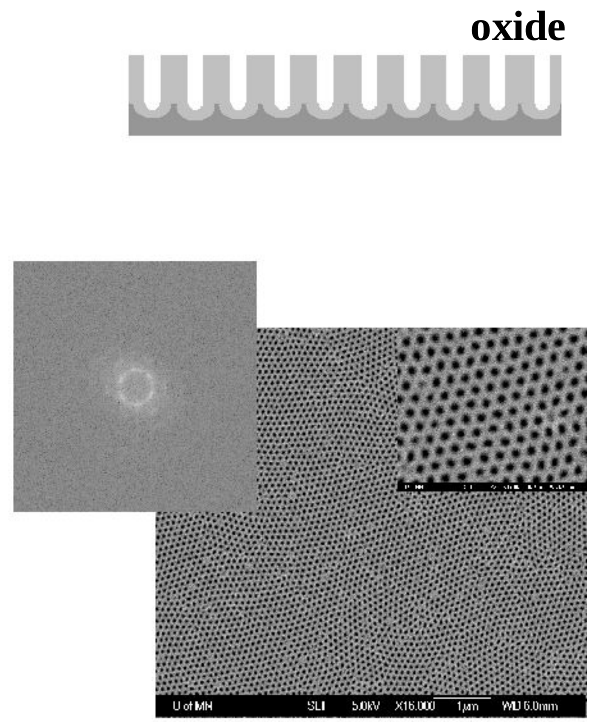
Two-step Nanoporous Anodic Alumina



(1) 1st Anodization



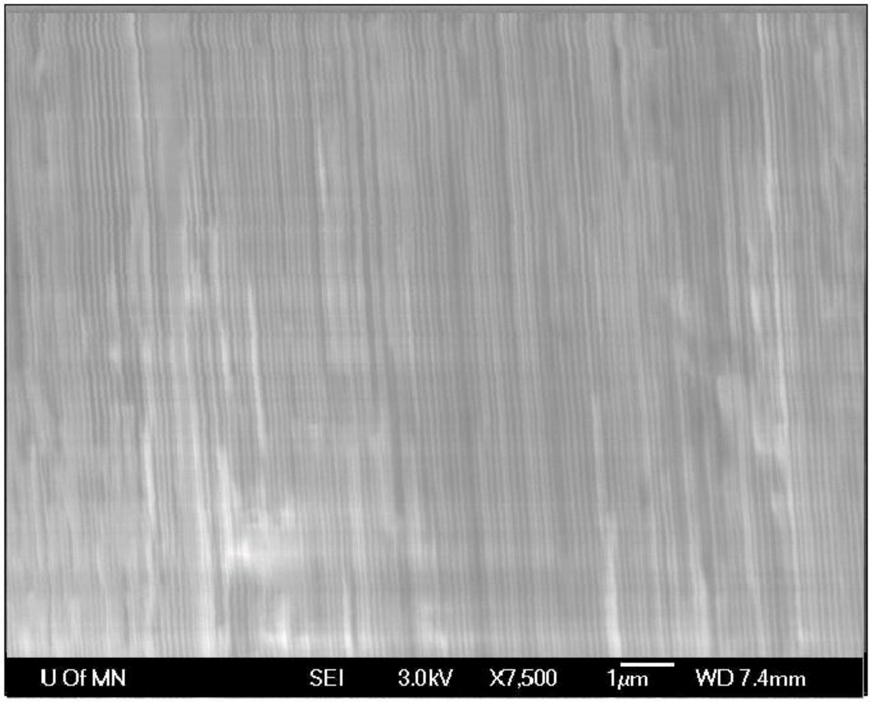
(2) Oxide Removal

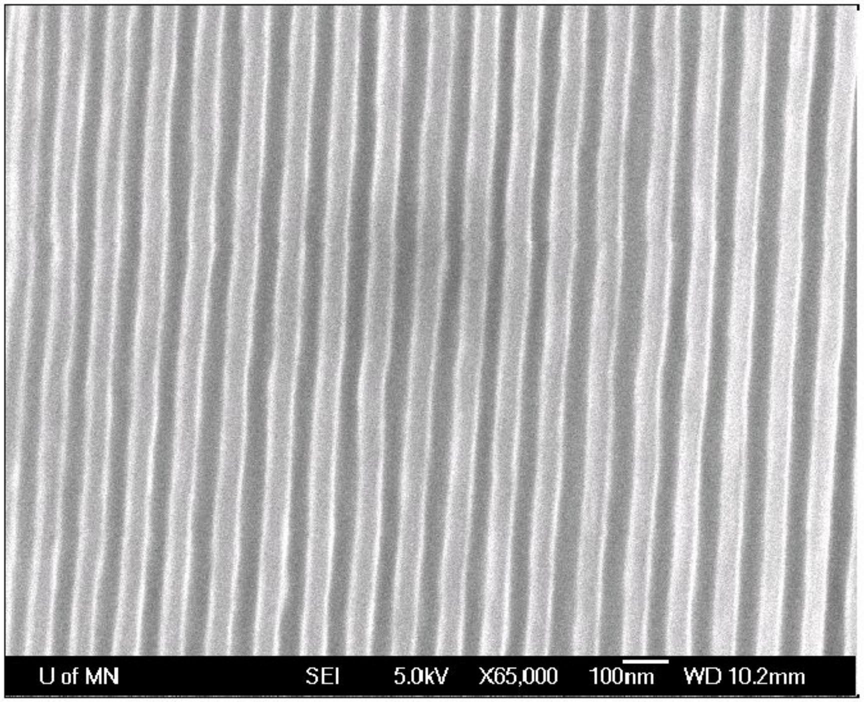


(3) 2nd Anodization

Two-step anodization yields nanopores w/ uniform diameter and spacing

Nanopores are strictly parallel





Oblique view

Side view

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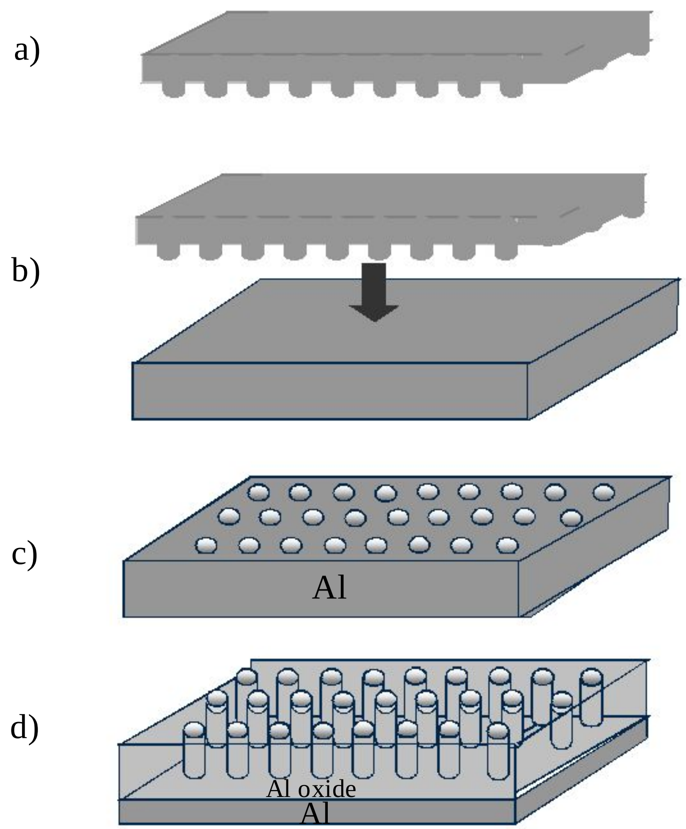
Directing the Self-Assembly



Nanoimprint stamp

Pattern Al surface

Pores grow on pattern

B. J. H. Stadler, Na hyoung Kim, L. Tan, J. Zou, K. Kelchner, R. K. Cobian, Mater. Res. Soc. Symp. Proc. **853E**, I6.3 (2005).
H. Masuda, H. Yamada, M. Satoh, and H. Asoh, Appl. Phys. Lett. **71**, 2770 (1997).
J. Choi, K. Nielsch, M. Reiche, R. B. Wehrspohn, and U. G.osele, J. Vac. Sci. & Technol. B **21**, 763 (2003).

Fig. 4.3. Process for directed self-assembly of nanopore arrays by nano-imprint method: a)Master stamp with ordered array of posts , b)Molding on the Al using an oil press, c)patterned Al sheet, d)Anodization and growth of high order nanopore arrays under particular condition

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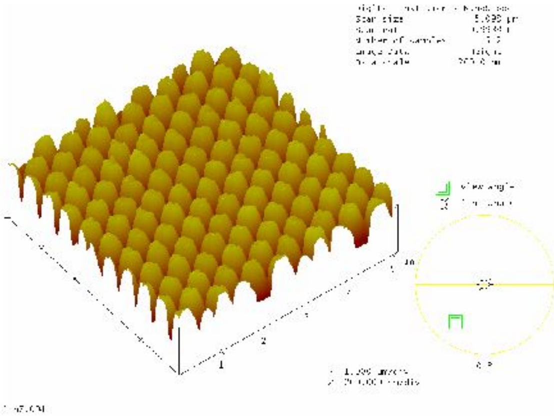
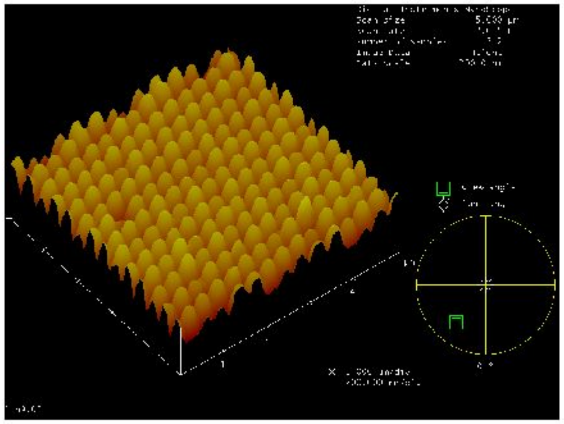
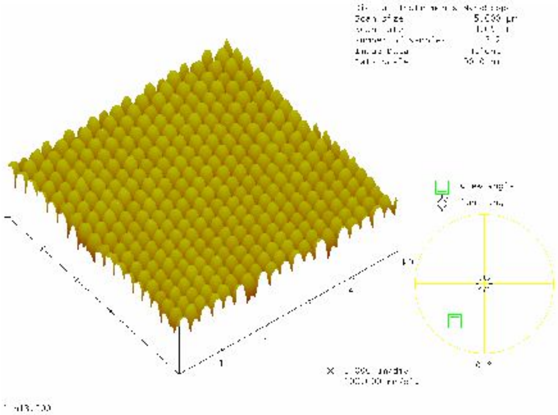
Imprint Stamps



a = 500nm



a = 400nm

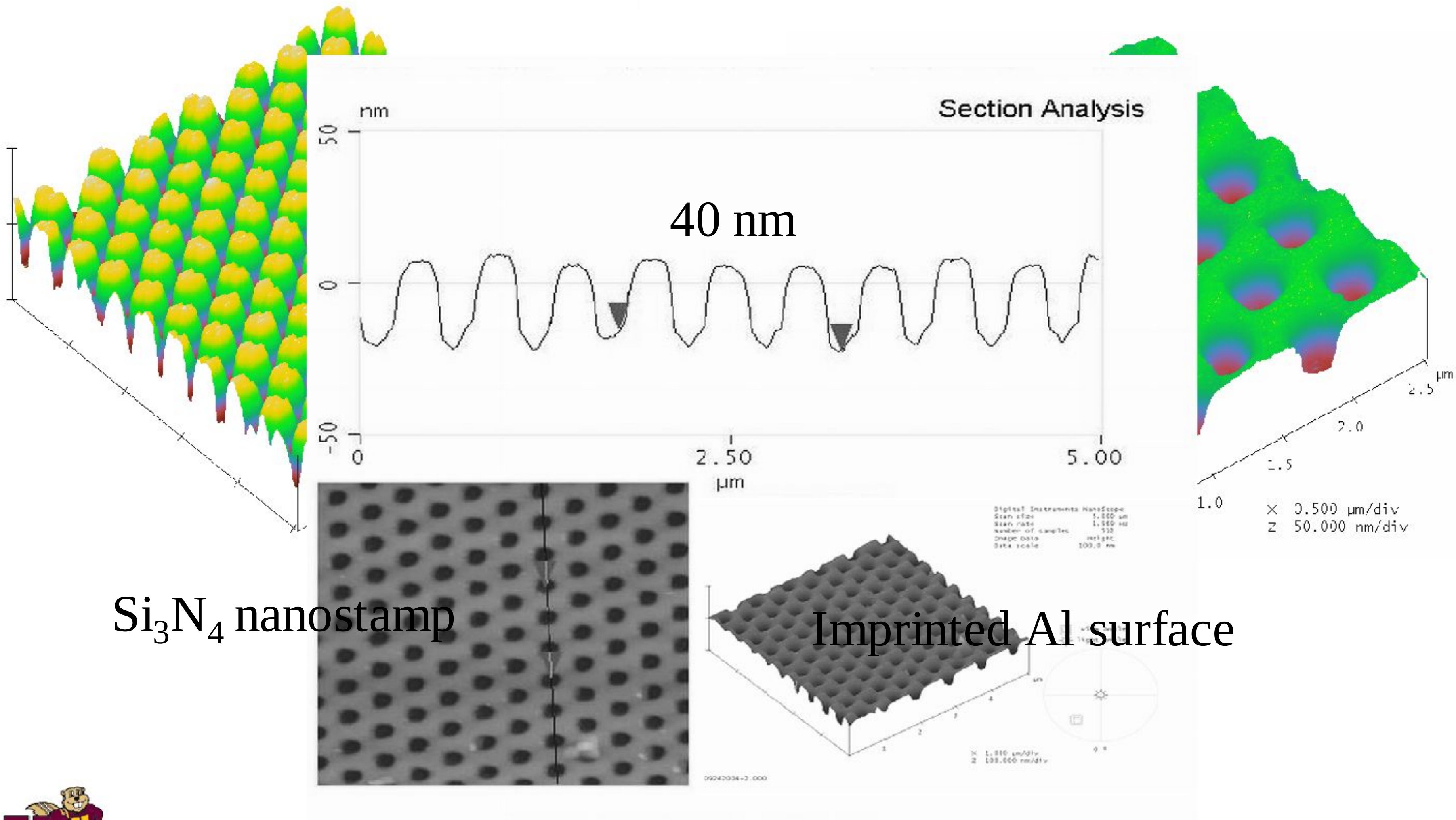


a = 300nm

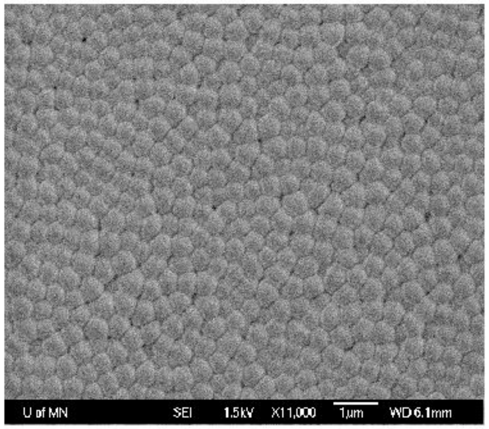
100nm high

Si_3N_4 tips (defined by e-beam lithography) can be used to imprint Al to produce aligned pores

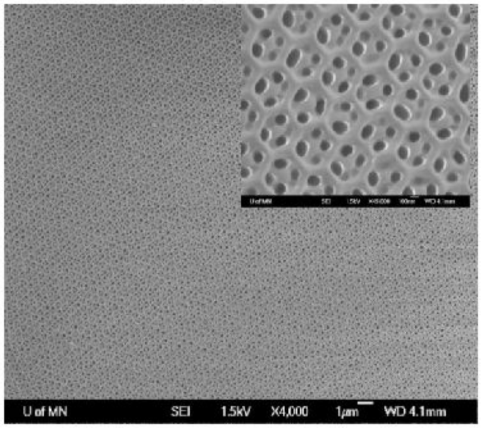
AFM Images


Section Analysis
nm
50
0
-50
40 nm
0
2.50
5.00
µm
1.0
1.5
2.0
2.5
µm
X 0.500 µm/div
Z 50.000 nm/div
Si_3N_4 nanostamp
Imprinted Al surface

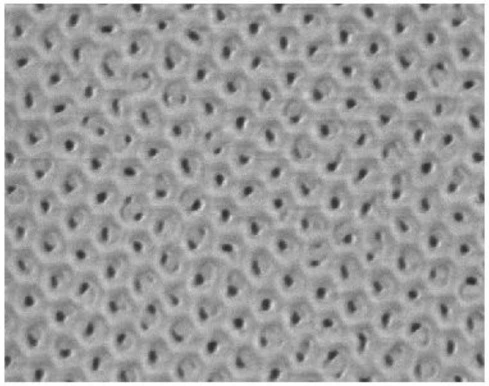
SEM After Anodization



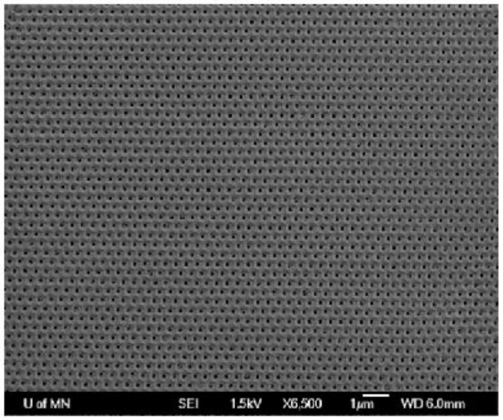
Bottom side of AAO made from nonimprinted Al that was anodized at 180V.



(Top view of AAO formed by anodizing Al that was imprinted with 700nm periodicity at 170V.

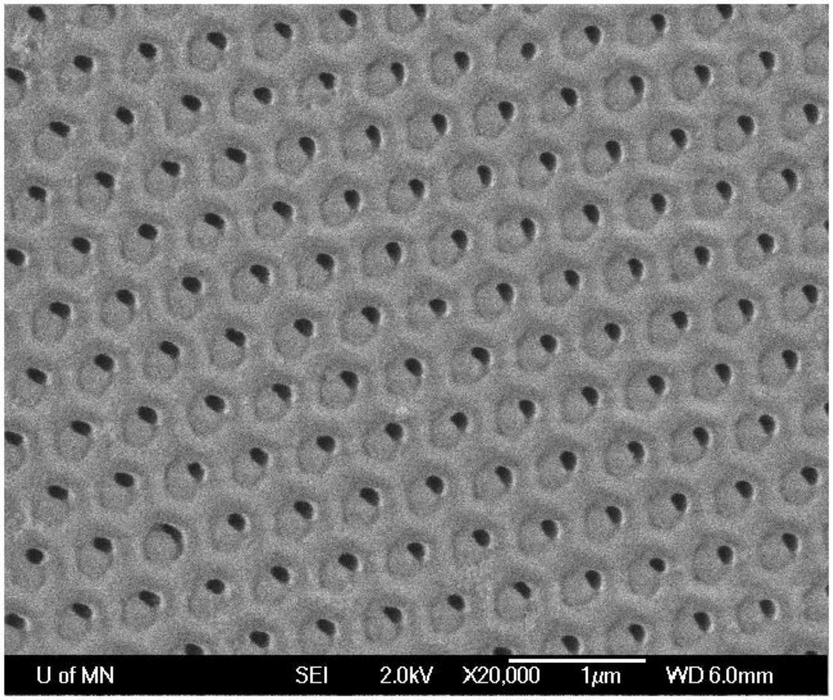


(Top view of AAO formed by anodizing Al that was imprinted with 400nm periodicity at 170V.

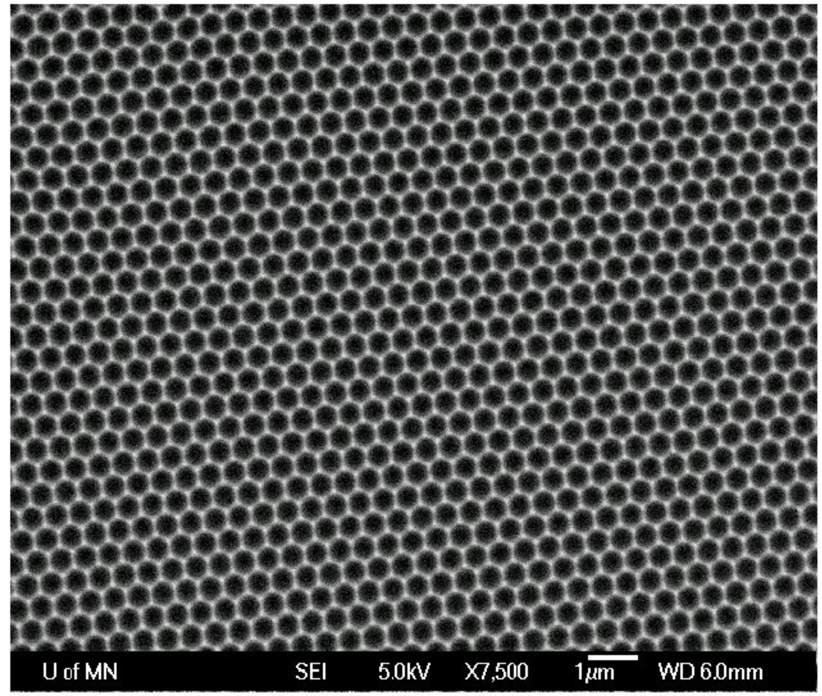


Top view of AAO formed by anodizing Al that was imprinted with 400nm periodicity at 180V.

SEM After Anodization



Top view of as-grown oxide



Etched in a solution of phosphoric acid (6wt%) and chromic acid (1.8wt%) at 60°C for 5h to remove oxide and view underlying Al interface with 500nm spacing maintained.

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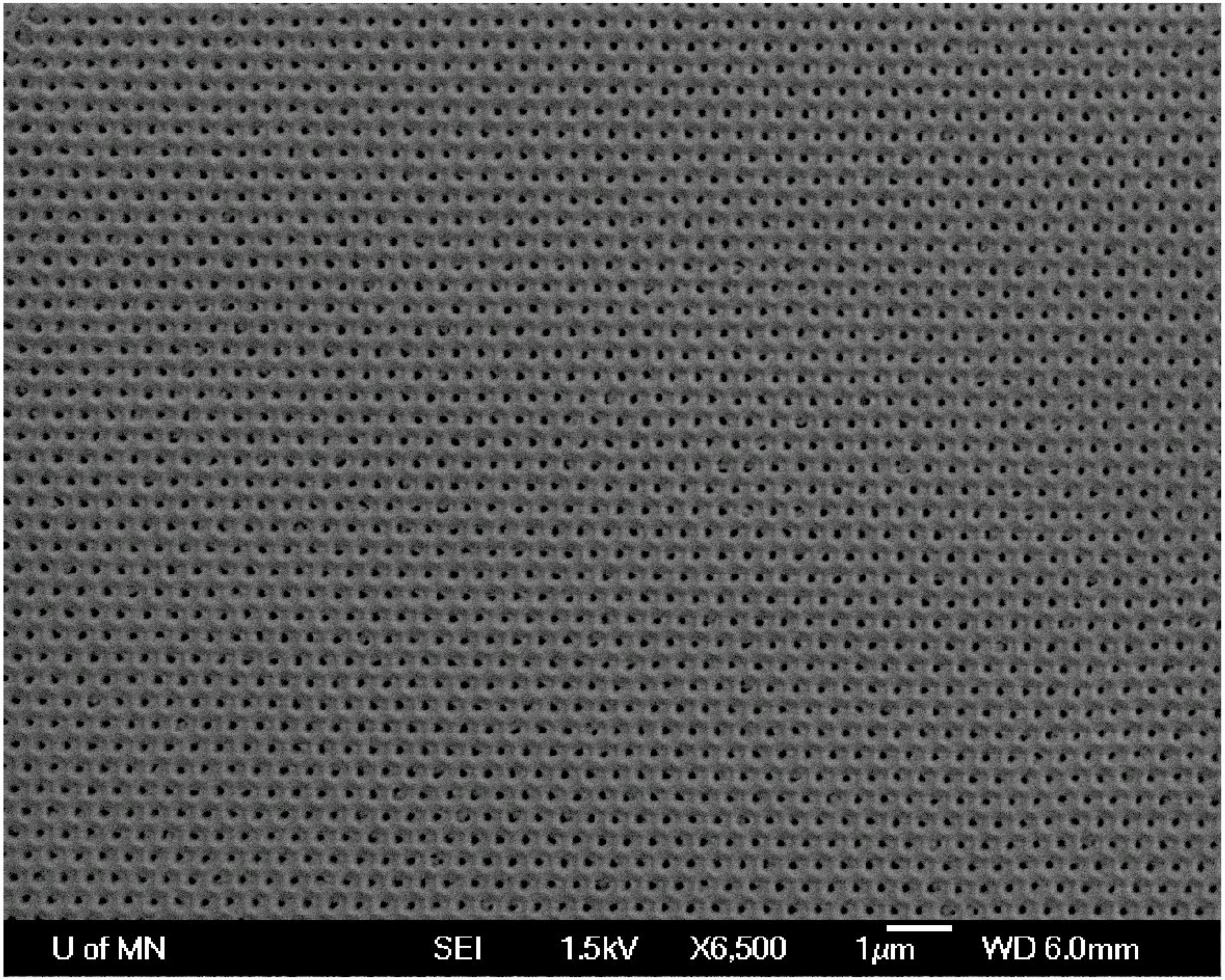
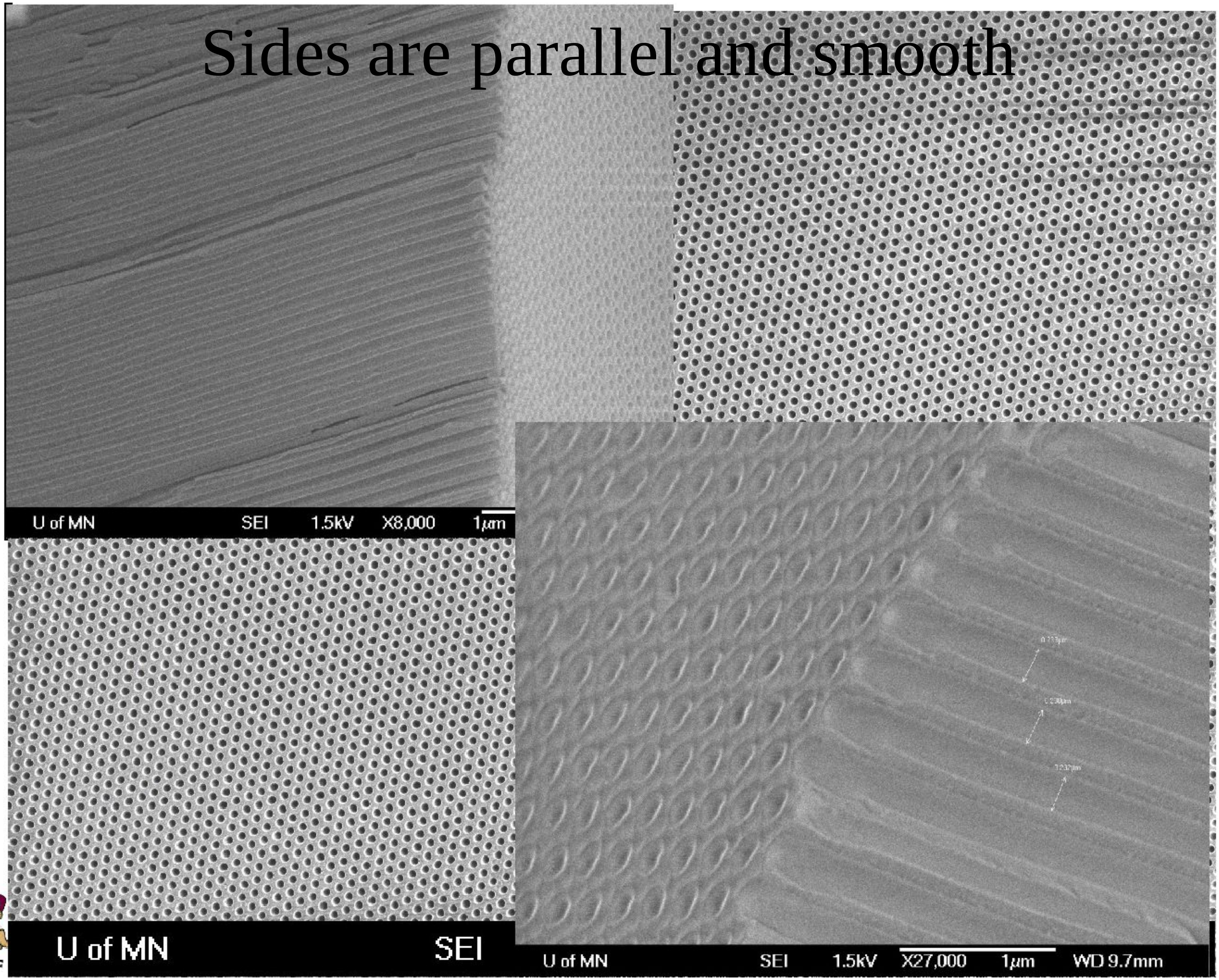

U of MN
SEI
1.5kV
X6,500
1μm
WD 6.0mm

Sides are parallel and smooth



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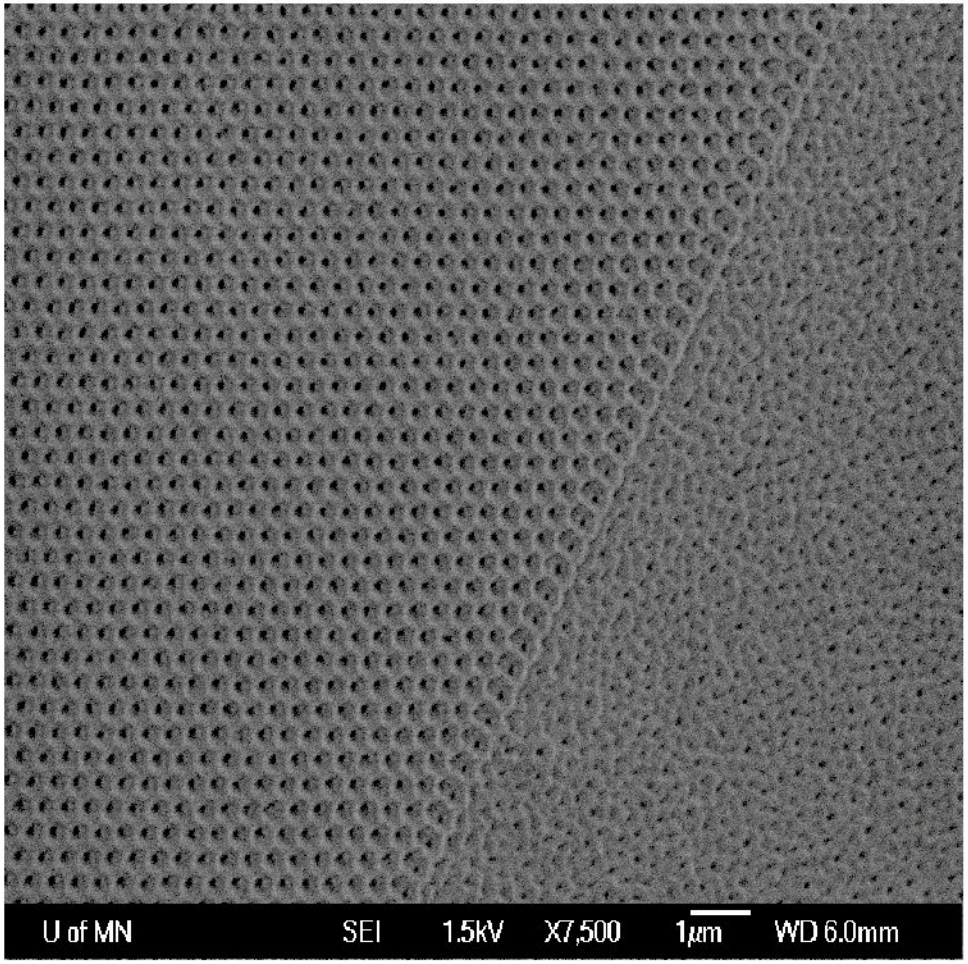
Boundary between Order & Disorder



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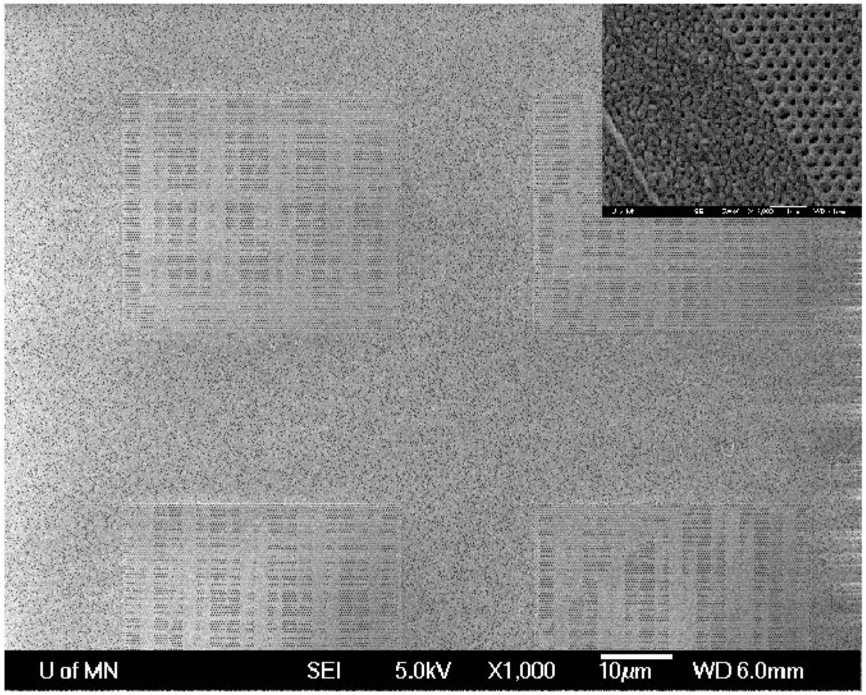
Boundaries between order and disorder can be used in photolithography

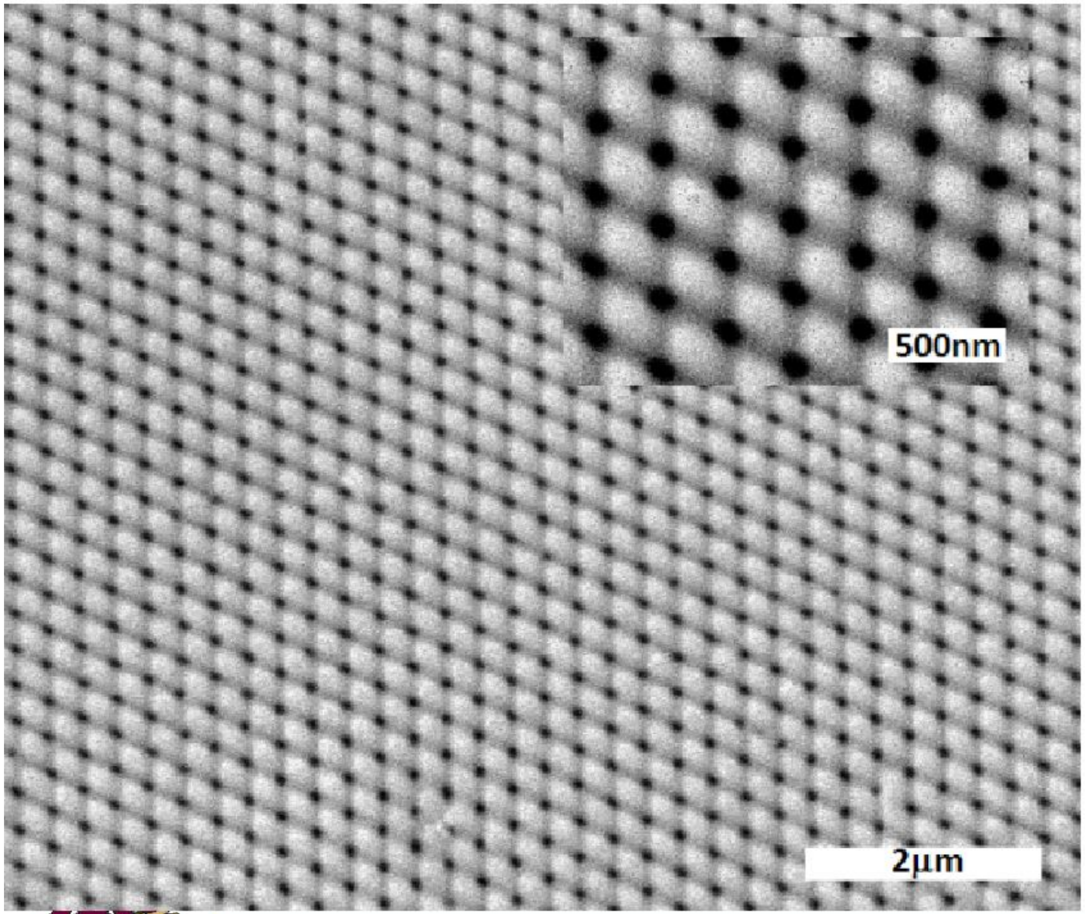


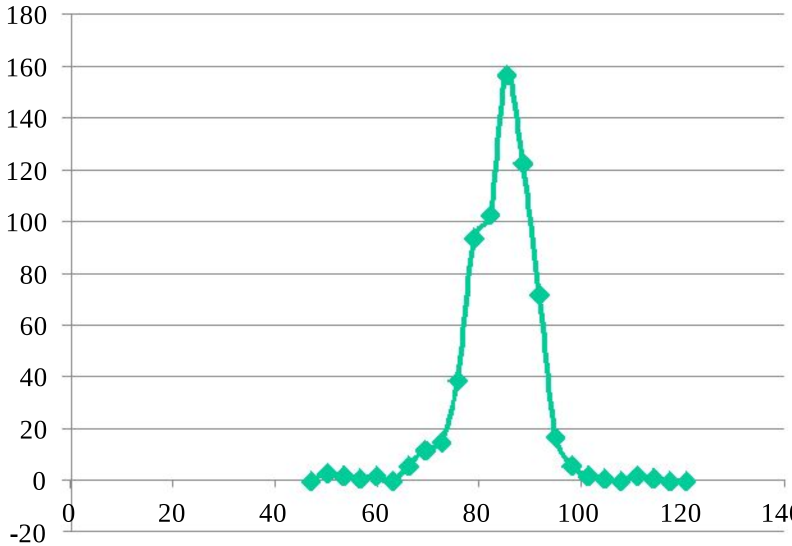
Anodic alumina template with two-scale order by nanoimprint method; insert is the boundary between ordered and disordered regions.

SEM image of nanopores with photo resist aligned to block rows of pores; insert zoomed out image of nanowires grown using electrode pattern.

Large Areas (ft^2) are possible

- 83nm diameter (+/- 6.1nm)
- Over 1 in^2 available for $5 in my lab (not for direct sale :)

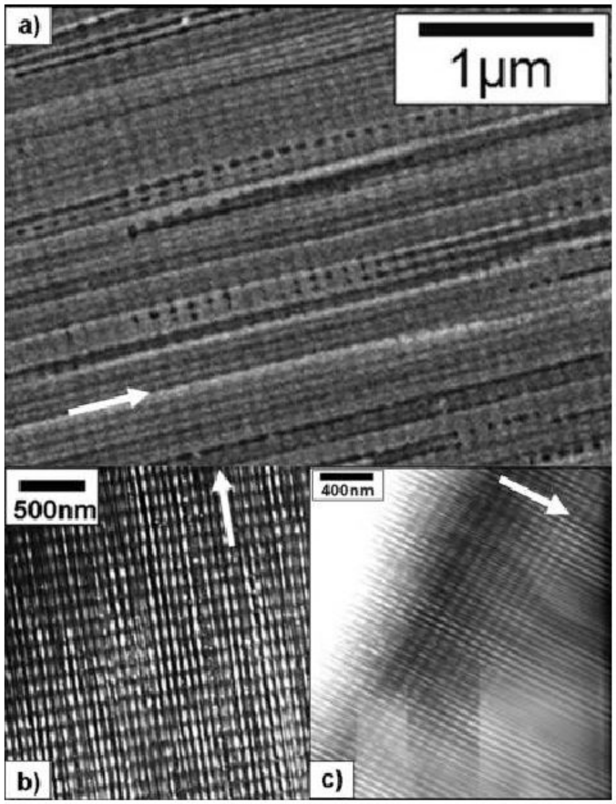




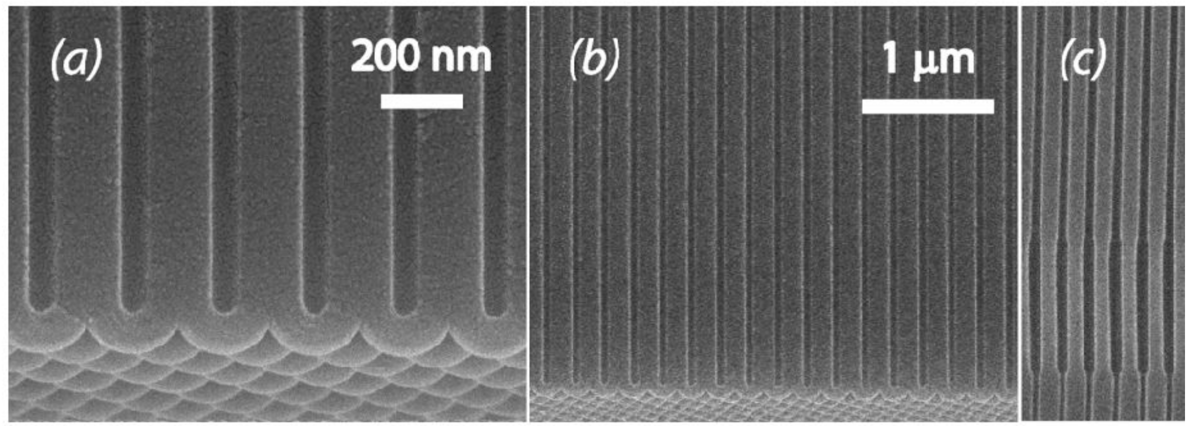
Histogram of 650 pores

Varying Diameters of Nanopores

Schwirn et al ACSNano (2008)



Pitzschel et al ACS Nano (2009)



Norby and Stadler
UMN 2009
unpublished

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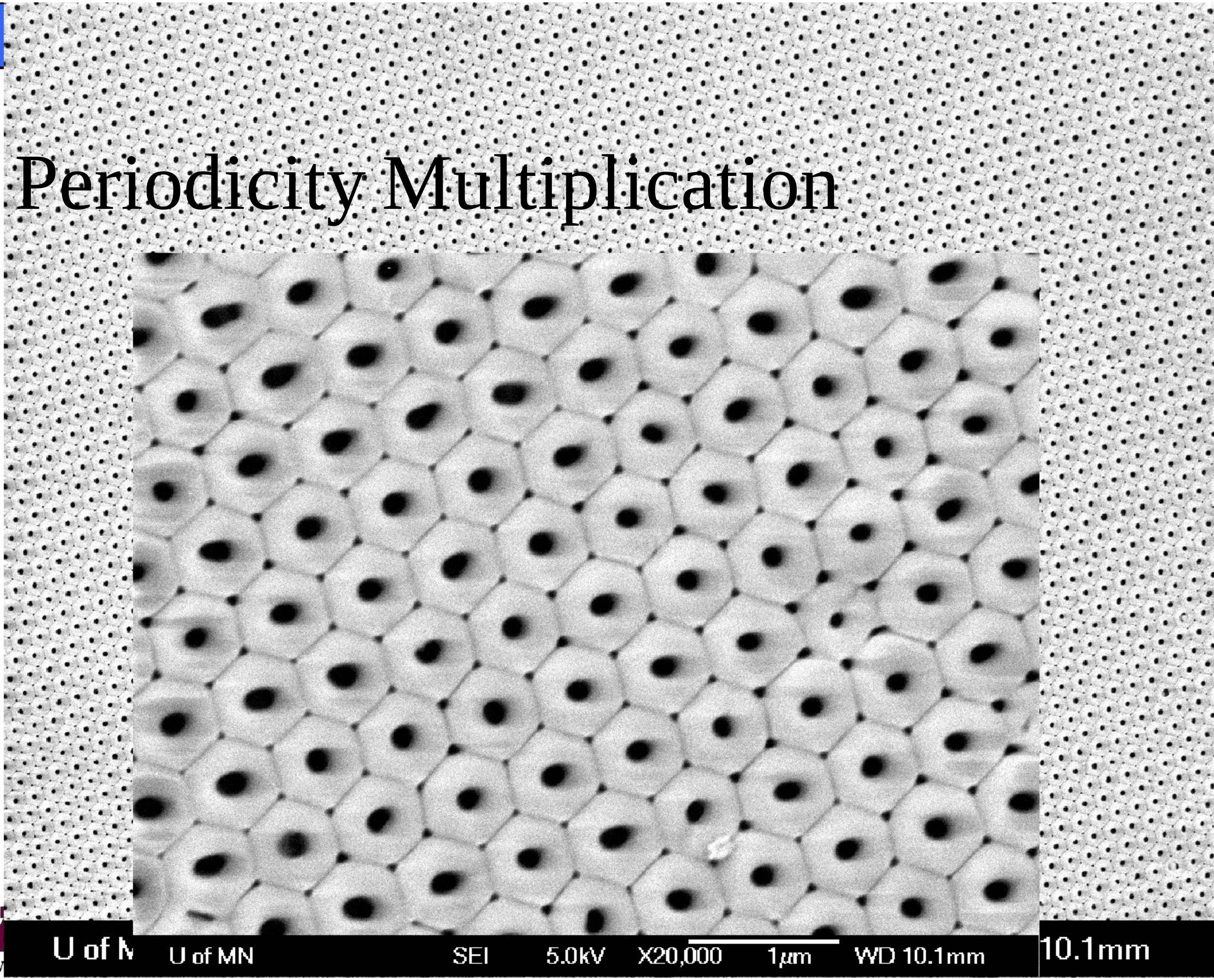
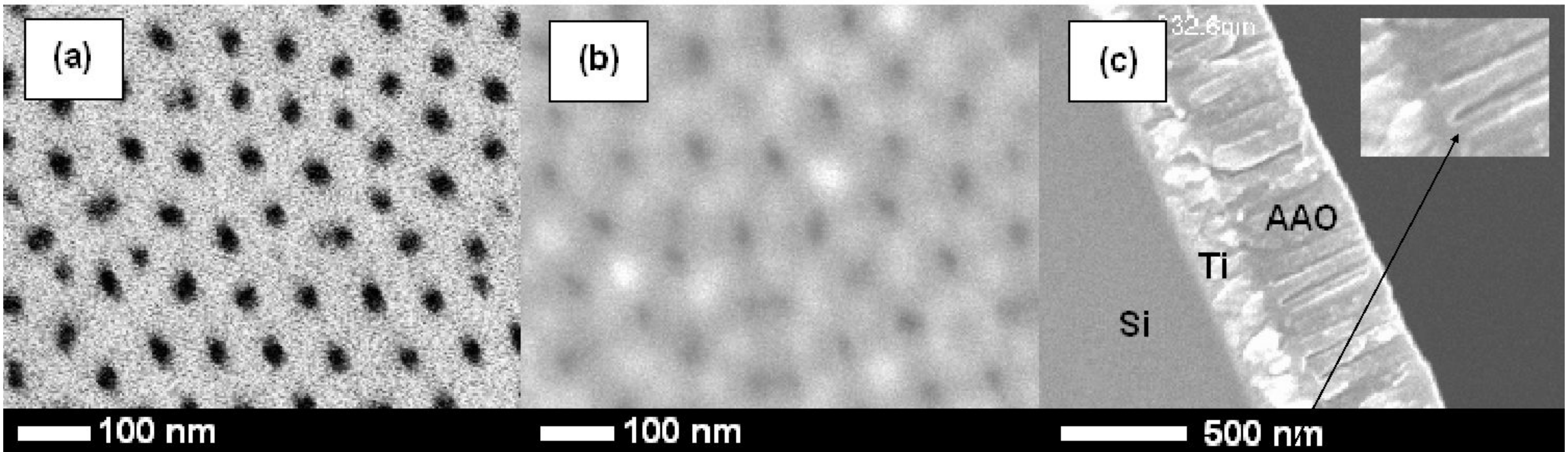
Periodicity Multiplication



AAO on Si



0.4M oxalic = 40nm pores

0.3M oxalic = 30nm pores

Barrier Layer

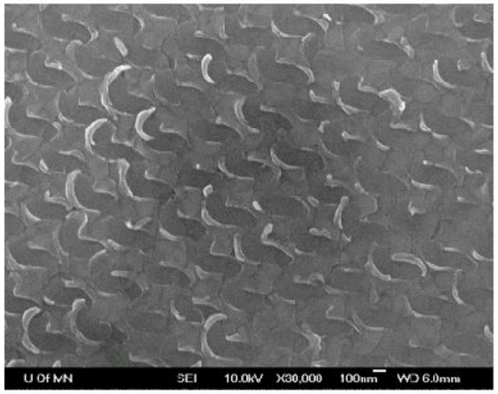
-ion mill (thin AAO only

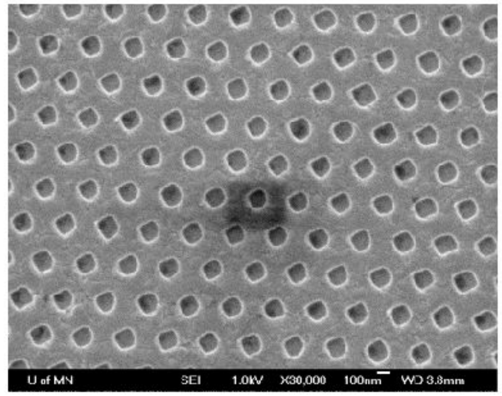
-Wet etch (widens pores)

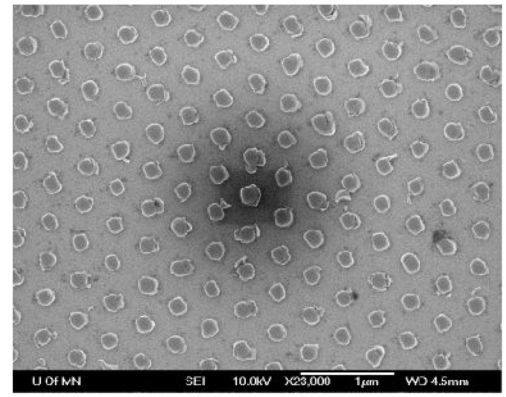
-Electrochemical etch

Perfect AAO on Si

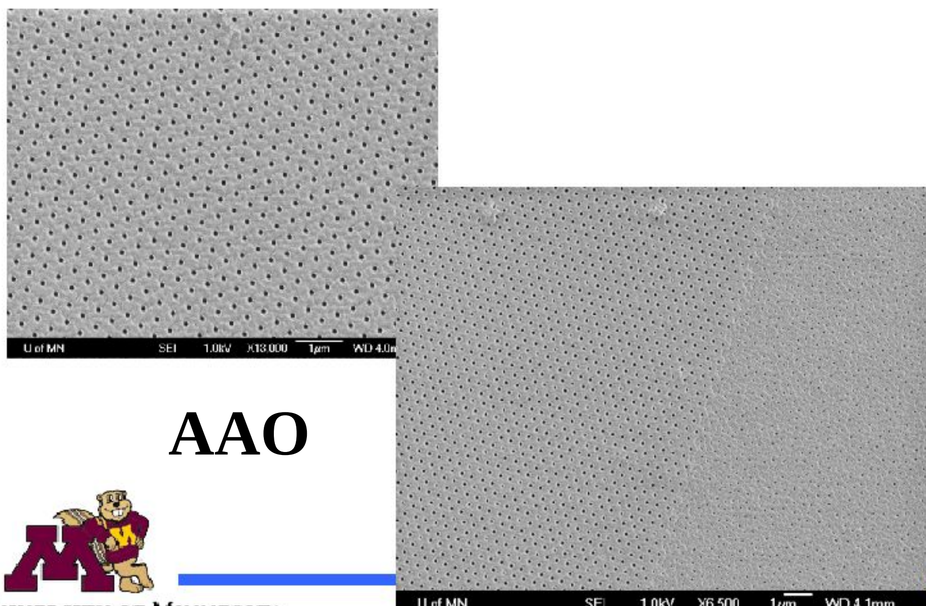
Stamp after >30 imprints





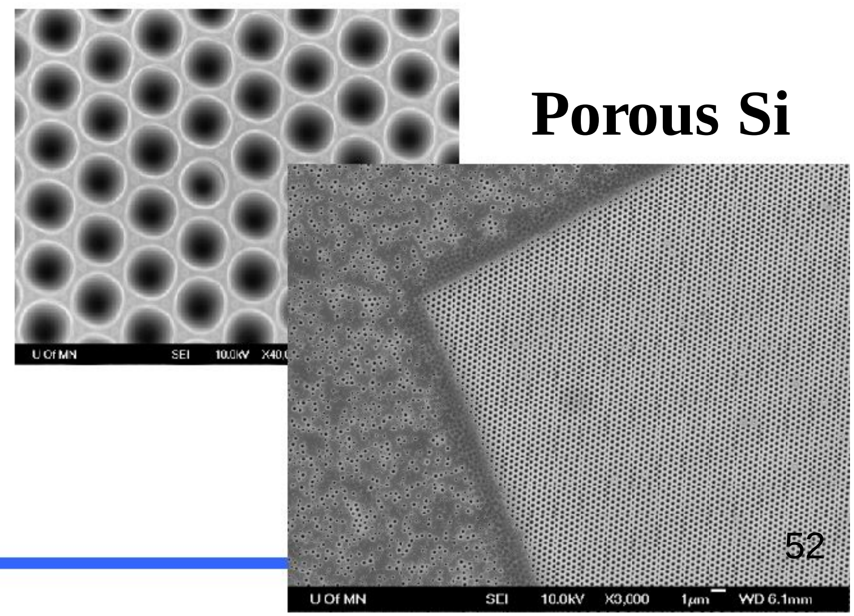


At first stamp slipped, but then it held and was not damaged



AAO

Porous Si



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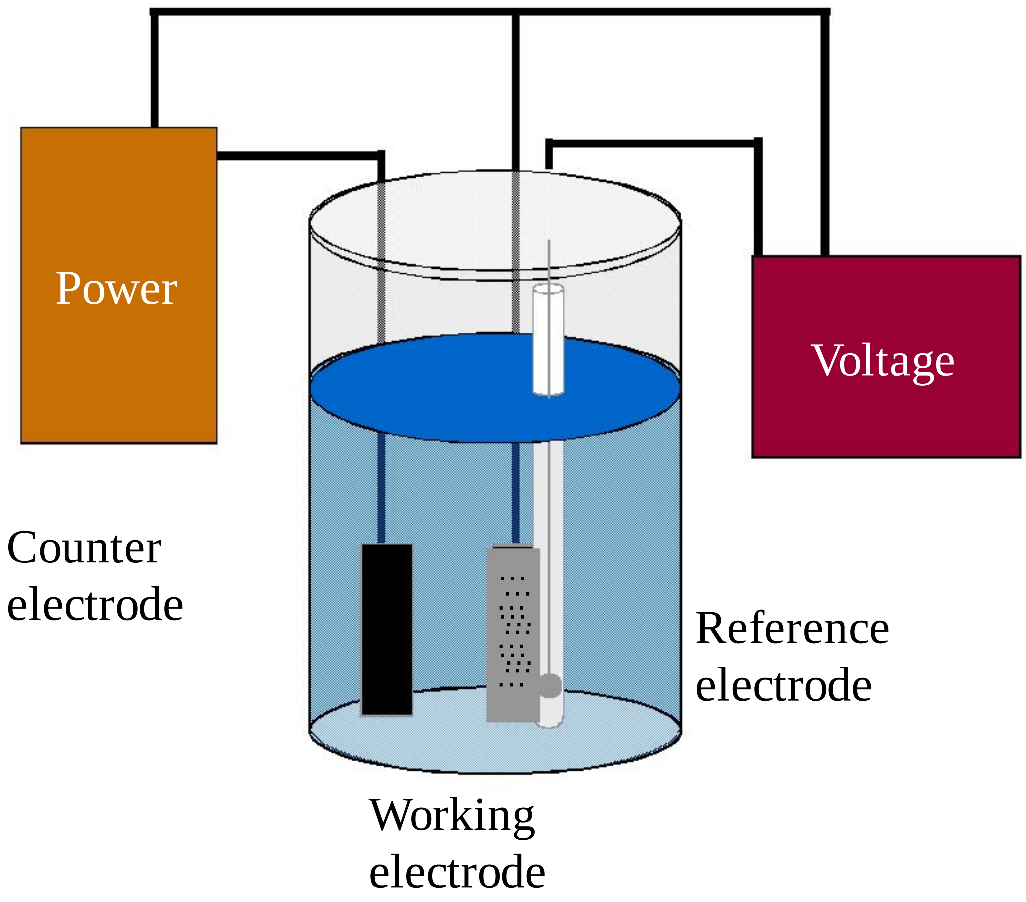
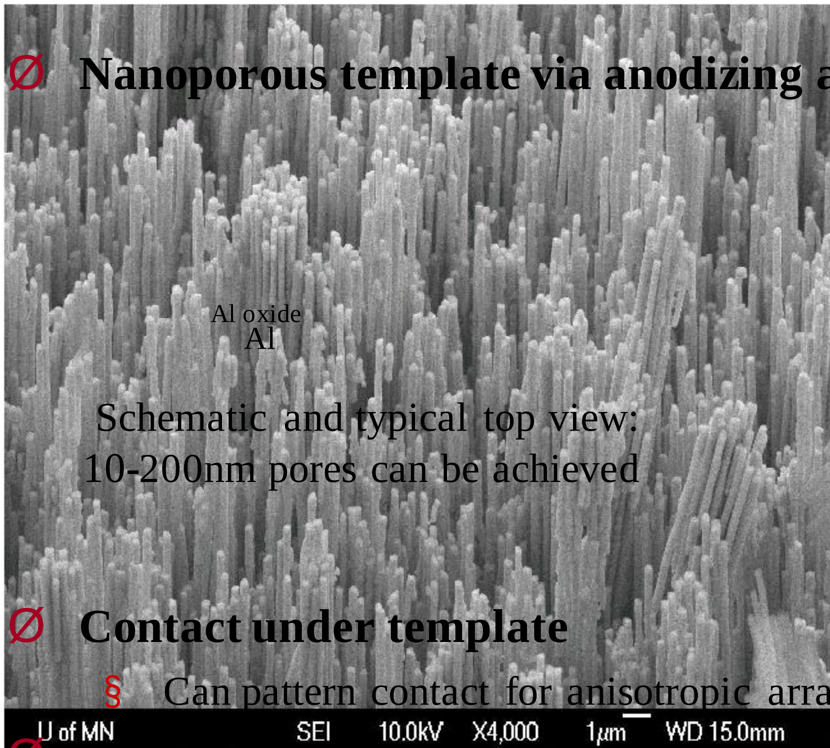
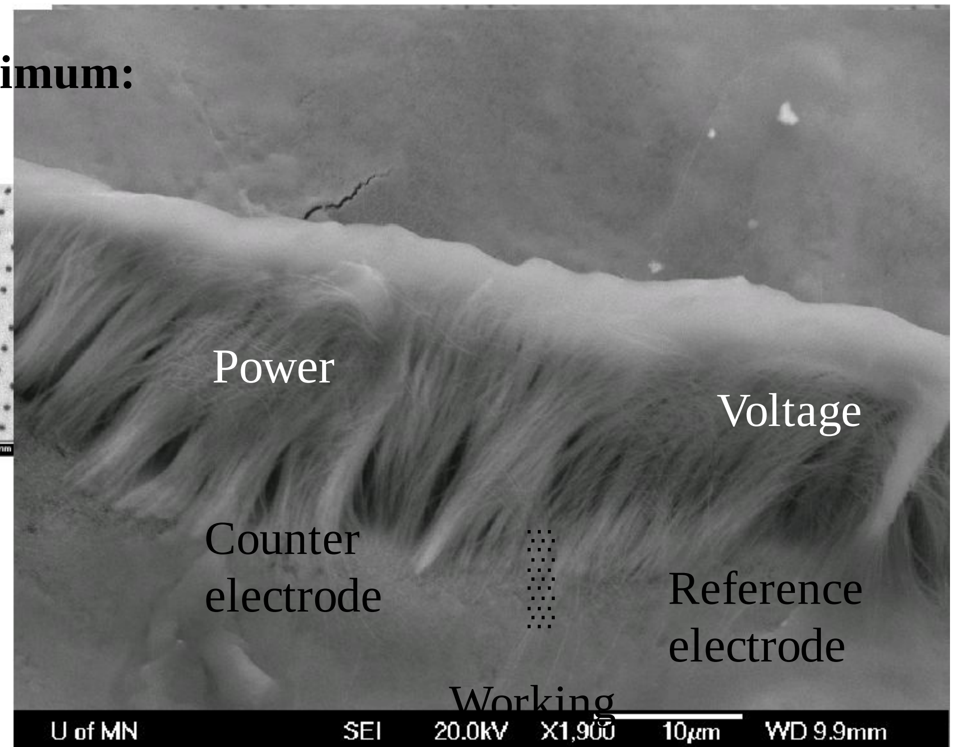
Making Nanowires



Making Nanowires

- **Nanoporous template via anodizing alumimum:**





Al oxide
Al

Schematic and typical top view:
10-200nm pores can be achieved

- **Contact under template**
  - Can pattern contact for anisotropic arrays
- **Electroplate nanowires into pores**
  - Any conductive material can be made
- **Etch template if application requires**

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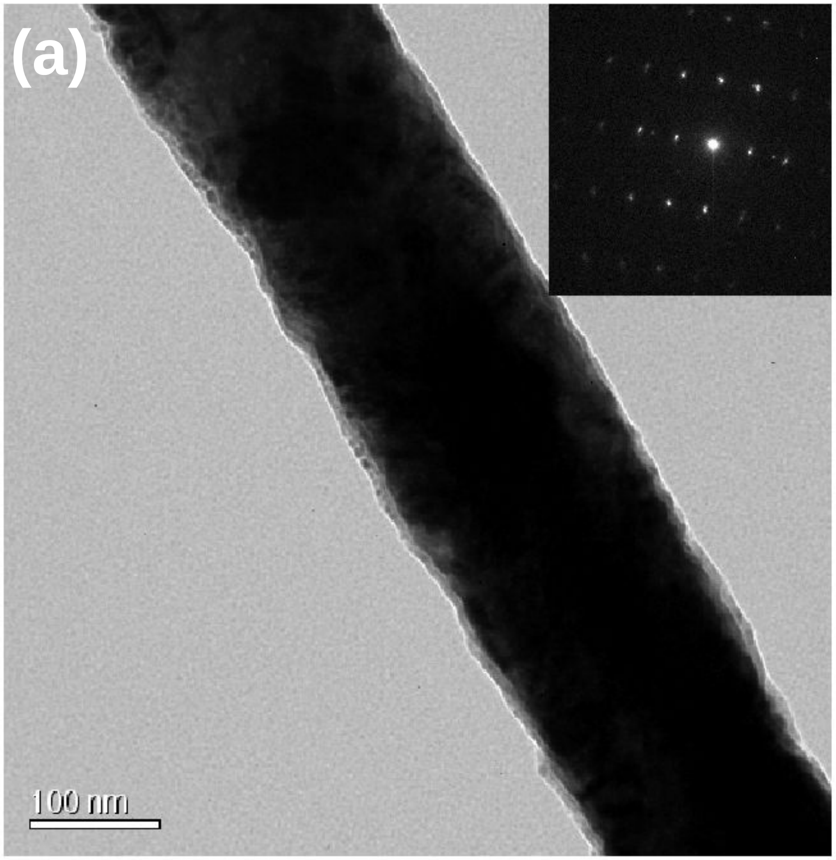
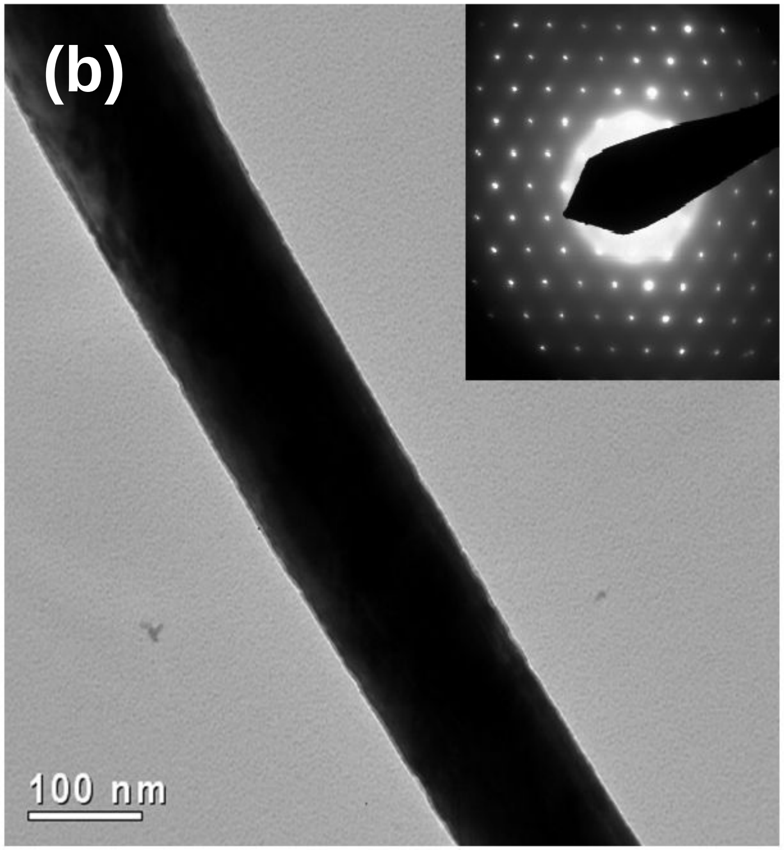
TEM Analysis



(002) along the wire



(002) Perpendicular to the wire

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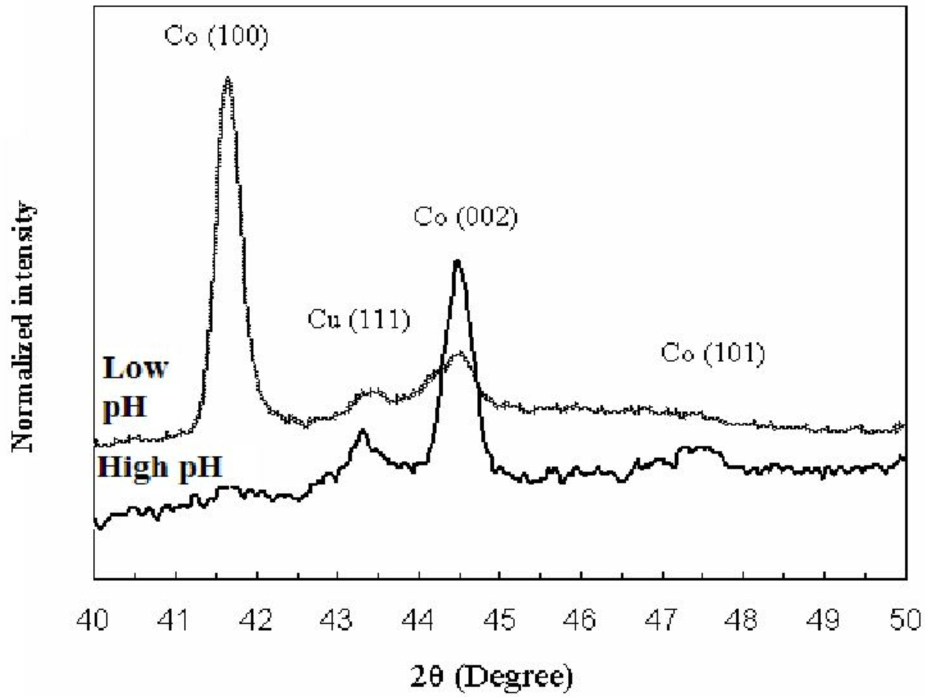
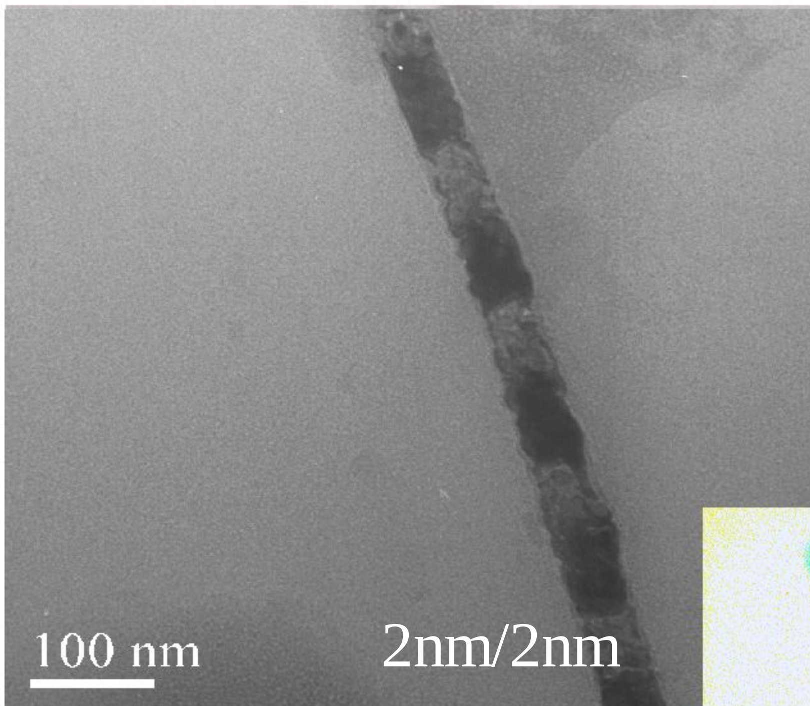
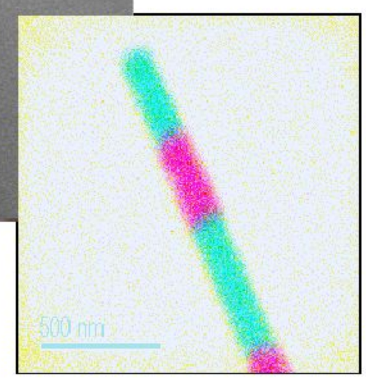
Control of Co Crystallographic Orientation



- Control pH of the solution to adjust Co caxis alignment
  - -- High pH, Co c-axis along wire
  - -- Low pH Co c-axis perpendicular to wire

TEM Image of Co/Cu Multilayered Nanowires

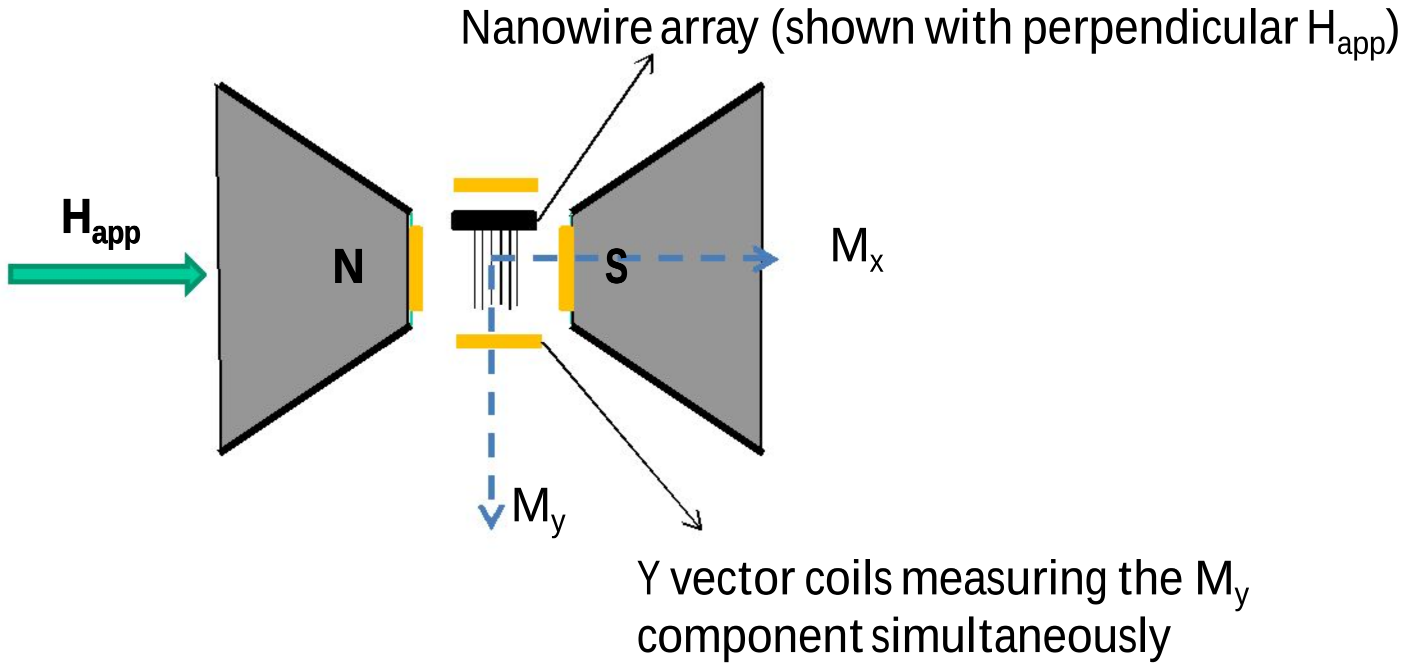




Outine

- Motivation: Memory Applications
  - Hard drives: media and heads
  - Random Access Memories
- Fabrication Techniques
- Measuring Magnetoresistive Elements
- Conclusions

Magnetic Characterization



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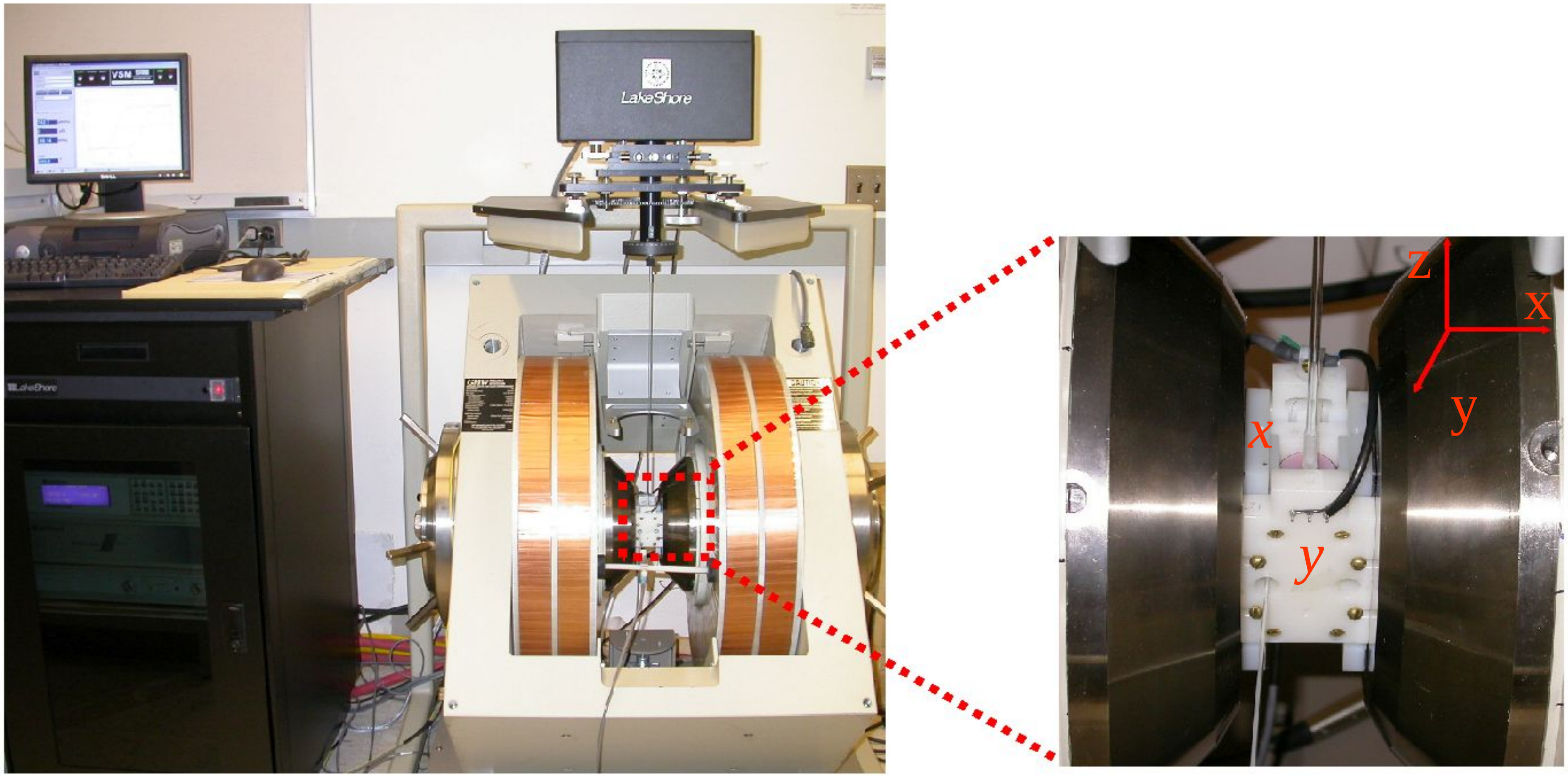
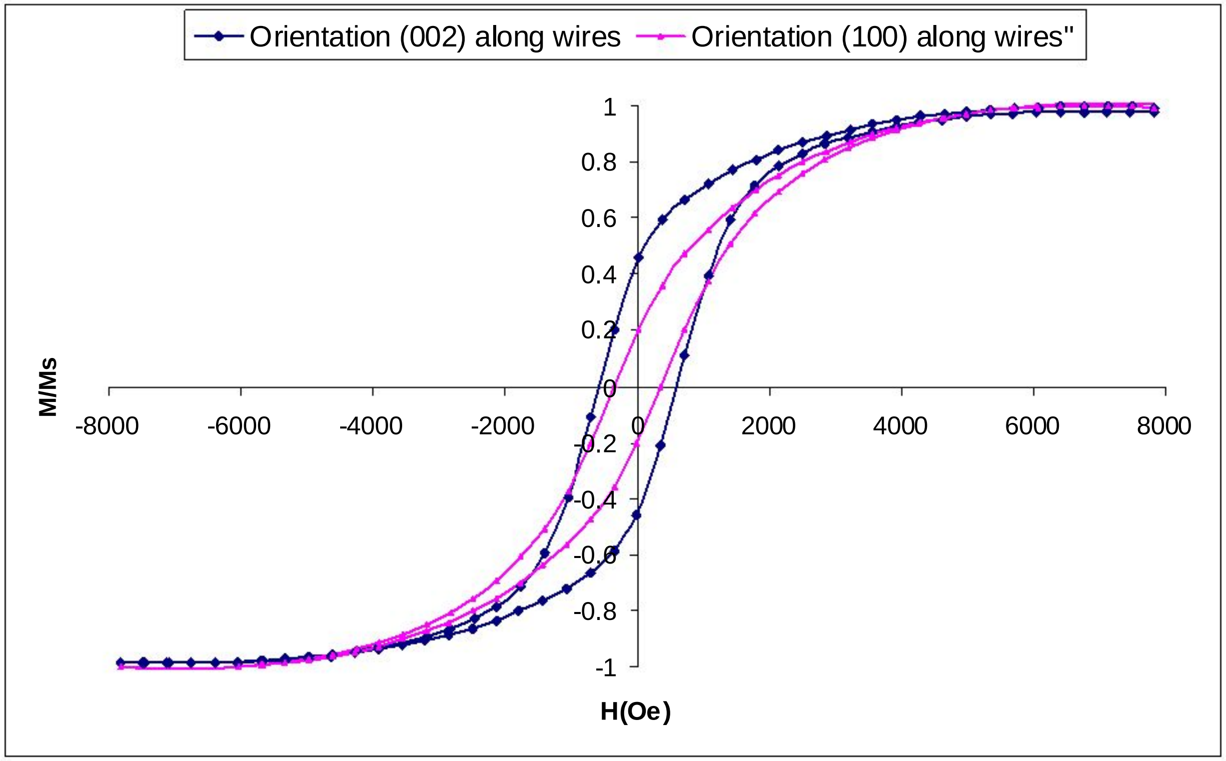
Vibrating Sample Magnetometer (VSM)



M_x— Magnetic component along magnetic field

M_y— Magnetic component perpendicular to magnetic field

M-H Loops of Co nanowires



Magnetic field parallel to nanowires (Diameter:150nm)

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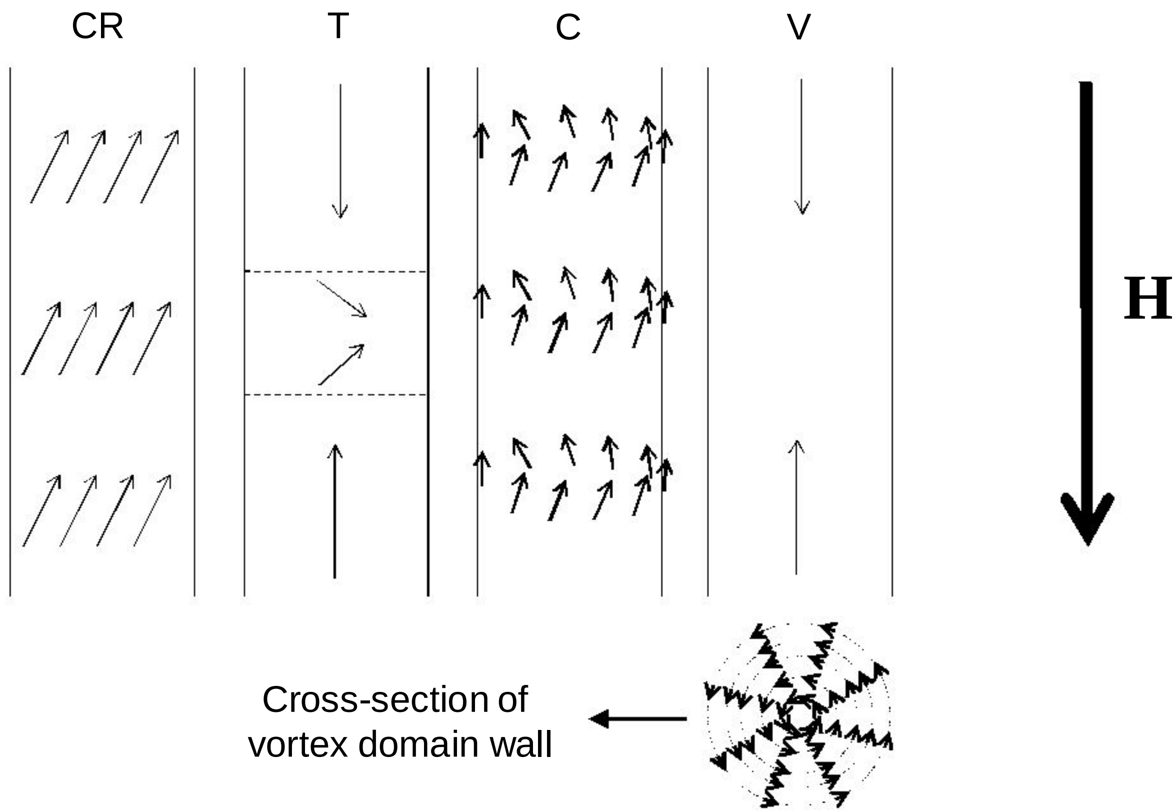
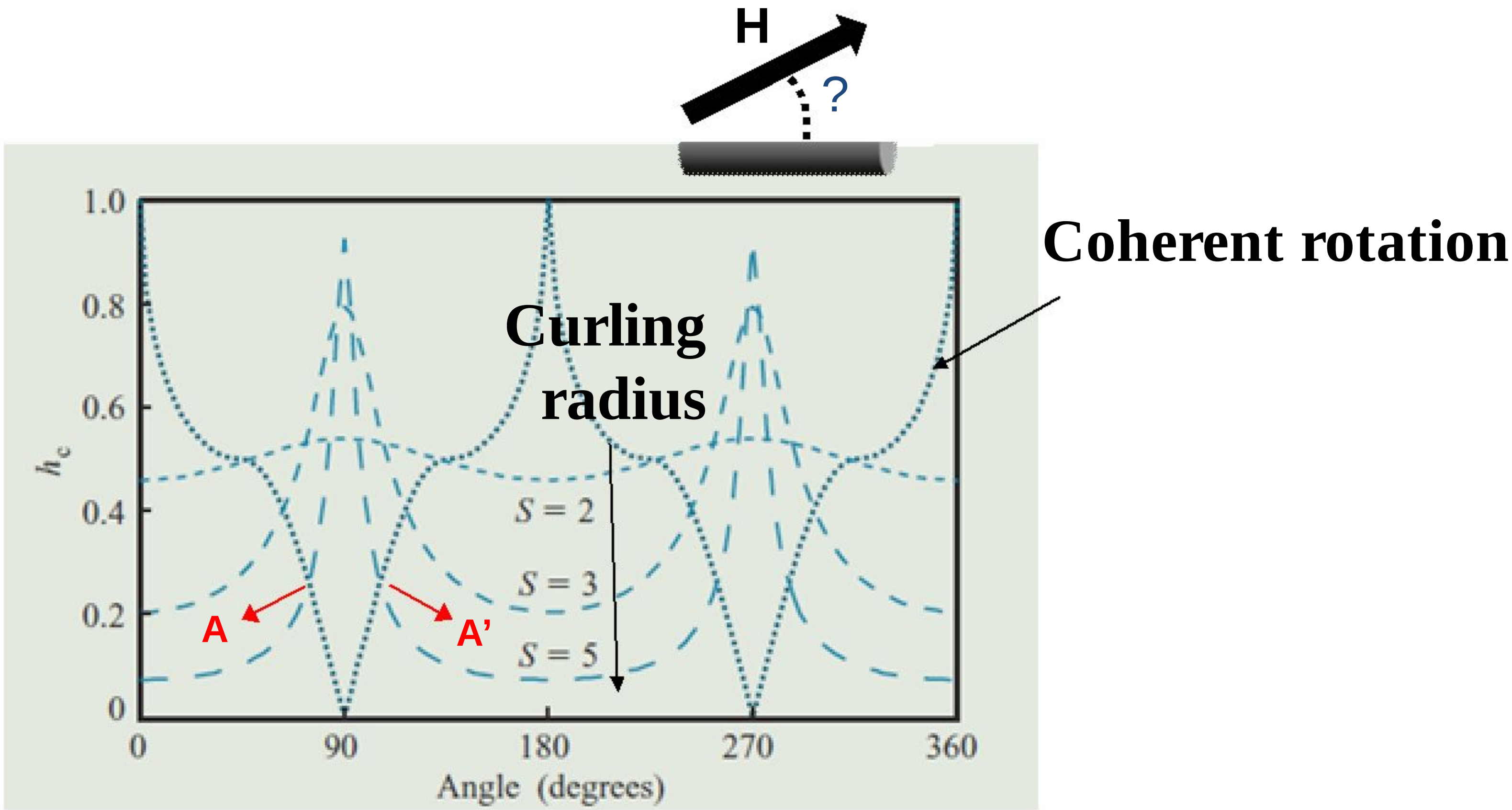
Magnetization reversal
- what is different for nanomagnetism?



CR: coherent rotation, T: transverse domain wall C: curling and V: vortex domain wall.

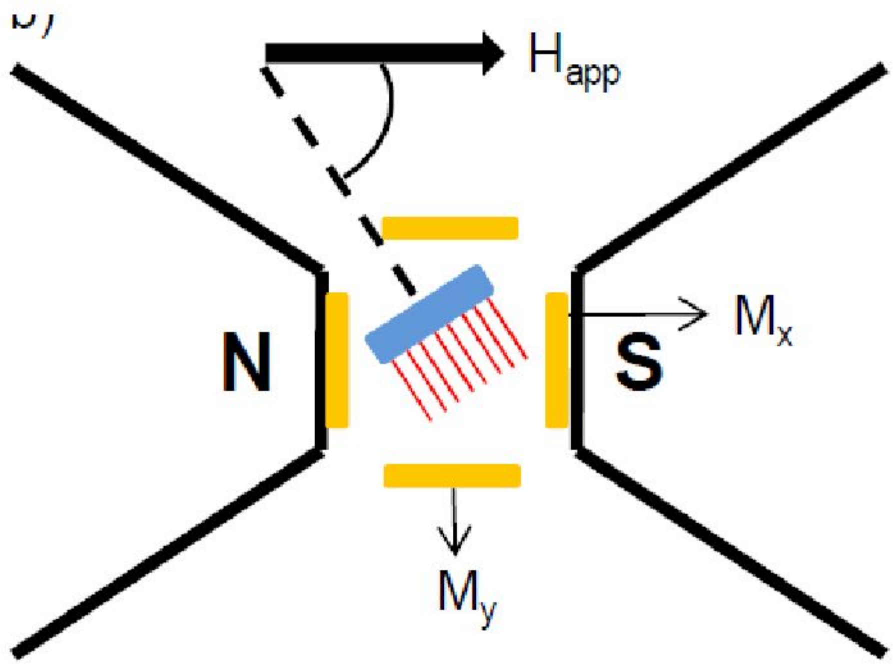
Angular dependence of coercivity (Hc)



Calculated angular dependence of the reduced coercivity $h_c = H_c/2pM_s$ for $S = r/r_0$, where $r_0 = A^{1/2}/M_s$.
For $Fe_{80}Ga_{20}$, A = 1.8 x 10^{-6} erg/cm, M_s = 1353 emu/cm^3, and therefore r_0 is ~10 nm radius or ~20 nm diameter.

Adapted from Sun et al IBM J. Res. Dev. 49, 79-102 (2005).

Experimentally



Sample moved, not field

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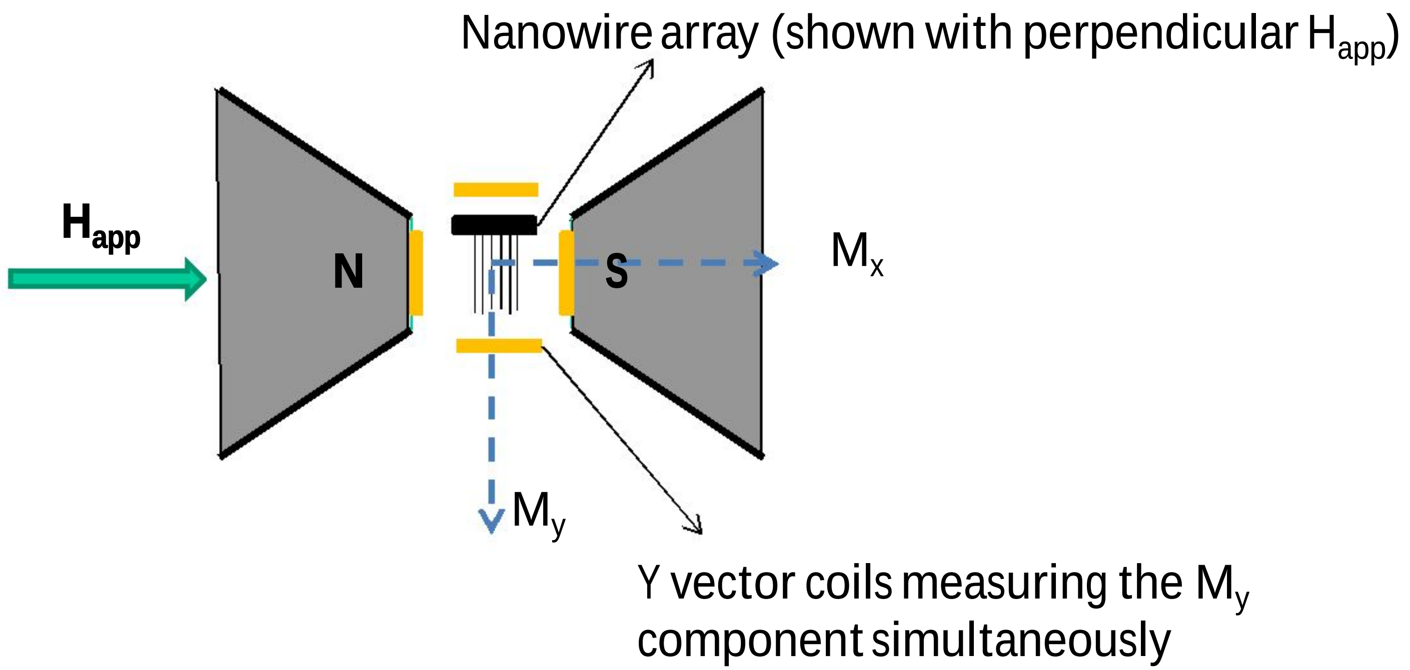
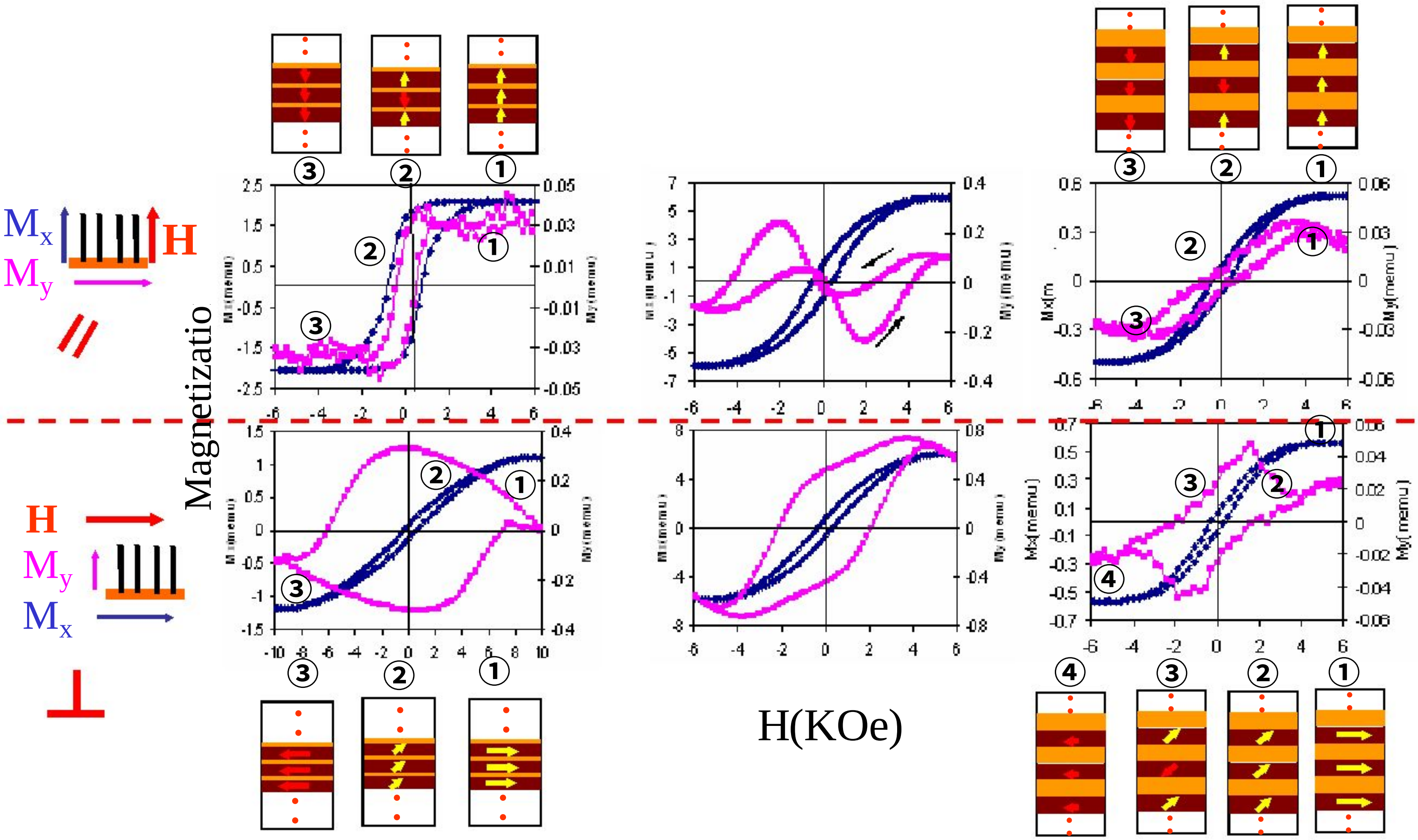
Magnetic Characterization



M-H Loops of Co(5nm)/Cu(xnm) Nanowires



Cu(0.5nm) Cu(1.5nm) Cu(5nm)

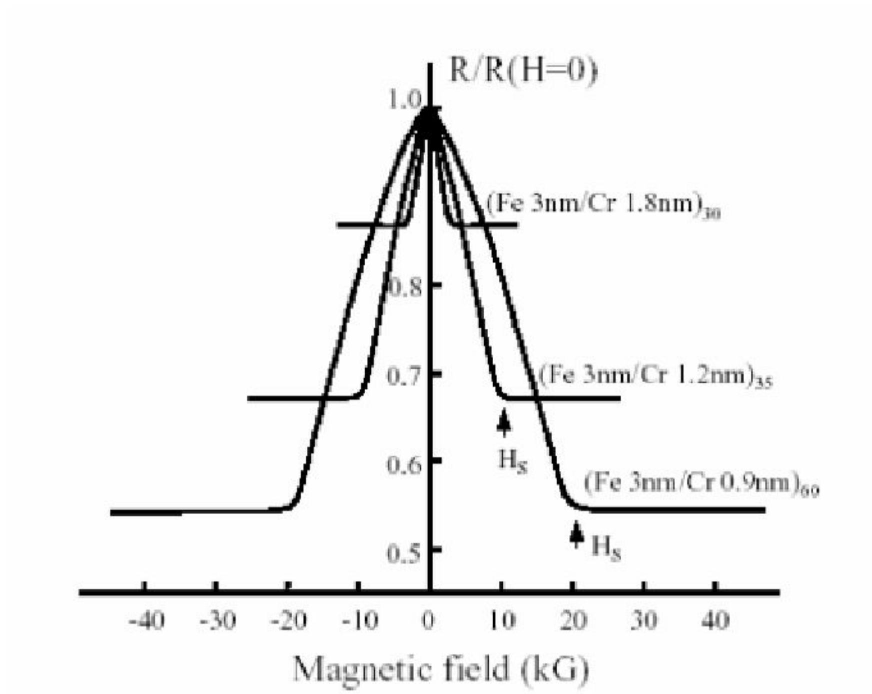
Magneto-transport measurements

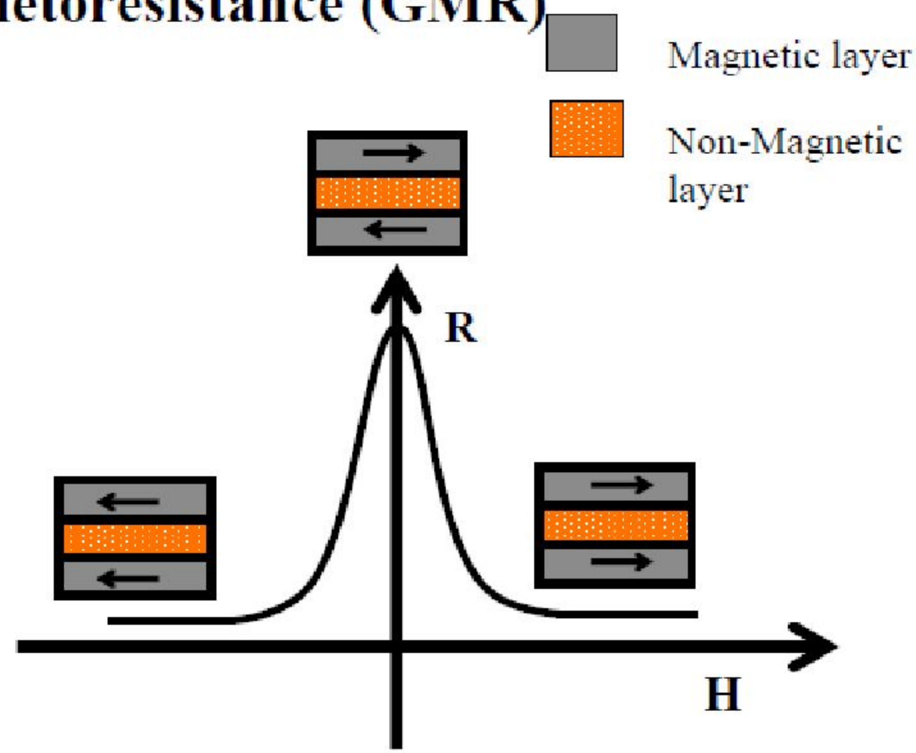
-magnetic and *electronic* effects

- PPMS
  - Same bottom electrode
  - Ag epoxy on top
- Head Tester
  - Two probes on top
- AFM
  - Conductive AFM probe on top
  - Same electrode

Introduction

------Giant Magnetoresistance (GMR)





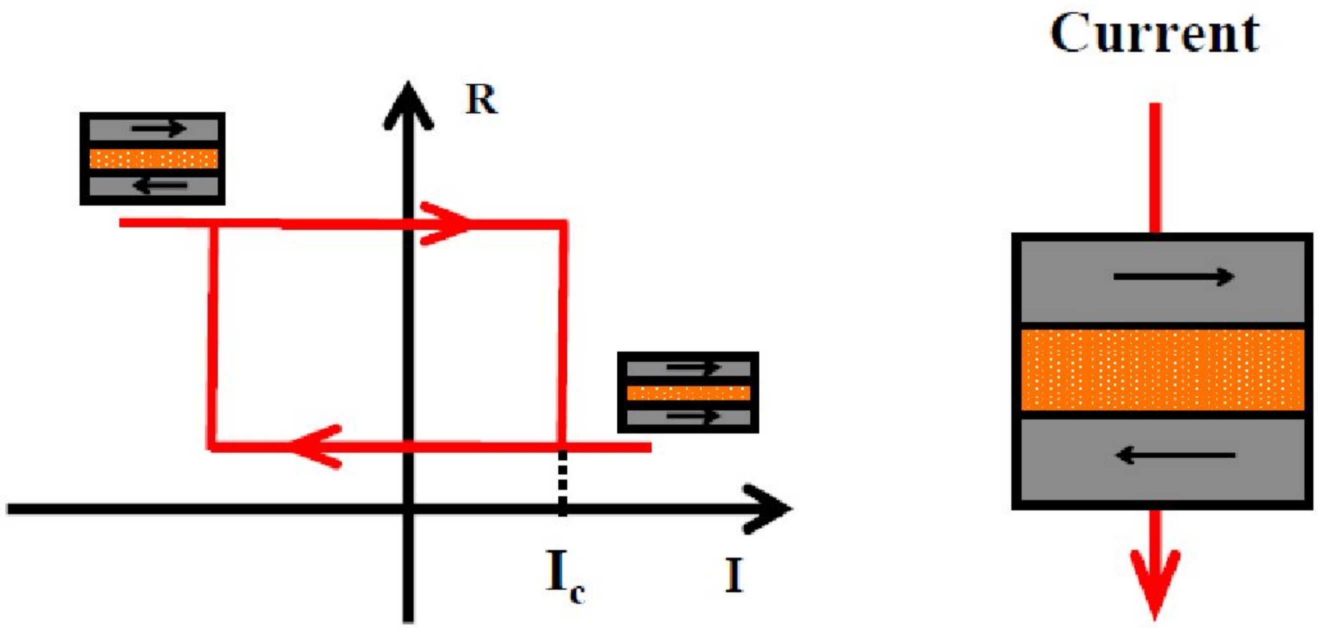
Baibich et al ,Phys. Rev. Lett. 61 (1988) 2472

$$GMR(H) = \frac{R(H) - R_{Sat}}{R_{Sat}}$$

The change of resistance of a conductor in an external magnetic field.

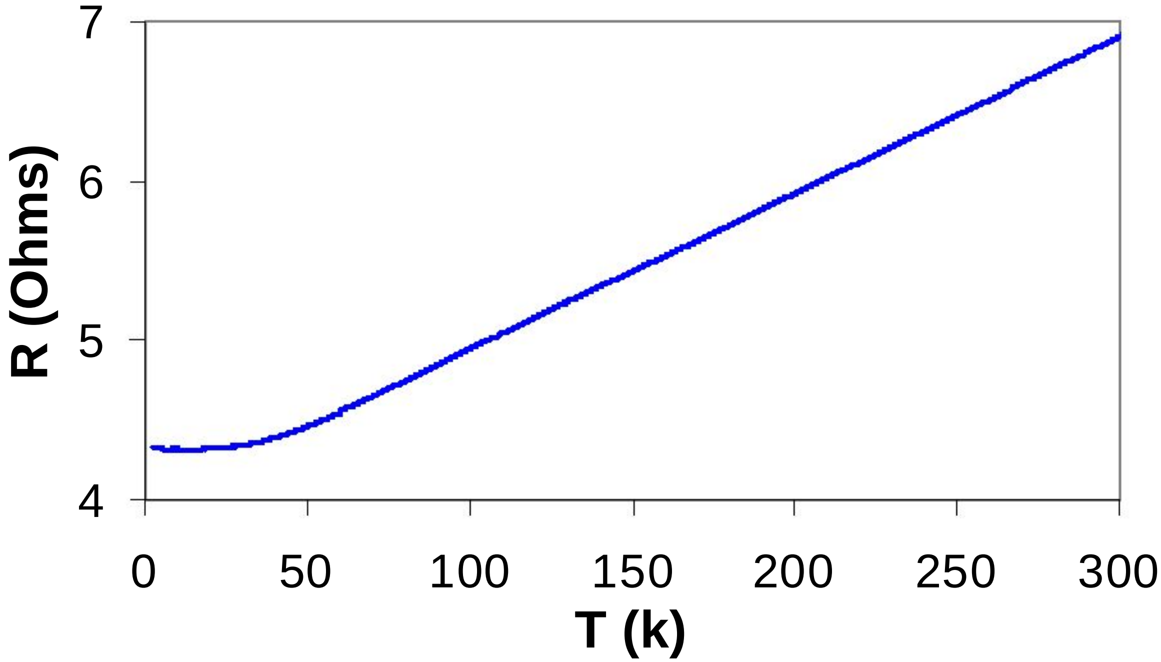
Introduction

----Spin Transfer Torque (STT)



Switching current ,I_c is about $10^7 A/cm^2$

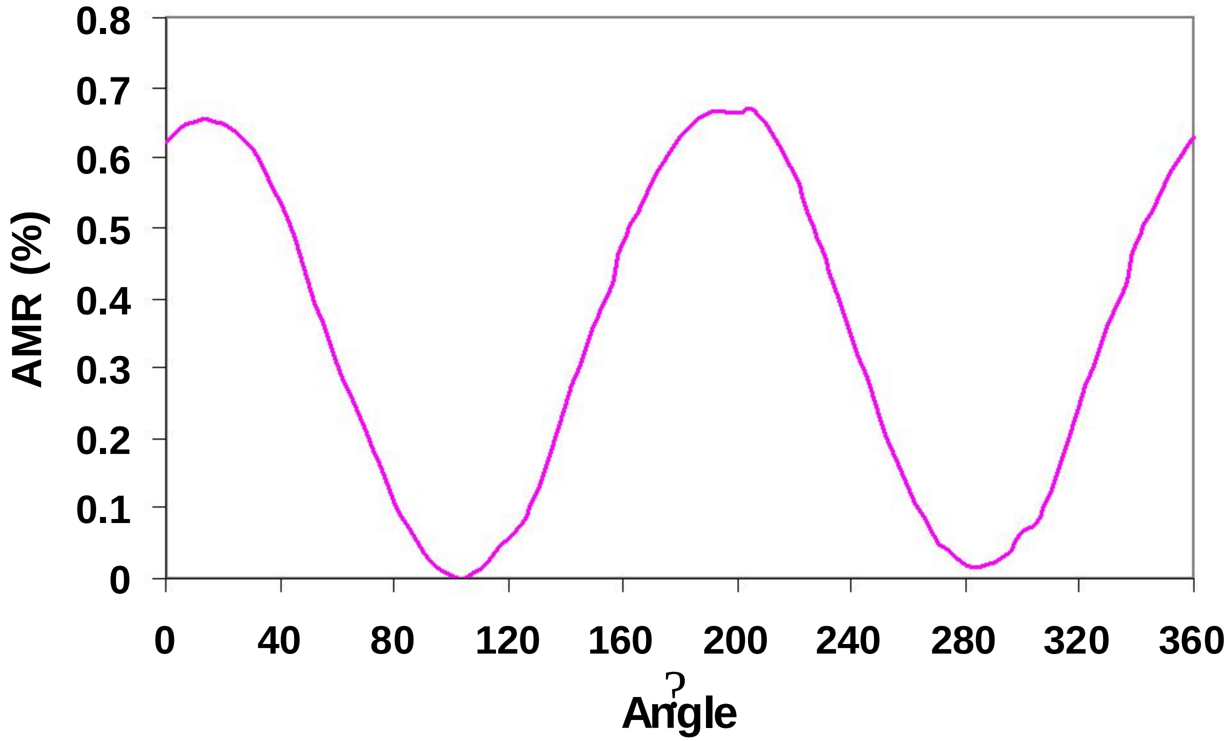
Resistance vs. Temperature



• Multilayered Co/Cu nanowires showed the metallic properties.

Anisotropic Magnetoresistance --AMR

Samples: 300*[Co(27 nm)/Cu(5nm)]

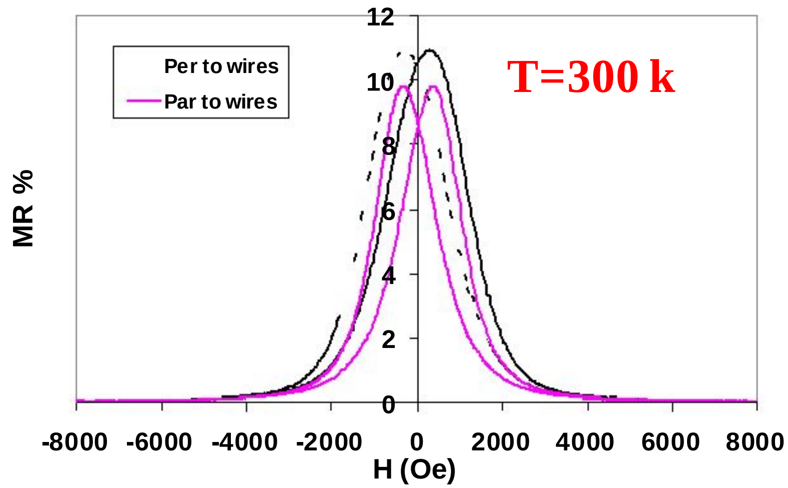


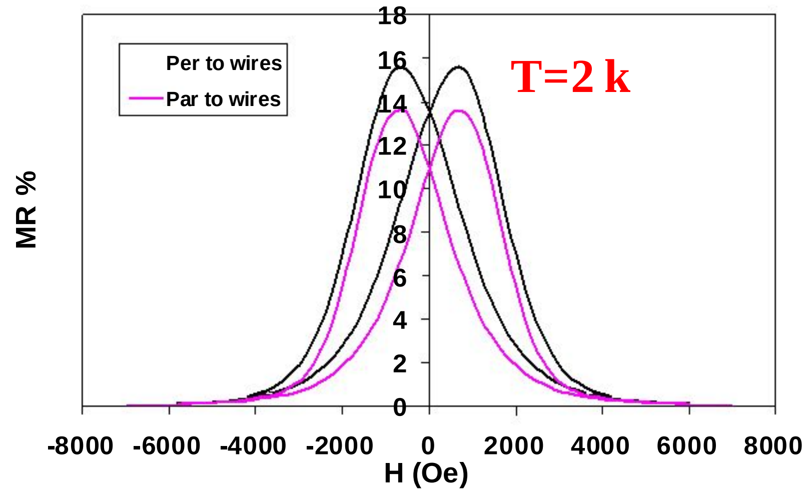
€ ? $_{max}$cos^2€ R ? ?$_{max}$ /?€

? is the angle between Ms and j.

GMR Varies with Temperature

Sample: 300*[Co(27nm)/Cu(5nm)]

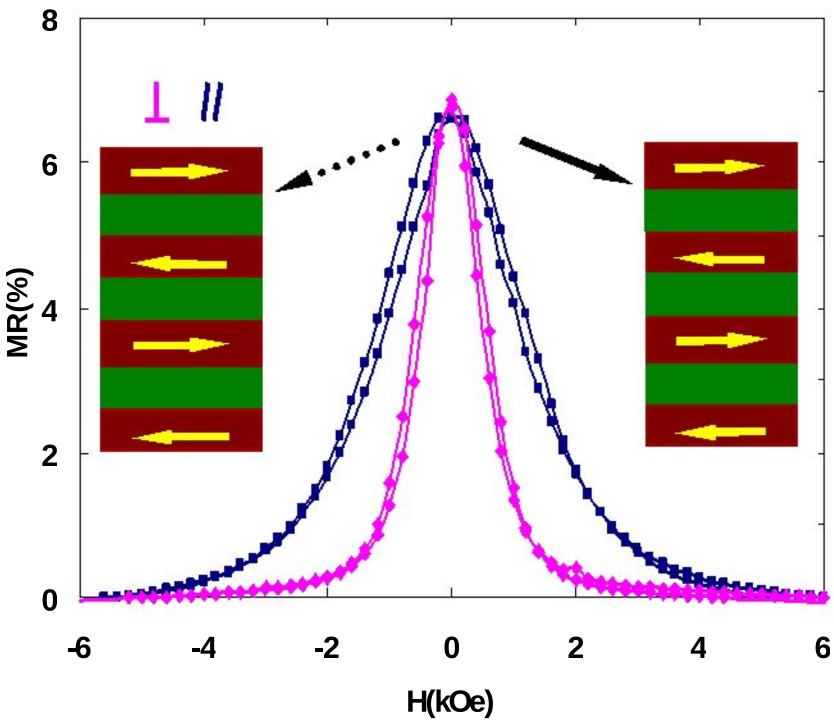




Without Lead Resistance:

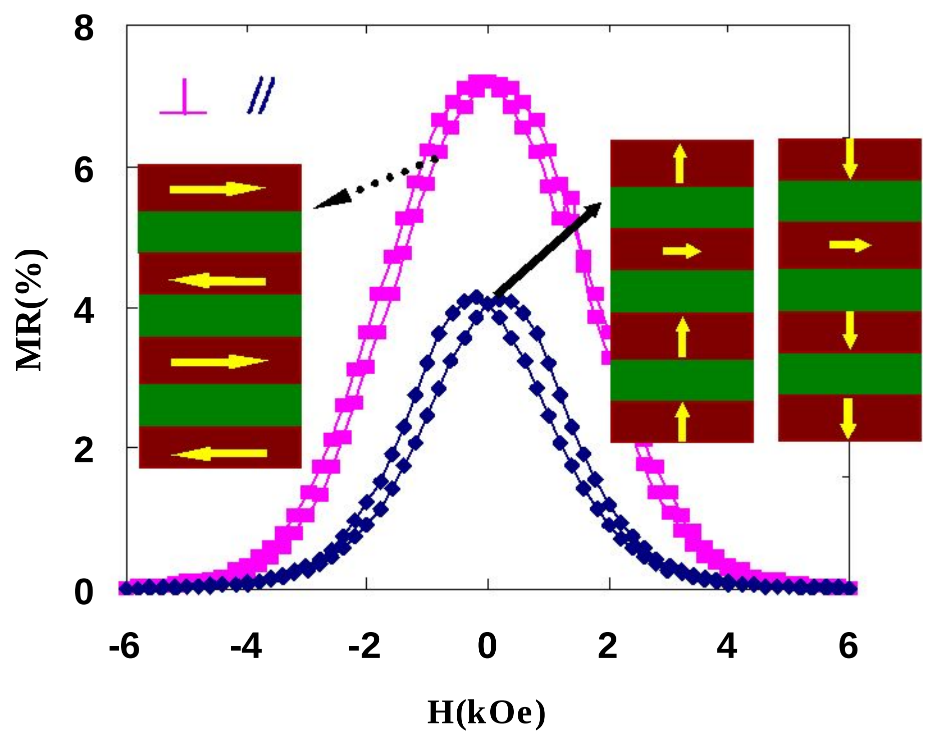
- At 300 K, MR=19% when Hper; MR=17% when Hpar.
- At 2 K, MR=30% when Hper; MR=26% when Hpar.

M-R Loops of Co/Cu Nanowires Vary with Magnetic Anisotropies



Co c-axis perpendicular to wires pH=3.4

c-axis



Co c-axis along wires pH=5.2

c-axis

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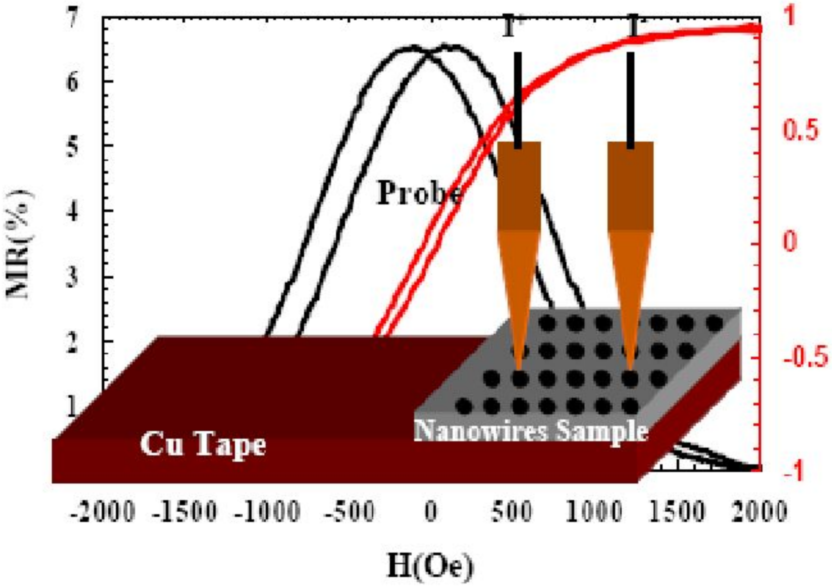
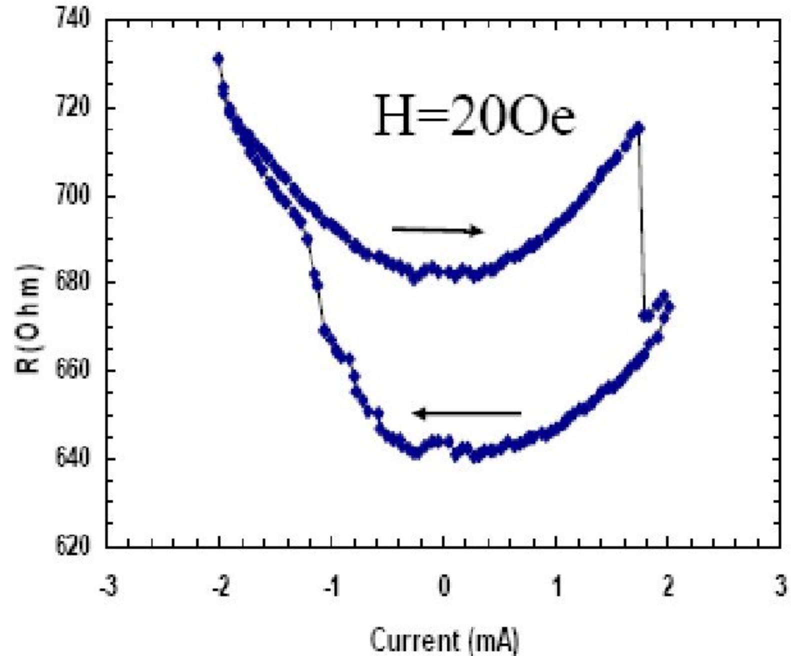
Spin Transfer Torque in Nanowires





$(Co5nm/Cu10nm)_{200}$

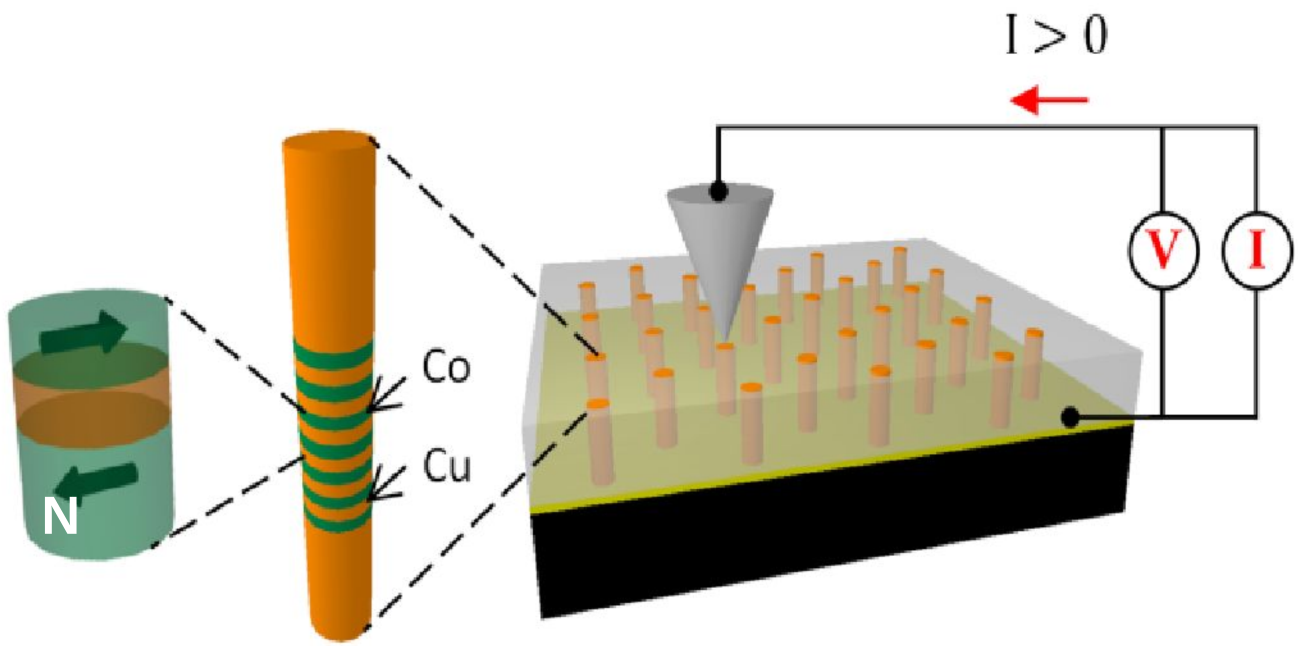
Critical current: 3-5 MA/cm^2 RA Product: 18 m^2

Includes oxide since 2 wires touched.

$_{one\ wire}$ = 9.2 cm

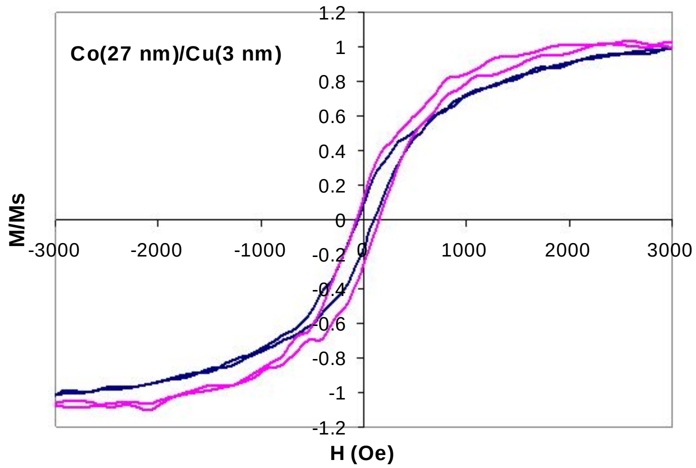
STT Measurement Setup

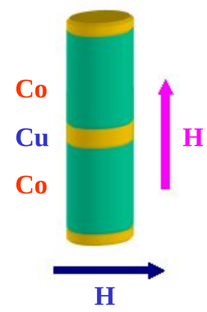
- A conductive AFM tip was used to measure STT

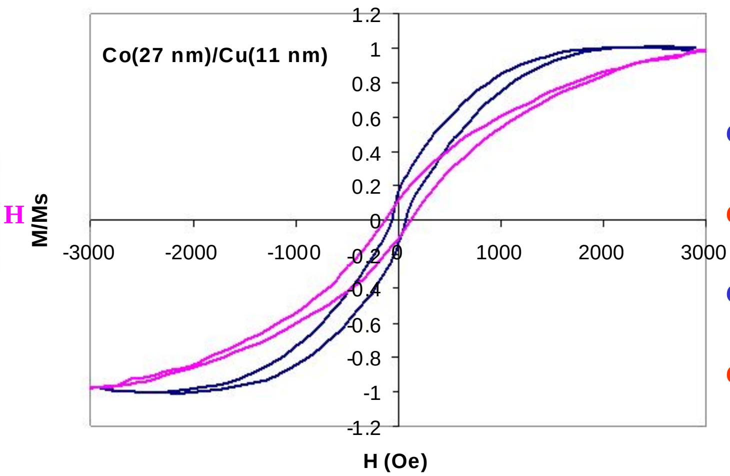


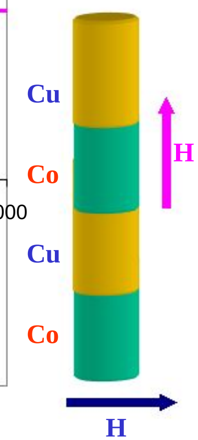
10nm diameter multilayers

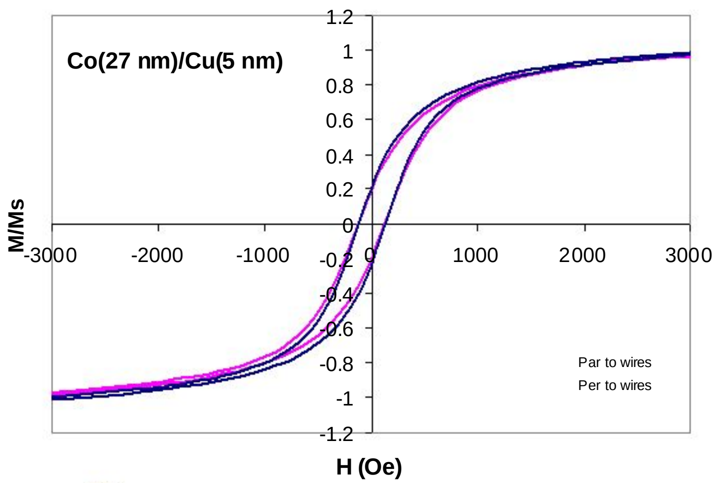
300*[Co(27 nm)/Cu(X nm)]

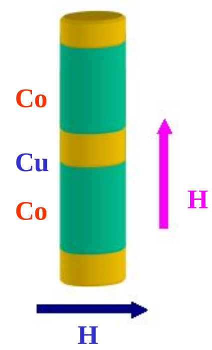








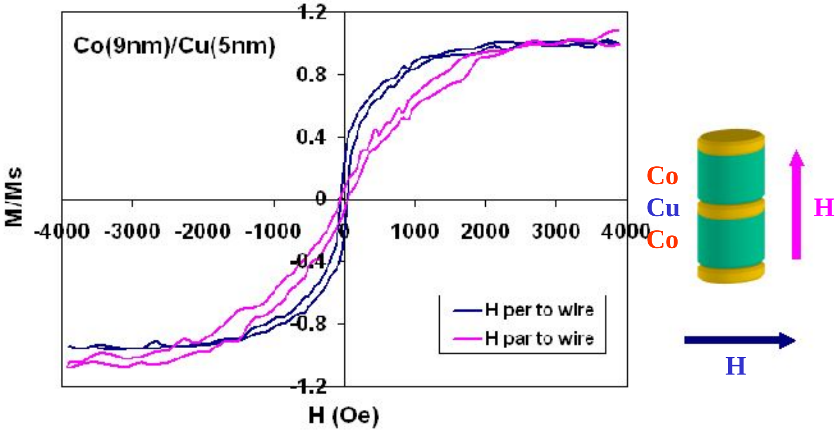


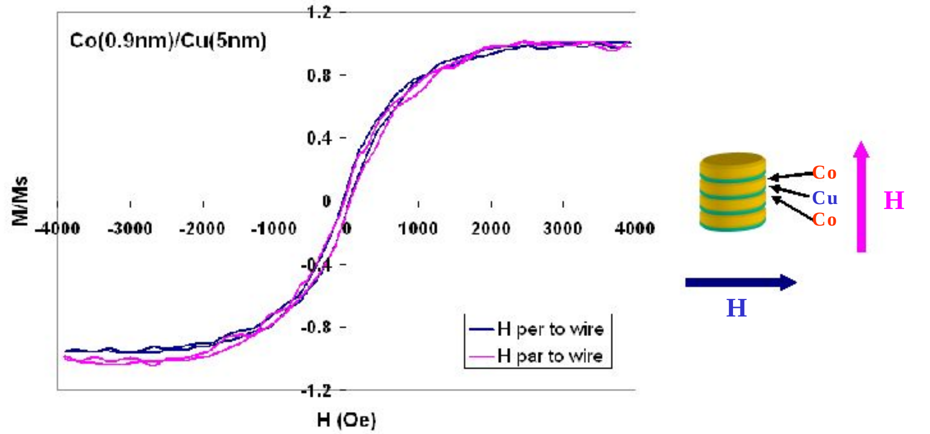


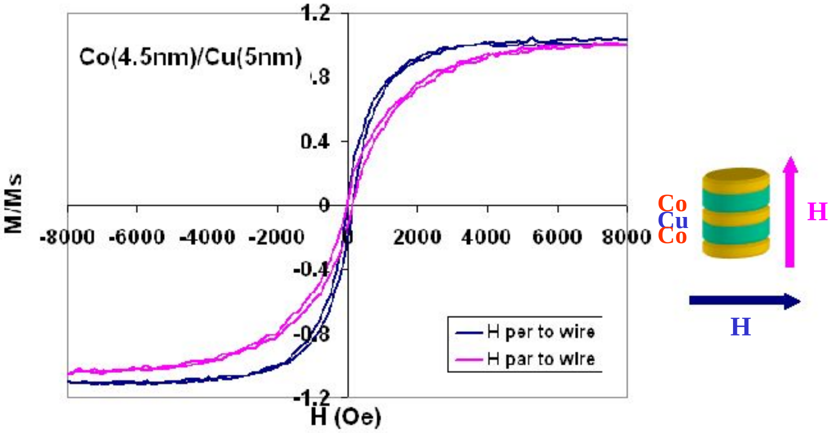
- As the Cu thickness increased, the anisotropy switched from out of plane to in plane.
- Magnetically isotropic nanowires had the highest MR.

Hysteresis Loop with Different Co Thickness

300*[Co(X nm)/Cu(5 nm)]







- Very thin layers 4.5nm Co/ 5nm Cu

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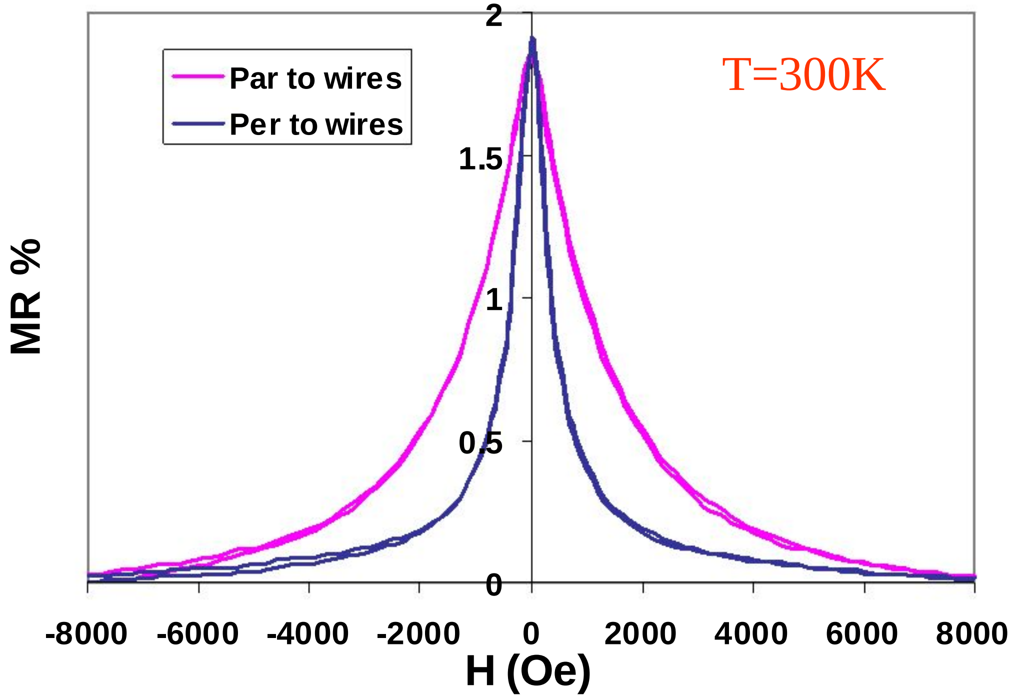
GMR -- Thinner Co Thickness

Sample: 300*[Co(4.5nm)/Cu(5nm)]



- small diameter nanopores (10nm)

-up to 18% magnetoresistance (for Cu5nm/Co4.5nm if lead R subtracted)

-R ~ 1ohm/nm for 10nm diameter wires

• MR=18% w/o lead R at 300K

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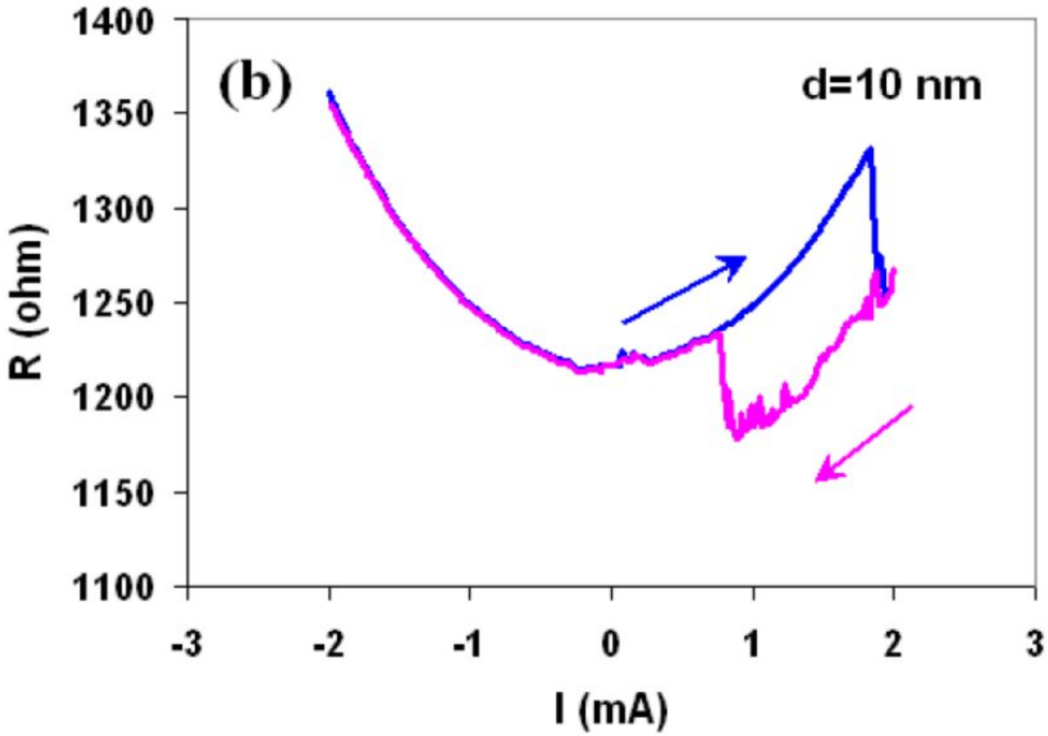
STT: 10-nm diameter multilayers



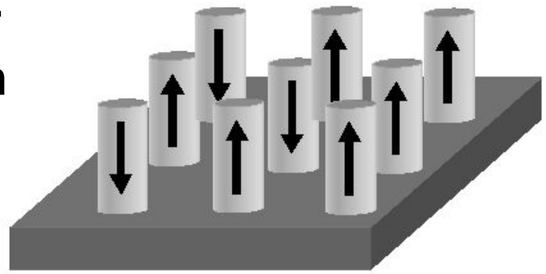
J_c: 20 x10^6A/cm^2 8% MR RA Product: 13 m^2

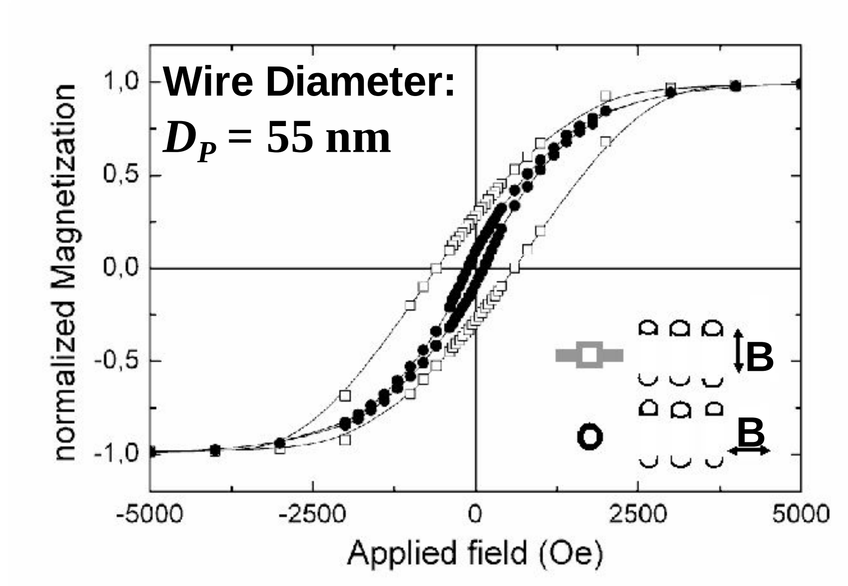
Without leads: 16% MR RA ~ 6 m^2

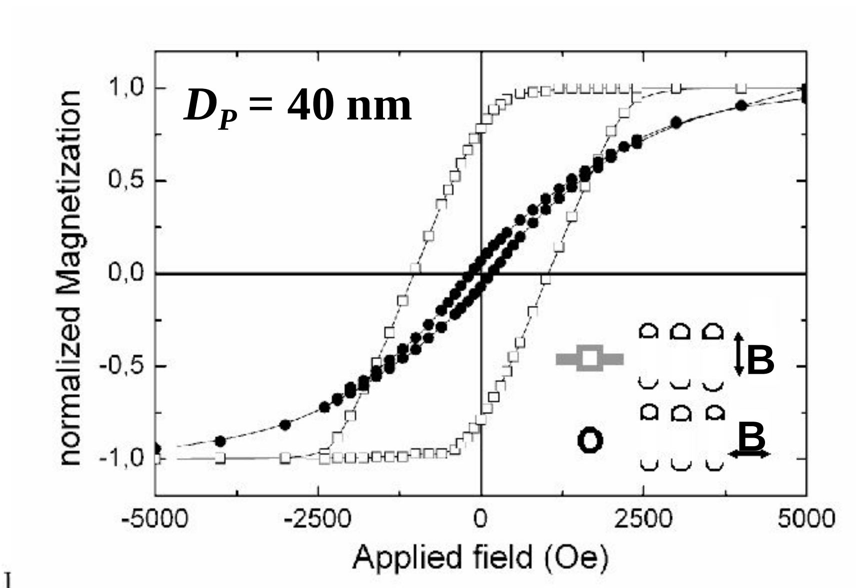
Back to Hard Drives where we started

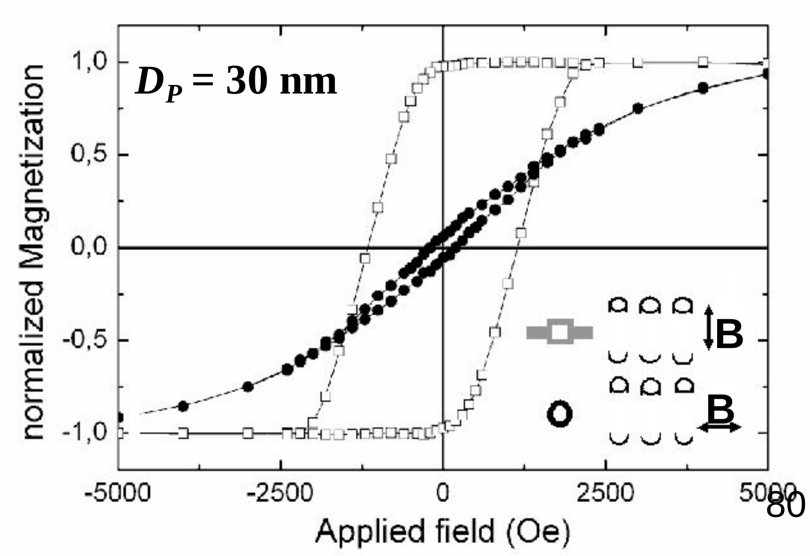
Nielsch from Hamburg Univ, Germany

Patterned magnetic medium with perpendicular magnetization

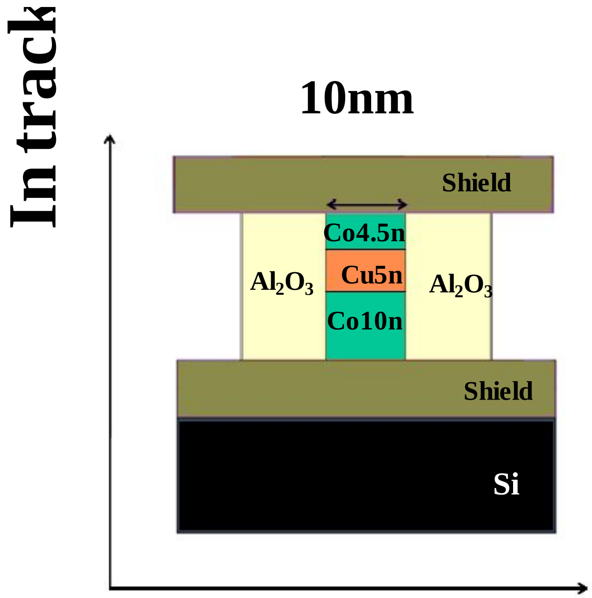






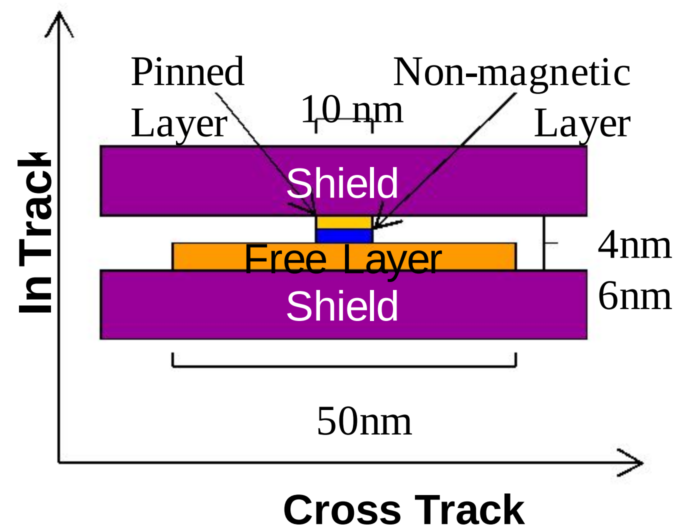


Read Heads- Trilayers



81

Cross track



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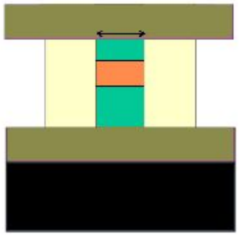
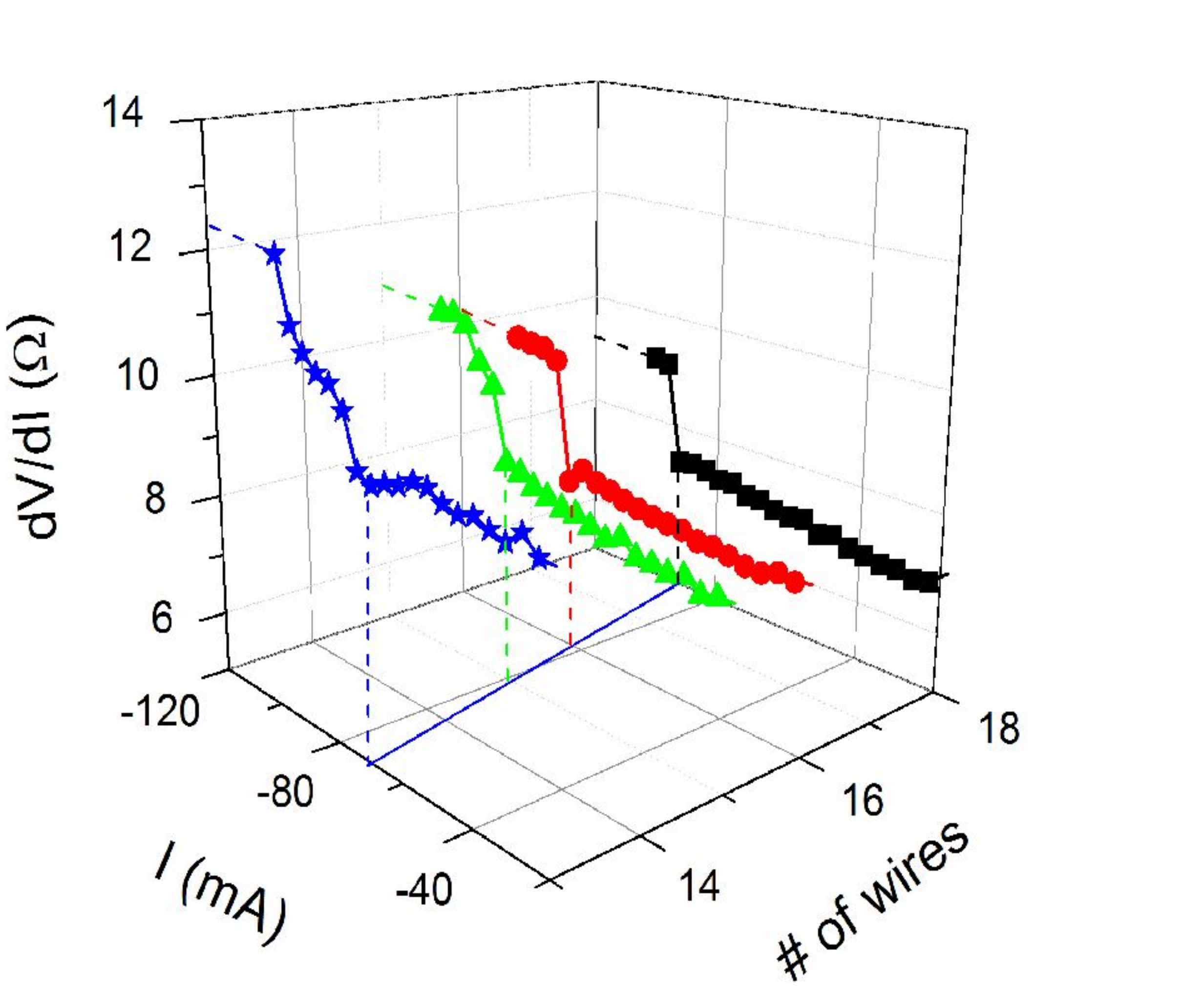
Trilayers (Co 10nm, Cu 5nm, Co 15nm)

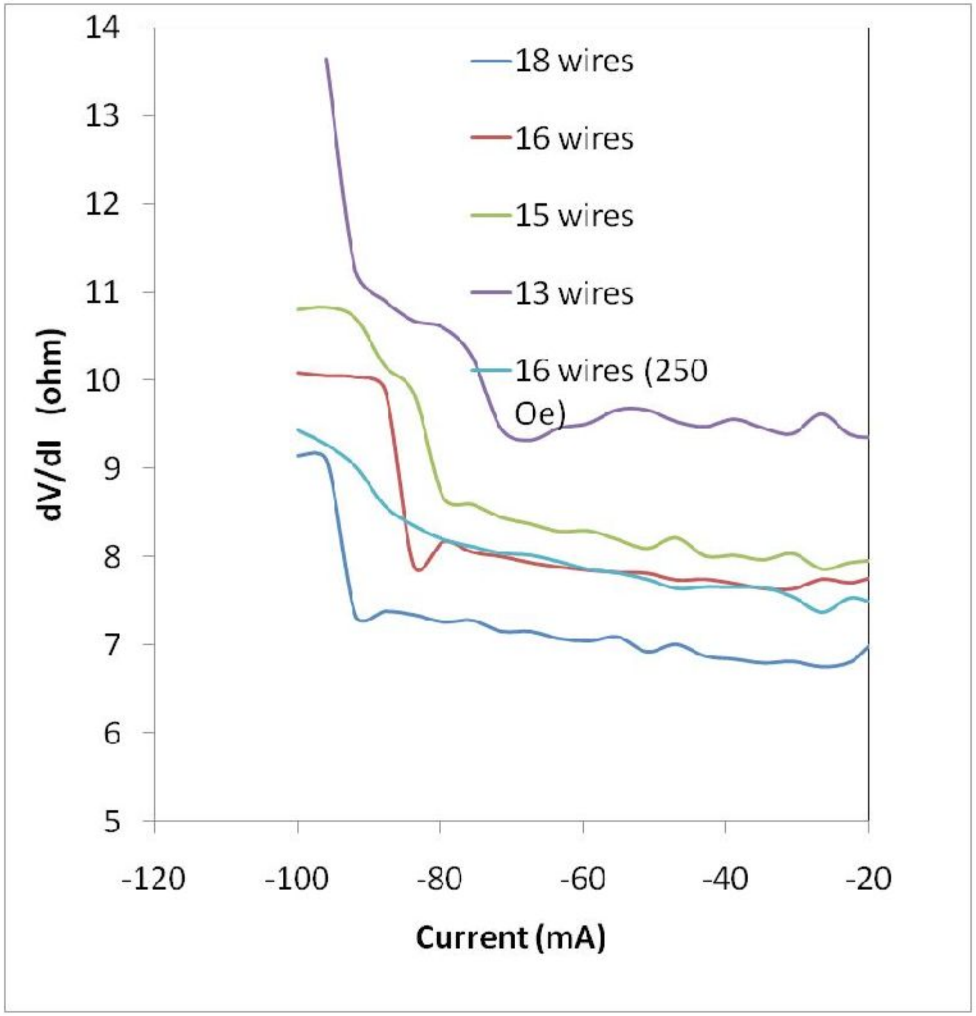




Total resistance changes with probe pressure-

Can use it to get R of single wires?

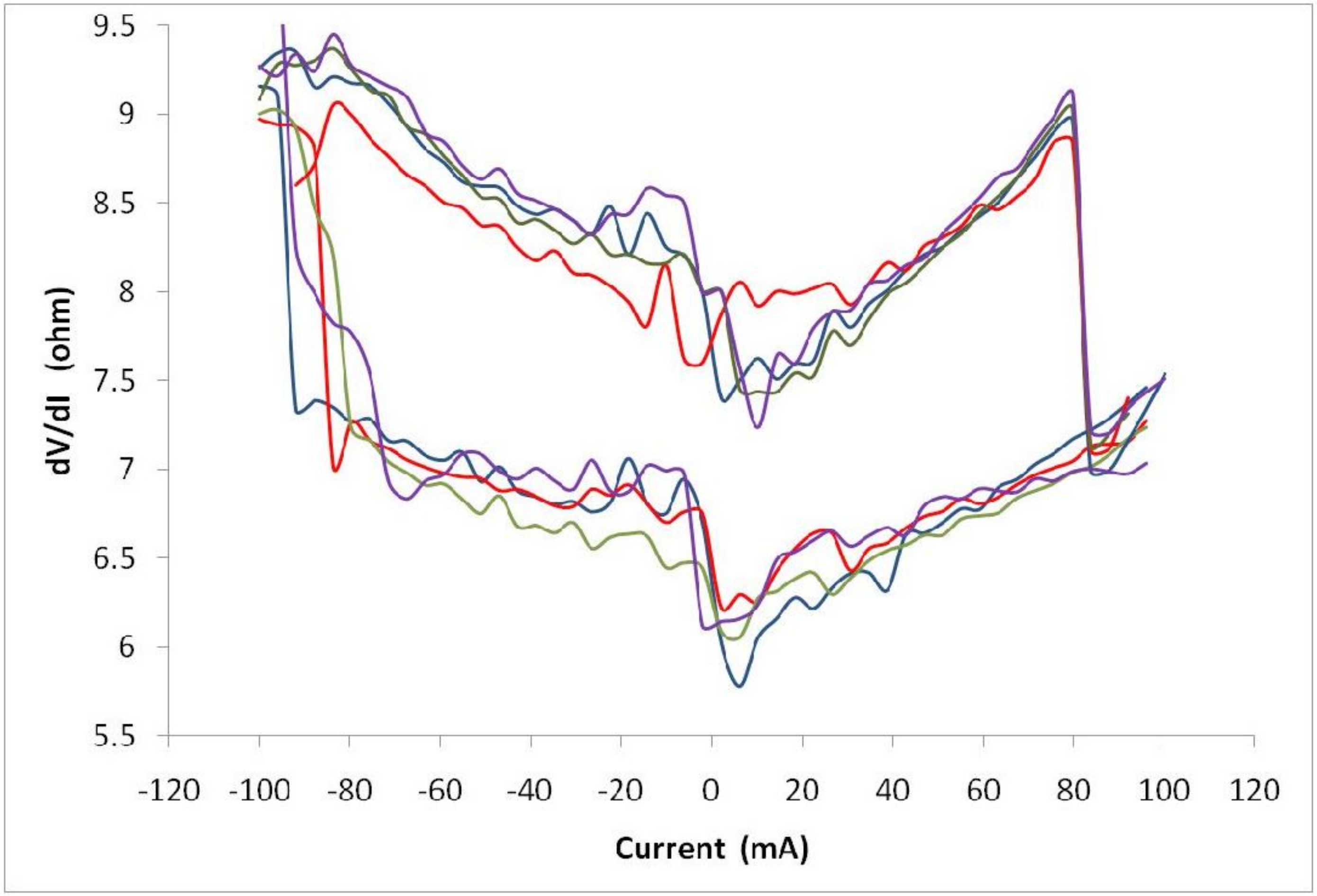
Raw Data- Current swept negative



- R decreased probe pressure increased
- Using integer values of # wires, $R_{single\ wire}$ can be found
- 190nm wires = 117

  3x resistivity of bulk

Critical Current Density agrees



R normalized to 18 wires

Calculated Jc

6.95E+09
6.79E+09
6.68E+09
6.51E+09
-6.73E+09

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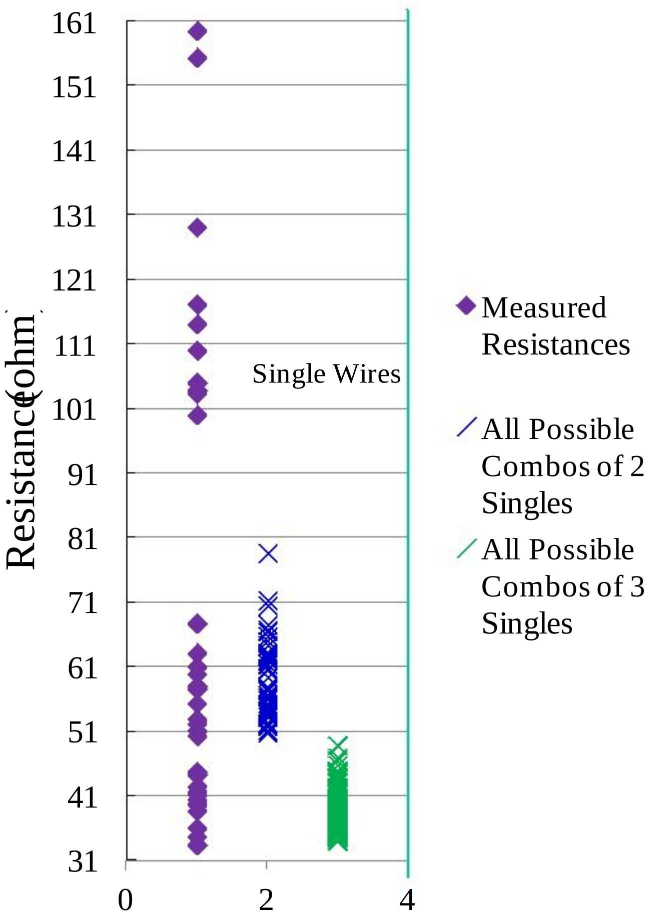
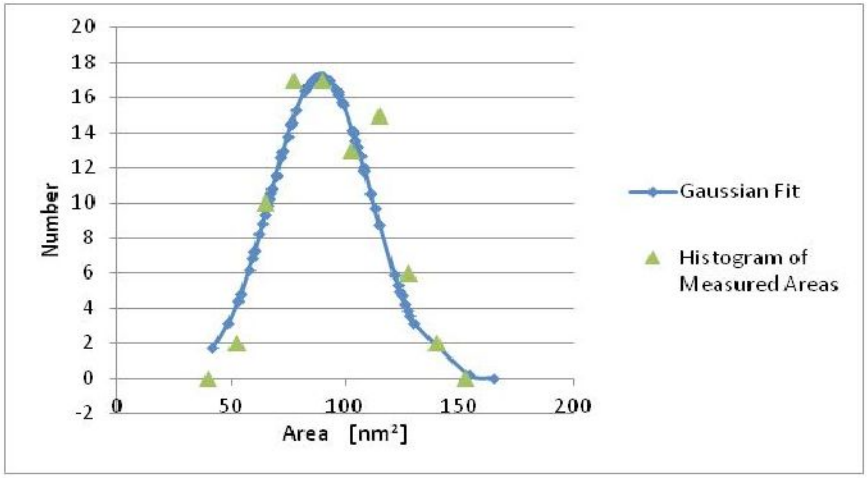
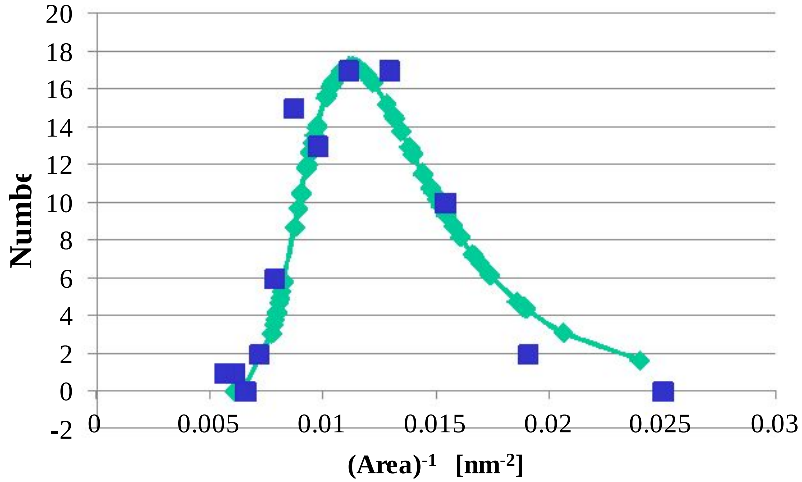
Resistivity of Single 10nm Nanowires







Review

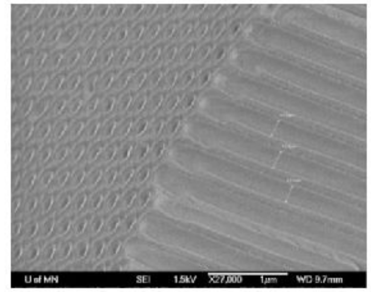
- Motivation: Memory Applications
  - Hard drives: media and heads
  - Random Access Memories

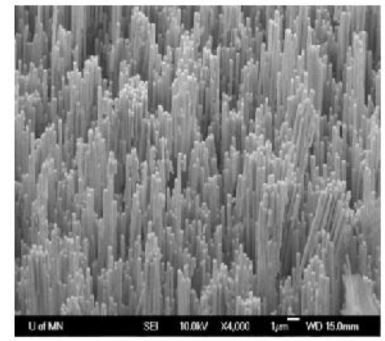
- Fabrication Techniques

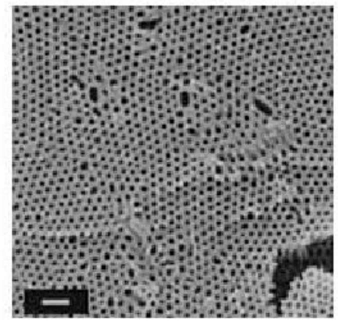
- Measuring Magnetoresistive Elements

Applications

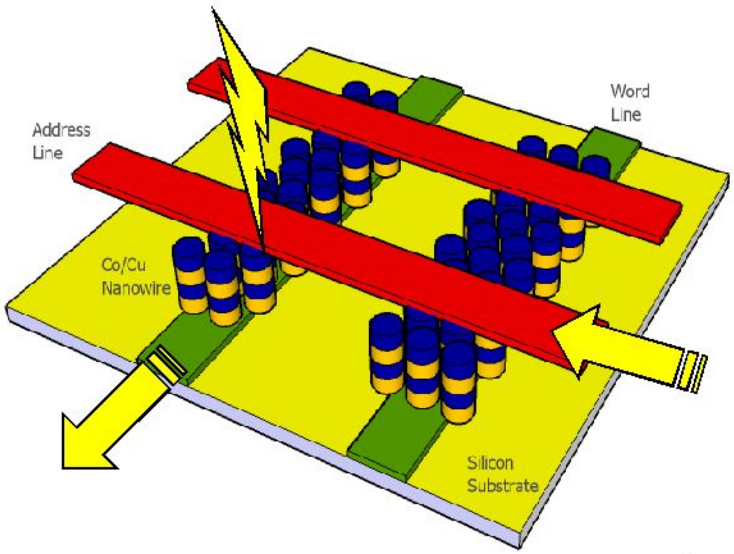
- Recording
  - Read Sensors
  - Bit patterned media (BPM)
- Random Access Memory (RAM)
- Cilia (NEMS)
- Biomagnetics

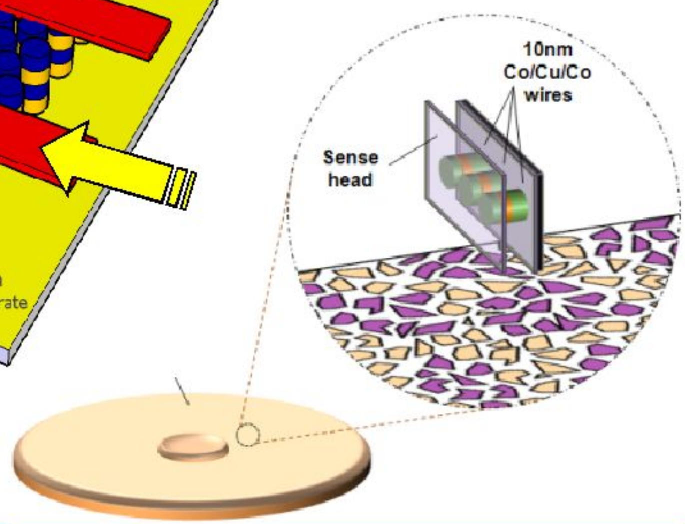


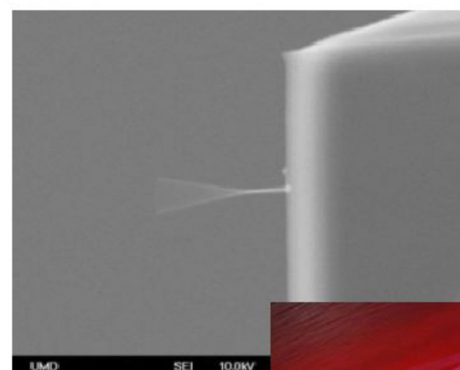


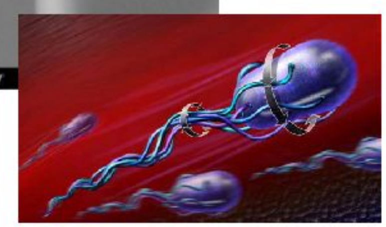


www.nano.umn.edu/omni/research









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