TexasWISE (Texas Workshop on Integrated System Exploration) 2017

IEEE CASS Outreach Initiative 2017

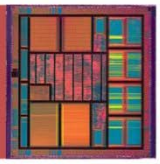
The 5th TexasWISE (Texas Workshop on Integrated System Exploration) was held at Southern Methodist University at Dallas on April 22, 2017. TexasWISE is a forum for academic scholars and industrial professionals in the field of VLSI systems to exchange the latest research results and brainstorm future research directions. This year's workshop features technical talks by prestigious technical leaders from industry as well as research stars from academia. The first talk was given by Alan Gatherer, a former TI Fellow, IEEE Fellow and current CTO of baseband research at Huawei. Alan's talk presented novel data analytic technology for wireless communication system design. The other industrial talk by Michael Polley, a senior VP at Samsung, reviewed the evolution of mobile system platforms. Eric Larson of Southern Methodist University presented his work on mobile health assisted by machine learning techniques. Recent research results on wearable electronics were showcased by J.-C. Chiao from University of Texas at Arlington. The talk by Gayatri Mehta from University of North Texas is about a novel approach to EDA computing through online games. About 20 posters were presented by students from Texas A&M University, Southern Methodist University and University of North Texas. They covered a wide range of topics including hardware security, VLSI testing, formal verification, low power design and networks-on-chip. Last but not the least, a panel discussion was held on IoT security with panelists from TI, University of Texas at Dallas, Oklahoma State University, Huawei and Southern Methodist University. This workshop attracted about 80 attendees from Texas universities and industry. It was sponsored by Southern Methodist University, Texas A&M University and University of Texas at Dallas. It was chaired by Prof. Jennifer Dworak from Southern Methodist University. In earlier years, the workshop has been held at University at Texas at Austin and Rice University.

Call for Participation

What is TexasWISE?

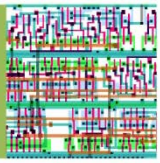
Texas Workshop on Integrated System Exploration (TexasWISE) is a one-day workshop to be held in Dallas, TX on April 21, 2017, sponsored by SMU, Texas A&M University, UT Dallas and UT Austin. It will consist of several plenary talks by distinguished speakers in the VLSI area, a student poster session, a panel session and time for interaction with industry and academic participants.

Why Attend TexasWISE?



- ✓ For **industrial professionals**, this is a wonderful opportunity for inspiring new product ideas, recruiting top students at Texas, and networking for future career.
- ✓ For **academic researchers**, this is a precious chance for discovering new research directions, interacting with industrial participants and understanding their research needs.
- ✓ For **students**, this is a great time for learning the latest technology trend, making new friends and finding job opportunities.

Workshop Registration



There will be no registration fee. However, registration is required to secure a seat for you, and it is in a first-come-first-serve basis.
Please register on-line at https://www.smu.edu/Lyle/AboutUs/Calendar/TEXASWISE2017/Registration

Program Overview

AM

- Keynote Speakers from Industry, Academia, and Government

PM

- Poster Session
- Keynote Speakers from Industry, Academia, and Government

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Program

TexasWISE, 2017 Southern Methodist University http://texaswise.tamu.edu/program2017.html	
8:30 am	Registration
9:00 am to 9:45 am	Alan Gatherer, Huawei
9:45 am to 10:30 am	Gayatri Mehta, UNT
10:30 am to 11:00 am	Coffee Break
11:00 am to 11:45 am	Michael Polley, Samsung
11:45 am to 12:45 pm	Lunch
12:45 pm to 1:30 pm	Eric Larson, SMU
1:30 pm to 2:15 pm	J.-C. Chiao, University of Texas at Arlington
2:15 pm to 3:30 pm	Poster Session
3:30 pm to 4:30 pm	Panel

Keynote Speakers

Alan Gatherer
On behalf of Ywh-Pyng Harn
Huawei

Title: The rise of Statistical Modeling and Data Science in IP and system level design

Abstract: As the era of 5G is emerging, we are facing more and more complex and challenging wireless system design. For this aspect, this talk is aimed at providing academic researchers ideas about the kind of problems the industry is facing, as well as how we approach the problem for a solution. In the first part, we will show that statistical and mathematical modeling is an excellent technique to provide guidelines and design direction in the early stages of system development, before a cycle-accurate model exists. In the second part, we will discuss how data science can be applied and now become indispensable for very large-scale and complicated system design.

Biography (Ywh-Pyng Harn) Ywh-Pyng Harn got his BS and MS degrees from National Taiwan University, and Ph.D. degree from UC Berkeley, all from the Department of Electrical Engineering. He worked for companies like Integrated Systems, Avanti, Broadcom and Cadence in the area of optimization-based control system design and IC physical layout design automation. He joined Huawei in July, 2013, and is currently working on next-generation system architecture exploration and optimization.

Biography (Alan Gatherer) Alan Gatherer is the CTO for Baseband System on Chip in Huawei Technologies, USA and Fellow of the IEEE. He is responsible for R&D efforts in the US to develop next generation baseband chips and software for 3G and 4G basestation modems. His group is presently developing new technologies for baseband SoC in the areas of message passing hardware and middleware, isolation for multimode, interconnect fabric, CPU/DSP clusters and virtualization. Recently they have focused on open systems, SLA enforcement and now 5G requirements. Alan joined Huawei in January 2010. Prior to that he was a TI Fellow and CTO at Texas Instruments where he led the development of high performance, multicore DSP at TI and worked on various telecommunication standards. Alan has authored multiple journal and conference papers and is regularly asked to give keynote and

plenary talks at communication equipment conferences. In addition, he holds over 70 awarded patents and is author of the book “The Application of Programmable DSPs in Mobile Communications.” Alan holds a bachelor of engineering in microprocessor engineering from Strathclyde University in Scotland. He also attended Stanford University in California where he received a master's in electrical engineering in 1989 and his doctorate in electrical engineering in 1993

Eric Larson
SMU

Title: : Flipping the Clinic with Mobile Machine Learning

Abstract: Mobile health technology has long been touted as a solution to global health access, allowing remote diagnosis, low cost disease management, and rapid training of health workers. The mHealth “revolution” has promised to deliver in-home health care that parallels the care we might receive in a physician’s office. However, the panacea of digital health has proven to be more problematic and messy than its vision, especially for collecting and interpreting medical quantities from the home. In this talk, I cover a number of existing research projects that lower the cost of sensing by offloading the computation to a mobile phone. I examine the hurdles in performing this research, including the importance of evaluating solutions with realistic context.

Biography: Eric C. Larson is an Assistant Professor in the department of Computer Science and Engineering in the Bobby B. Lyle School of Engineering, Southern Methodist University. Dr. Larson has developed a number of mobile health technologies; including medical applications that use mobile phone's to track baselines for patients with pulmonary ailments, depression, and neonatal jaundice. Dr. Larson's main research interests are in machine learning, sensing, and signal & image processing for ubiquitous computing applications, in particular, for healthcare and education. His work in both areas has been commercialized and he holds a variety of patents for embedded sensing and machine learning in mobile phone-based health sensing. Dr. Larson has more than 30 research publications, 2 books, and 7 patents. He received his Ph.D. from the University of Washington in 2013.

Michael Polley
Samsung

Title: Mobile Platform Evolution

Abstract: Considering industry trends and increased market demands for better, faster and smarter mobile devices, this presentation will contrast computational capabilities of embedded devices with the evolving requirements of new and existing mobile equipment and applications. In addition to considering how to match next-generation devices with the needs, we will also consider what part of the system should be on-device versus in the cloud.

Biography: Mike is Senior Vice President and Head of the Mobile Processor Innovation Lab at Samsung where he leads a team of world-class algorithm and system designers and chipset architects focused on creating new technologies for next-generation smartphones and wearable devices. Prior to Samsung, Mike worked at Texas Instruments for 18 years defining chipset architectures and leading embedded signal processing R&D. He was recognized for his technical accomplishments by election to TI Fellow in 2009. Mike received his B.S., M.S., and Ph.D. degrees in electrical engineering from MIT. He holds 32 U.S. patents on a broad range of products across communications and multimedia systems.

Gayatri Mehta
UNT

Title: : Interactive Game-Like Design Environments for Electronic Design Automation

Abstract: Custom reconfigurable computing platforms offer low power and high performance for a suite of applications. They can be tailored according to the needs of an application domain. The ability to

successfully create these highly customized domain-specific reconfigurable architectures offers tremendous advantages, including orders of magnitude power savings, longer battery life, smaller, faster, more robust devices, and shorter time to market. However, making extreme customization an integral part of the design process requires design to be significantly simpler and easier to create novel, out of the box architectures that directly address the requirements of a specific application domain. This challenge can be categorized into three areas: (1) discovering faster and efficient algorithms that allow exploring design space rapidly; (2) broadening participation by promoting computational thinking among non-scientists and non-engineers; and (3) educating the next generation of custom chip designers through innovative highly visual interactive frameworks.
In this talk, I will present the interactive design frameworks that we have developed to harness human intelligence to discover efficient algorithms for mapping and architecture design. People excel at navigating complex and dynamically changing situations, recognizing recurring patterns, and identifying potential opportunities. I will show that these reasoning and problem solving skills can be brought to bear in solving real problems in Electronic Design Automation. Our mapping game, UNTANGLED has received People's Choice Award in the Games & Apps category of the 2012 International Science and Engineering Visualization Challenge conducted by the National Science Foundation and Science.

Biography: Gayatri Mehta is currently an Associate Professor in the department of Electrical Engineering at the University of North Texas, Denton, TX. She received her Ph.D. in Electrical and Computer Engineering from the University of Pittsburgh in 2009. Her research interests are broadly in the areas of Electronic Design Automation, Reconfigurable Computing, Low-Power VLSI Design, System on a Chip Design, Embedded Computing, and Portable/Wearable Computing.

J.-C. Chiao
University of Texas at Arlington

Title: : Flipping the Clinic with Mobile Machine Learning

Abstract: Mobile technologies have changed our life style significantly. Personalized tools such as wearable and implantable devices through wireless communication and Internet of Things have been utilized in healthcare to provide unique functions and reduce costs. Individuals can be empowered with tailored solutions without limitation in mobility or daily activities. Quantitative documentation of physiological parameters presents more accurate assessment. Direct stimulation on tissues or organs by electrical signals can restore or improve body functions. Continuous monitoring and adaptive administration of therapy to treat symptoms via wireless body networking can adaptively optimize the closed-loop health management. This presentation discusses the development of wireless micro devices and integrated systems for clinical applications. The systems are based on batteryless, wireless implants with enhancement in miniaturization and functionalization. Miniaturization owing to flexible substrates and the elimination of bulky batteries allows endoscopic or minimally invasive procedures to deploy the implants without painful surgeries. Several diagnosis and therapeutic treatment examples for management of gastric and neural disorders, particularly as closed-loop systems, will be introduced. These examples aim to inspire new system application ideas to address the implementation and cost challenges in healthcare, and enable integration of electronics and medicines to improve human welfare and assist better living.

Biography: J.-C. Chiao is Greene professor and Garrett professor of Electrical Engineering at University of Texas – Arlington. He received his PhD at Caltech and was with Bellcore, University of Hawaii-Manoa and Chorum Technologies before he joined UT-Arlington in 2002. Dr. Chiao has published more than 260 peer-reviewed papers and received 12 patents. He received the 2011 O'Donnell Award in Engineering presented by The Academy of Medicine, Engineering and Science of Texas. He received the Tech Titan Technology Innovator Award; Lockheed Martin Aeronautics Excellence in Engineering Teaching Award; Research in Medicine milestone award by Heroes of Healthcare; IEEE MTT Distinguished Microwave Lecturer; IEEE Region 5 Outstanding Engineering Educator and individual Achievement awards. Currently, he is an IEEE Sensors Council Distinguished Lecturer and serving as the Editor-in-Chief for Journal of Electromagnetics, RF and Microwaves in Medicine and Biology. More information about him can be found at his website .

Panelists

David Pan (*Panel Moderator*)
UT Austin

Daniel Engels
Southern Methodist University

Rama Venkatasubramanian
TI

Alan Gatherer
Huawei

Jeyavijayan(JV) Rajendran
University of Texas at Dallas

Jingtong Hu
Oklahoma State University

Xiaolin Lu
TI

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Venkateshwar Kottapalli and Flemming Andersen.
Formal Property Verification of a MESI-based Cache Implementation

Abstract: The design and verification of cache coherency is complex due to non-atomic transitions in hardware implementation. Simulation-based techniques fail to ensure the absence of design failures. Formal methods can identify the numerous race conditions and corner cases. In this study, we perform formal property verification (FPV) of a 4-core snooping cache design with private L1 cache, shared L2 cache, and an atomic bus. We present the advantages of FPV over a state of the art UVM verification environment.

Ignatius Praveen Lawrence and Duncan Walker.
Optimal Test Conditions and Scenario for Detecting Resistive Opens in Latches and Flip-Flops

Abstract: Stuck-At and Transition Delay Fault models have been used to screen defective chips. These fault models are not sufficient to detect resistive opens. Our work proposes aggressive test conditions and scenario for detecting subtle resistive opens. The aim is to improve quality of chips especially in safety critical applications.

Hui Jiang and Jennifer Dworak.
Enhancing Cell-Aware Fault Detection through Intelligent Use of Scan Shift Cycles

Abstract: In this paper, we investigate the ability of the intervening shift cycles to achieve high static cell-aware fault coverage using only the test patterns generated to detect stuck-at faults. We also investigate reducing the number of shadow flops required. Our results show that high cell-aware coverage is achievable even when only a stuck-at test set is applied—in some cases equal to the coverage obtained by a dedicated cell-aware test set.

Jiafan Wang and Jiang Hu.
Thwarting Analog IC Piracy via Combinational Locking

Abstract: A combinational locking technique is introduced to enhance analog IC security against piracy. The kernel idea is reconfigurable current mirror design using Satisfiability Modulo Theories. With the locking system, only a single key value can make analog IC operate properly. The effectiveness is confirmed by simulations on analog IC designs.

Shilpi Sharma and Rashaunda Henderson.
Predictive Method for Multiplexing Laguerre-Gaussian Beams at Radio Frequencies

Abstract: This research focuses on developing predictive techniques to combine with experimental demonstrations of orbital angular momentum multiplexing. Laguerre Gaussian beams contain an orbital angular momentum phase term, which can be exploited to increase the data rate of communication systems. Using MATLAB toolkits we are trying to build a numerical framework for multiplexing and demultiplexing message signals in E-band (73 GHz) that we have carried out using impulse radios.

Abbas Fairouz and Sunil Khatri.
A Comparison of Low Standby Power Techniques for an Asynchronous NoC Router

Abstract: The Network-on-Chip (NoC) paradigm is now widely used to interconnect the processing elements (PEs) in a chip multiprocessor (CMP). It has been reported that the NoC consumes about a third of the total power consumption of the multi-core processor. To address this, asynchronous NoC routers have been proposed, to eliminate the clocking power associated with the NoC implementation. In this work, we present a comparison of techniques to reduce the standby power of a state-of-the-art asynchronous NoC router.

Wenbin Xu and Jiang Hu.
A Simple Yet Efficient Accuracy Configurable Adder Design

Abstract: Approximate computing is a promising approach to low power IC design and recently received considerable attention. In this work, we investigate a simple accuracy configurable adder design that contains small redundancy and uses very simple carry prediction. Simulation results show that our design dominates previous work on accuracy-delay-power tradeoff while uses 39% less area.

Mallika Pokharel and Duncan M. (Hank) Walker.

Multi-cycle At Speed Test

Abstract: We use multiple functional cycles for compacting K-longest paths per gate to generate minimal patterns. Each path delay test is compared to at-speed patterns in the pool. We try to place each path in the first pattern in first capture cycle. If it fails, we exploit other capture cycles.

Abbas Fairouz and Sunil Khatri.

Design of a Hardware Hash Unit for use in Modern Microprocessors

Abstract: In recent times, applications such as cloud computing, web-based search engines, and network applications are widely used. Hashing is a key algorithm that is extensively used in such applications. Thus, implementing a hardware-based hash unit as a new special function unit on a modern microprocessor would potentially increase performance significantly. In this work, we present the microarchitecture and circuit designs for a hardware hash unit (HU) for modern microprocessors.

Zachary Simpson and Gayatri Metha.

Solving Complex and Constrained Mapping Problems using Interactive Design Framework

Abstract: Untangled III is an online interactive mapping/placement game to harness human intelligence for large, complex, and constrained mapping problems. This game is broadly accessible and it does not require any engineering background to play. Players can easily build upon other players' solutions using the community play feature of the game.

Yi Sun and Jennifer Dworak.

Using FPGA as a Tester in a 3D stacked IC

Abstract: Using FPGA as a tester in a 3D stacked IC provides options for different testers for different company, using an FPGA as a tester reduces the power consumption when compared to Embedded Deterministic Test.

Gity Karami and Jeff Tian.

Improving Web Application Reliability and Testing Using Accurate Usage Models

Abstract: Markov OP is a good candidate for effective web quality and reliability assurance because it captures the behavior of web components and related navigation facilities to support usage based statistical testing (UBST). The accuracy of such usage models would affect the effectiveness of quality assurance and testing activities. We examine the impact of accurate usage models on reliability, test coverage, and test efficiency.

Soha Alhelay and Jennifer Dworak.

Detecting a Trojan Die in 3-D Stacked Integrated Circuits

Abstract: 3D integrated circuits introduce both advantages and disadvantages for security. Among the disadvantages unique to 3D is the potential insertion of a Trojan die into the stack between two legitimate dies. We propose a Trojan detection technique and the required architecture to measure the propagation delays across the 3D dies to detect and locate the extra die in a 3D die stack.

Nirosha Dinayadura and Armin Mikler.

An Efficient Approach for Outbreak Preparedness for Dengue

Abstract: Dengue is the world's fastest growing vector-borne disease. An efficient integrated solution that addresses broad aspects of the dengue mitigation is presented. Support Vector Regression ensemble; dengue epidemic prediction; and a development of a surveillance system to effectively monitor case data were cooperatively implemented in the proposed system.