Project-Based Learning in Digital Fundamentals Course Using FPGAs

Dingjuan Chua, Jieyi Gao, Massimo Alioto, Yong-Ping Xu and Sangit Sasidhar
National University of Singapore, elechuad@nus.edu.sg

***Abstract*— As embedded systems become integral in both academia and industry, hardware description languages are becoming a requisite part of Electrical and Computer Engineering curricula. The implementation of project-based learning in a freshman Digital Fundamentals course using an FPGA platform allows for greater engagement and learning through interesting and real-world projects. Through this approach, students strengthen the conceptual links between hardware description languages and circuit hardware while developing the ability to manage complex systems with multiple levels of abstraction. This paper discusses the implementation of three different application-driven projects on the Basys-3 trainer FPGA platform at the National University of Singapore and evaluates the effects of the key pedagogical differences. Both qualitative and quantitative assessment results are presented, showing how students perceived these projects and met the learning objectives.**

I. INTRODUCTION

As modern embedded systems become ubiquitous, traditional discrete logic gates and programmable logic devices on breadboard implementations are being replaced by field-programmable technology such as field-programmable gate arrays (FPGA) in both academia and industry. Instruction in hardware description languages and FPGAs are thus being incorporated into foundation courses on digital logic design [1]-[4]. Through FPGAs, students are enabled in designing larger, more exciting systems and have almost instant feedback via simulation or verification. This also allows students to learn about design flows that are used in the industry for developing commercial products in embedded systems and ASICs.

Project-based learning contextualized in real-world systems or applications that these students have already been exposed to can engage and excite these students much more as they are enabled to create and innovate. Through building these digital hardware applications, students are introduced to fundamental engineering principles, strengthen the conceptual links between hardware description languages and circuit hardware while developing the ability to manage complex systems with multiple levels of abstraction.

This paper is organized as follows: section II describes the Digital Fundamentals course at the National University of Singapore while section III describes three application-driven projects that have been successfully implemented in this course. Section IV describes the quantitative and qualitative assessment on the effectiveness of the course design projects and section V concludes the paper.

II. DIGITAL FUNDAMENTALS COURSE

The Digital Fundamentals module at the National University of Singapore is a required foundation course for electrical engineering and computer engineering students. The students typically take this course in semester 2 or semester 3 of their studies. The four/five modular credit course is conducted over thirteen weeks for large class sizes of 200 to 250 students. In 2014, the course was revised to fully incorporate modern digital circuit implementation technologies with the use of hardware description languages (HDLs) and FPGAs. The curriculum was revised to introduce HDLs in tandem with circuit hardware in lectures that are supplemented by lab and project activities which provide hands-on hardware experiences for practice and reinforcement of concepts. The alignment between lectures and hands-on activities helps students to develop a stronger coherence between HDLs and circuit hardware and lays the foundation for subsequent courses in embedded hardware systems and advanced digital design.

A. Hardware

The FPGA development board used in the Digital Fundamentals module is the Basys 3 Artix-7 FPGA Trainer Board by Digilent [5], designed for introductory users of FPGA technology. This trainer board is to be used exclusively with the Xilinx Vivado Design Suite (for which the WebPACK edition is made available to university students). The Xilinx Artix-7 FPGA contains 33,28 logic cells in 5200 slices (each slice contains four 6-input LUTs and 8 flip-flops) and supports 1,800 Kbits of fast block RAM and 90 DSP slices. The trainer board features :

- On-chip analog-to-digital converter
- Digilent USB-JTAG port for FPGA programming and communication
- Micro-B USB cable not included.
- Serial Flash
- USB-UART Bridge
- 12-bit Video Graphics Array (VGA) output
- USB HID Host for mice, keyboards and memory sticks
- 16 user switches and LEDs
- 5 user pushbuttons
- 4-digit 7-segment display
- 4 Pmod ports: 3 Standard 12-pin Pmod ports, 1 dual purpose XADC signal / standard Pmod port

This FPGA trainer board was chosen as it came complete with ready-to-use software and hardware, was at a student-level price point and had multiple on-board I/O devices. Most

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importantly, there was great potential for expansion with Digilent's line of Pmod I/O interface boards that extend the capabilities of the FPGA boards. Each device comes with reference manuals, code examples and user guides on the Digilent website which greatly enhances accessibility to the students and supports independent learning and exploration.

B. Laboratory Exercises and Design Project

As part of the Digital Fundamentals module, students work on laboratory exercises and a design project in a computer and electronics laboratory setting over nine weekly 3-hour sessions. Throughout the course, each student is provided with their own individual Basys 3 Trainer Board.

C. Laboratory Exercises

The first four laboratory sessions are structured for individual student work with a series of guided tasks followed by a few to-do tasks. In the beginning of each session, students are introduced to the key concepts through a tutorial where step-by-step guidance is provided. With that, students are tasked to complete simple design or implementation tasks(s) which require the application of the practical knowledge from the tutorial. The completion of these tasks are endorsed by the teaching staff and act as formative assessments to provide feedback to both the students and the instructor. There are two summative assignments distributed in these weeks.

The first lab session introduces students to FPGA digital design methodology in the Xilinx Vivado Integrated Design Environment (IDE) through the implementation of a combinational logic block to control some LEDs via switches. The students are introduced to the concepts of project and design creation, testbench and simulation, synthesis, constraints mapping and bitstream generation in the context of a simple design problem. In the second lab session, students are introduced to concepts of hierarchical design via module instantiations, interconnections and functional blocks through the implementation of four cascaded one-bit full adders to create a parallel four-bit adder. Aligned with the lectures on signed number systems, the formative assignment tasks students to implement a four-bit subtractor by reusing the adders built during the laboratory exercises.

In the subsequent two lab sessions, students are introduced to sequential circuits such as clocks and flip-flops. These primitive components are used as building blocks to create more complex integrated designs such as registers, counters and timers. The concepts of hierarchical design is re-emphasized through the implementation of different timers and the implementation of a pushbutton debouncing circuit. At the end of these sessions, the formative assignment tasks students with building a simple interactive user game such as a snake or 'catch-the-LED' game using the switches and pushbuttons as input drivers and the LEDs as output displays.

D. Design Project

In the subsequent five sessions, students work on the design project under a specific application-driven theme. In the first session, students are introduced to the motivation for the theme chosen for the design project. They are then introduced to the fundamental engineering principles behind such an application and the associated I/O interface peripheral boards for the implementation. With this, students are guided to form the most basic function(s) of the design project. The structured portion of the project ends at this point and over the subsequent four sessions, students are given free rein to expand on the basic functions and/or implement additional features to enhance their project. The students are highly encouraged to conduct research on implementing new features which they judge to be beneficial to the function of the project or to exercise creativity when expanding on existing features. The specific details for three application-driven projects are elaborated in section III.

III. Application Driven Design Projects

A. Related Work

FPGAs are introduced into undergraduate curriculum at varying points across different universities. However, previous works discussing design projects in digital logic education often involve the implementation of finite state machine controller projects or game-based projects. These projects typically implement specific functions and involve only the switches and pushbuttons as input drivers with the 7-segment and user LEDs as output displays [2][6][7][8]. Todorovich et. al. discusses a design project where students develop a modular printed circuit board with the basic functionality of a configurable logic block similar to a logic slice on an FPGA [3]. Tabrizi develops and implements defective or improvable IP products on FPGAs which require students to correct or improve [9] as part of their project work.

B. Project 1 : Digital Oscilloscope

In the first launch of the revised curriculum, this iteration of the module was worth five modular credits where students work independently on the design project. Students were also provided with a project archive with multiple Verilog and VHDL modules that included 1) top-module of the design where a VGA and ADC controller were already instantiated, 2) clock wizard IP files, 3) VGA interface controller, 4) ADC interface controller, 5) sample clock divider, 6) sample test bench, 7) signal generation simulator and 8) constraint file for the Basys-3 board.

The selected application or theme for the design project is the design of a Digital Oscilloscope. Prior to taking this module, all students were required to complete a foundation module of Electrical Engineering. In this module, students are introduced to fundamental DC/AC electrical circuits as well as taught to use basic measurement equipment of multi-meters, oscilloscopes and signal generators. With prior experience in using and operating such traditional bench-top oscilloscopes, students were familiar with common functions that are available on typical oscilloscopes. In the first session, students were given the chance to operate these bench-top oscilloscopes again and are also exposed to modern USB-based plug-and-play oscilloscopes. The considerations of

cost, size, form factor and basic performance metrics were also compared and discussed with the students.

After a basic review of oscilloscopes commonly seen on the market, students are introduced to the technical specifications of the project. The project required them to take in signals from a signal generator within specified frequency ranges and voltages, represent these signals digitally within the FPGA and display these signals on a 1024 x 1280 pixel resolution computer monitor display via a VGA interface.

Students are first introduced to the fundamental engineering principle of analog-to-digital conversion (ADC) and guided in setting up the Artix-7's on-chip ADC by using the predefined ADC controller module provided to them. They observe a 1Hz sinusoidal and square wave signal on the oscilloscope and the equivalent digitized forms on the LEDs. Subsequently, they are introduced to the basic idea of how VGA controllers work and guided in using the predefined VGA controller module to display a teal-background with white horizontal and vertical axes on a computer monitor screen. They were then tasked to combine the two controllers together to display a 1Hz sinusoidal signal on the screen.

At this point, the structured portion of the project ends. Students are tasked to design extensions to the project to improve their digital oscilloscope in aspects of functionality and user experience over the next four weeks. Examples of features that students went on to implement include horizontal and vertical displacement of signal trace, time and voltage division scaling, automatic scaling, triggering functions, measurement of time and voltage parameters, enhancing the VGA displaying by writing text or numbers to screen, dual channel inputs and many more.

The general feedback indicates that students highly enjoyed this project as it gave them the ability to create a practical and useful measurement device that was 'useful' in the real world. The open-ended nature of the project also provided room for implementing any feature. A student feedback on the project is as follows.

"What I liked most about the project was that it was interesting to observe how a few lines of codes, a VGA cable and a FPGA board can create an electrical instrument such as an oscilloscope. It was also interesting to note that by just adding more codes, we can implement so many more additional features such that it can almost be a fully functioning oscilloscope. This has taught me just how effective and efficient Verilog can be when applied properly."

However, there was also negative feedback on two main fronts. The first was that students felt that the initial project archive contained too many code samples and this presented a barrier to the initial phase of the project. This was further compounded by the encrypted IP-based codes for the ADC and the relatively complex VGA controller codes. The second was that synthesis times were exceedingly long when implementing VGA-related features due to the high pixel resolution of 1024 x 1280 that was adopted in accordance to the computer displays in the laboratory.

C. Project 2 : Digital Signal Generator

The second iteration of this module was similarly worth five modular credits where students work independently on the design project. However, based on the feedback of the first iteration, a conscious decision was taken to select a project that could mitigate some of the difficulties students met previously.

Thus, the selected application is the design of a Digital Signal Generator. Similarly, students had prior experience in operating traditional bench-top signal generators and were familiar with typical common functions. Students were also exposed to modern USB-based plug-and-play digital signal generators. The considerations of cost, size, form factor and basic performance metrics were also discussed with the students. The project required them to generate signals within specified frequency ranges and voltages, convert them to analog output signals and display these signals on an oscilloscope.

Students are first introduced to the fundamental engineering principle of digital-to-analog conversion. They are then tasked to generate the required clock signals for the DAC interface controller board and guided in observing equivalent analog signals on the oscilloscope. Students are tasked to design extensions to the project to improve their digital signal generators in aspects of functionality and user experience over the next four weeks.

The differences from the oscilloscope project were multifold. Firstly, in addition to the Basys-3 development board, additional dual-channel Digital-to-Analog converter (DAC) peripheral interface boards (PmodDA2) were purchased. Though a small factor, the use of an external board reduced the level of abstraction and made it easier for students to visualize the DAC process. Secondly, students were provided with only one predefined DAC interface controller module in VHDL. This module in essence performed a serial-in, parallel-out shift register function which was relatively easier for the students to understand. This reduced the barrier to entry and it was observed that students picked up and started on the project much more quickly. Thirdly, without a compulsory VGA display, the synthesis times were greatly reduced.

Examples of features that students went on to implement include other periodic waveforms such as sinusoidal, square, pulse, triangle, frequency and amplitude scaling, variable duty cycles, IP-based direct digital synthesizers (DDS), addition of VGA displays and many more.

The general feedback indicates that though students enjoyed this project for hands-on and real-world application reasons, the constraint of requiring oscilloscopes to observe the signal generator output was highly limiting as the students had difficulty accessing oscilloscopes outside of laboratory operating hours. Even though the open-ended nature of the project was retained to provide room for creative implementations, students were observed to be visibly less excited due to the fact that the output display (bench-top oscilloscope) was not within their design or control. A

student feedback is as follows.

"The whole project was very interesting and it's very practical and relevant to me. I've always been using the function generators in lab and it was really amazing to be able to program my own function generator using the Artix-7. The whole project topic was very broad in terms of implementing different and unique features. We are also able to apply what we had learnt in lectures and make full use of it."

D. Project 3 : Real-Time Sound Effects Machine

The third iteration of the module was worth four modular credits. Due to the reduction in credits, the format of the project was modified to become pair-work. The selected application or theme for the design project is the design of a Real-Time Sound Effects Machine.

To allow for ease of pair work, the project is segmented into three sub-systems. The first sub-system incorporates an additional MEMs Microphone peripheral board (PmodMIC3) to perform input audio capture. The second sub-system incorporates a DAC (PmodDA2) and low power audio amplifier (PmodAMP2) peripheral boards to perform sound generation via an output audio jack. Each student selects a sub-system to concentrate on for the duration of the project. The third and last consist of the features that are commonly developed by the students.

Different from both previous projects, students did not have prior experience in signal processing or operating sound effects generators. Students are therefore first introduced to the fundamental engineering principles of how ADC is used to digitize audio signals for storage and processing in digital systems. Digital-to-analog conversion is then introduced to explain how analog signals are generated from the digital data.

They are then individually tasked to generate the required clock signals for the peripheral board that they are using and are guided in setting up a microphone-to-speaker system by speaking into the microphone and observing the equivalent audio output via earphones. In this project, each student was similarly provided with only one predefined interface controller module that was relatively simple for the students to understand. It was observed that students started on the project quickly and many completed the microphone-to-speaker system within an hour.

Students are tasked to design extensions to the project to improve their sound effects generator in aspects of functionality and user experience over the next four weeks. Examples of features that students went on to implement include real-time delays, pitch shifters, electronic keyboard, pre-programmed melodies, loop mixers, VGA displays and many more.

The general feedback indicates that students enjoyed this project especially because it dealt with audio and sound. The open-ended nature of the project allowed them to explore many other uses of the FPGA. However, the constraint of requiring both peripheral boards to implement certain functions required both members to meet up frequently outside of class time and they would have preferred access to more peripheral boards. A student feedback is as follows.

"It was an open ended project with that challenges us to explore and learn beyond the boundaries of the classroom. There is a certain sense of satisfaction when functions that we could only imagine at first finally works and our ideas come to fruition."

IV. Results and Discussion

The university collects both quantitative and qualitative feedback for all courses and students via an online system. Providing feedback is optional and non-obligatory. The module has been very well-received by the students as indicated by both quantitative and qualitative feedback. Table I summarizes the quantitative feedback received for the overall opinion of the module (out of 5.0) across the three years where each design project is introduced for two semesters over the year. Even though the feedback consistently outperforms faculty and department averages, it can be clearly seen that the design project of signal generator implemented in 2016 was less well-received than the other two.

TABLE I
Quantitative Feedback Collected from Students

Year	2015	2016	2017
Number of Students	303	346	241
Number of Respondents	189	261	179
Number of Respondents	62.3%	75.4%	74.3%
Overall Numerical Score (out of 5.0)	4.2	3.9	4.1

The qualitative feedback received from students was also encouraging and some selected comments follow.

"The module gave the fundamental tool-set for designing digital systems. I enjoyed the Verilog side of the course the most, it showed how most of the theory taught was used and really emphasized its importance."

"The module enables me to get involved in areas I have never thought before and arouses my interests in learning EE as the project is interesting."

"The entire project was very intriguing and thought provoking. By leaving the extra features open ended, it allows us to explore features that we would not have covered in the scope of the module. This kind of experiential learning is very helpful towards the understanding of hardware description languages."

"My favorite part of the project was realizing the vast options and capabilities of this FPGA board. Over time, I slowly implemented features I probably would have never expected to be able to. Overall, it was understanding and putting to use all the Verilog concepts that gradually piqued my interest in the project, as I realized the almost endless possibilities I could implement on the board. "

From feedback received over the years, it can be seen that the design projects are well-received by the students because of the hands-on and open-ended experience it offers.

V. CONCLUSIONS

In this paper, three real-world application-driven FPGA design projects implemented on the Basys-3 board platform have been discussed. The adoption of FPGA development boards in conjunction with peripheral interface boards provides students and instructors with many possibilities for creative real-world driven applications.

Project-based learning has been successful in creating room for students to explore and providing a sense of achievement while reinforcing the concepts taught in class. In seeing theory to practice, students strengthen the conceptual links between hardware description languages and circuit hardware. By providing predefined controller modules strategically, students are able to create exciting functions by expanding on what is created. The open-ended structure of the projects also strengthens the ability of managing different levels of abstraction as students research and implement their conceptualizations by making use of reference sources. However, one of the disadvantages is the number of boards required for such large class sizes is a significant initial investment. However, these boards have high re-usability and can be adopted in other design or prototyping courses.

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