Hybrid Teaching Mode for Laboratory-based Remote Education of Computer Structure Course

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***Abstract*—We describe an Open edX-based blended course developed for a reformed Computer Structure course at Beihang University. In three iterations of this laboratory-based course, we dive into key issues that impact students' learning, and then redesign our curriculum, which integrated with virtual laboratory technique into the MOOC platform. We show how certain course design aspects affect students' learning in the hybrid teaching mode: (a) Kung Fu style competency education with online-support laboratory system prompts students to own their learning as the pace and/or the path of learning, which is dictated by mastery instead of the time/space; (b) strengthen the use of learning-aid tools empowered teachers with the skills and information to define standard for each learner in each stage; (c) automated test technology make this blended learning possible at scale and also financially sustainable; (d) using discussion forum to build the lesson about 'what to do' when learners get stuck helped in overcoming challenges.**

Keywords— Open edX; Hybrid teaching mode; Online virtual laboratory component; Blended learning; Mastery based education;

I. INTRODUCTION

Laboratory-based Computer Structure is a second-year course offered in School of Computer Science and Engineering at Beihang University. In this course, we help students to write a MIPS CPU using Verilog-HDL in order to deepen their understanding of the computer structure.

In this article, we describe our course evolvements in Summer 2013, Fall 2014 and Fall 2015. We show the problems we found in each iteration and how we improved in the next one.

MOOC (massive open online course) as a stand-alone approach has grown tremendously in the recent years. This approach offers numerous benefits, such as using various educational resources as instructional tools, allowing multiple communication methods, supporting self-directed/paced learning and etc.

MOOCs are initially built for online use. Thus, our MOOC, developed from online materials designed for blending, which reversed the direction of most current-generation MOOCs. The hybrid teaching mode is now being touted as vehicles to reform on-campus education.

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In 2012, Duke University began using MOOCs to promote innovation in teaching and learning within the campus community, with the goal of importing successful new pedagogical ideas into Duke classrooms [1]. Practices show how instructors changed their teaching approach in both MOOCs and traditional courses, including by improving classroom materials and activities, crafting better measures of student learning, and experimenting with new pedagogies to increase engagement and learning.

Dr. Masato Kajimoto from HKU's 'Making Sense of News' gave a seminar to teachers on January 14, 2016 [2] about his experience in integrating a MOOC into on-campus teaching. He incorporated ideas and examples submitted by his MOOC students into his on-campus online teaching materials, facilitating inter-cultural knowledge exchange.

Rebecca described the design of a large-scale study undertaken to examine the use of MOOCs in fourteen campus-based courses [3], and they found there were a number of potential benefits for both students and faculty members associated with use of MOOCs, including flexibility in the use of class time, enhanced critical analysis skills, and exposure to different types of teaching styles and class discussions.

S. Rayyan elaborated a mooc based on blended pedagogy [4] for a reformed introductory physics classroom at Massachusetts Institute of Technology. The teaching staff interact with small groups of students doing problems using an expert problem-solving pedagogy. This paper shown how certain course design aspects affect students' behavior, and compared the MOOC students' behavior with the on-campus students' behavior.

[5] presented some experiences carried out at Universidad Carlos III de Madrid that combined MOOC-like content in on-campus courses.

In blended online learning environment, some students encounter barriers may ask questions directly to the teacher, and some might publish the questions in the forum where they can get help from other students. [6] outlined the capability of discussion forum to collect, distribute, and archive learning content. They also pointed out future learners have very valuable learning information based on the hands-on experience of previous learners.

[7] outlined a feedback approach to evolving a multi-section, large enrollment course over five semesters. They shown a slower pace of new topics, the mix of covering the lower-level material online with higher-level and more depth covered in class, made the blending experience more rewarding for the ECE 2040 students.

In paper [8], Luis described the use of haptic devices to improve the learning process of basic physics concepts from electromagnetism and the haptic tools via simulation of magnetic forces in 3D. Their results suggested that students from the treatment group achieved better understanding than those from control group. And 95% of the students considered the use of haptic devices combined with appropriate virtual environments facilitated them to understand the nature of electrical forces.

[11] shown how to apply the problem-based learning (PBL) approach to teach elementary circuit analysis. The PBL students appeared to grasp better the details and the overall picture of the issues taught.

David proposed an online platform where the students can design and verify their circuits with an individual and automatic feedback [12]. Results shown that students using the platform were a 20 percent more likely to pass the course than students who did not use it.

[13] proposed a novel apporach in hardware and software architecture design for implementation of remote laboratories for automatic control. Their physical setup and communication principles of hardware architecture are based on two types of devices: the programmable logic controllers and industrial network routers. The suitabilith of the architecture had been proved, and the benefits with weakness were evaluated.

CS61C Spring 2016 at UC Bereley EECS [14] taught great ideas in Computer Architecture (Machine Structures). The subjects covered in this course include: C and assembly language programming, translation of high-level programs into machine language, computer organization, caches, performance measurement, parallelism, CPU design, warehouse-scale computing, and related topics. The MIPS datapath/control in sigle-cycle processor and MIPS pipelining hazards were taught. Students need to complete a 2-stage pipelined processor.

6.004 Computation Structures at MIT [15] introduced architecture of digital systems, emphasizing structural principles common to a wide range of technologies. Starting with MOS transistors, the course developed of series of building blocks - logic gates, combinational and sequential circuits, finite-state machines, computers and finally complete systems. Both hardware and software mechanisms are explored through a series of design examples. The problem sets and lab exercises are intended to give students "hands-on" experience in designing digital systems; each student need to complete a gate-level design for a RISC processor during the semester.

A key objective of our study was to learn how faculty can take advantage of existing online teaching mode to redesign our laboratory-based course and benefit the students, and whether efficiencies can be created in this process. We conducted side-by-side comparisons to evaluate outcomes of students in hybrid teaching mode with those of students in traditionally taught iterations.

Our findings shown that students in the hybrid teaching mode did better than students in the traditional course format in terms of excellent rates, pass rates and learning assessments. At the same time, we had to work through many types of implementation challenges, including how to establish the high-quality blended learning, how to do the laboratory that need hardware device's support online, how to evaluate students' ability at scale, and etc..

This research also provided resource sharing into the process of innovation within university systems. For the universities, who are willing to import our labs into their courses, could join this online virtual laboratory without order the customized hardware devices.

II. Curriculum Evolvement

In our laboratory-based Computer Structure Course, students learned MIPS architecture and assembly. We give several projects' practice to help students in building the MIPS processor using Verilog-HDL. MIPS assembly programs are used to test the correctness by running them on the students' processor. Furthermore, students are requested to build a micro-system, which includes the MIPS processor, a bridge and I/O devices. Students need to download their packages to the FPGA board, and observe the behavior to judge their correctness at the end of the final project.

The first part practices are preparing the students with the programming ability using Verilog-HDL.

The second part practices include running and debugging MIPS assembly programs, as well as writing MIPS functions. All these skills are required when students need to test their own MIPS processor that built using Verilog-HDL.

Then the third part practices composed of learning the data path and control unit of MIPS architecture. These need students to understand what each instruction will do, and how components collaborate with each other.

A. Multi-cycle processor in Fall 2013

We redesign our course in 2013, since we found students usually got stuck when they were asked to build the processor (even just supports 7 MIPS instructions) using Verilog-HDL directly. We surveyed and discussed with students, found some of them could not understand the behavior of each instruction properly, and some of them cannot set up the datapath between components correctly.

When implementing the instructions of the Instruction Set Architecture (ISA), there are two parts work:

- Datapath, this is the part of the processor that contains the hardware necessary to perform operations required by the processor.
- Control, this is the part of the processor which tells the datapath what needs to be done.

TABLE I. PROJECTS IN FALL 2013

	Project Name	Project Content	Checkpoint
P1	The basic **Verilog-HDL** practice	Master the language grammars, and could test the function/ timing of the project using testbench	week1-2
P2	MIPS assembly language exercises using Mars	Learn how to code and debug assembly programs in the MARS	week3
P3	Single Cycle CPU design using Logisim	This single cycle CPU should support the MIPS-Lite1 instructions: {addu, subu, ori, lw, sw, beq, lui}. Learn how to use sub-circuits to demonstrate the schematic, datapath and control	week4
P4	Single Cycle CPU design using Verilog-HDL	Support MIPS-Lite2 instructions: {MIPS-Lite1, addi, addiu, slt, j, jal, jr}	week5
P5	**Multi-cycle CPU** design using Verilog-HDL	Support MIPS-Lite3 instructions: {MIPS-Lite2, lb, lbu, lh, lhu, sb, sh, slti}	week6
P6	**Multi-cycle CPU** design using Verilog-HDL (advanced)	Support MIPS-C3 instructions: {MIPS-Lite3, SLL, SRL, SRA, SLLV, SRLV, SRAV, AND, OR, XOR, NOR, ORI, XORI, LUI, SLTI, SLTIU, BNE, BLEZ, BGTZ, BLTZ, BGEZ, JALR}	week7
P7	MIPS micro-system-V1 with Uart	Micro-system including MIPS-processor, UART and timer. Support MIPS-C3 instructions	week8
P8	MIPS micro-system-V2 support interrupts	Based on MIPS micro-system-V1 with Uart, support interrupts	week9-11

As shown in TABLE I. , we added Project P2 to use MARS in helping students learning the MIPS Assembly. And Project P3 using Logisim [10] to help student set up circuits from scratch.

MARS [9] is a MIPS simulator as shown in Fig. 1. Using this tool, learners can execute the assembly program in a single-step to observe all the components' change after one instruction is executed.

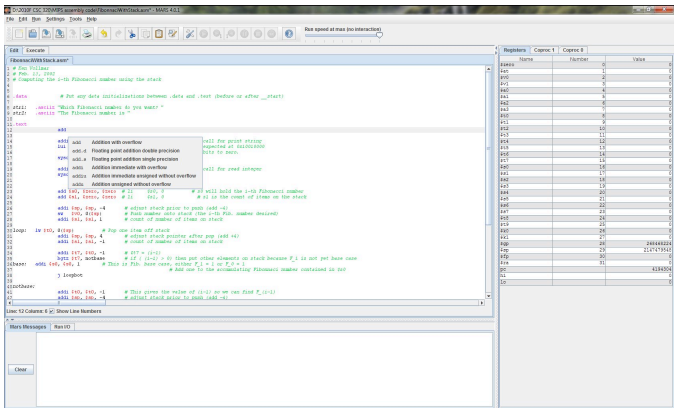

Fig. 1. MARS 4.0.1 screenshot [9]

Logisim is a graphical tool for designing and simulating logic circuits. This tool is useful for learners to build the single cycle processor from sketch. As shown in Fig. 2, when loading binary code into the instruction memory, learners could execute the code step by step to see which signals are on during the execution.

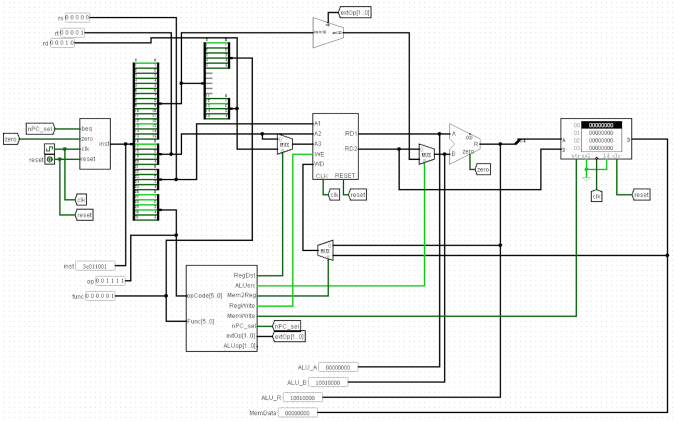

Fig. 2. Single cycle processor in Logisim

The included "combinational analysis" module in Logisim, which also helped in the teaching, allows for conversion between circuits, truth tables, and boolean expressions.

B. *Pipelined processor in Fall 2014*

We concluded lessons from Fall 2013: maybe a third of the class is sitting there and if we tested them, they could show proficiency. And maybe a third of the class, don't have enough background knowledge, or they are lacking a certain skill to make this project accessible. And the rest of the class, there was the right project at the right time.

The key point is teacher need to tell which stage the learner belonged to. So in Fall 2014, in the classroom sessions, from P3, we asked student to finish the project before the checkpoint, and we added a centralized test at the beginning of each class. We asked the students to add one extra instruction into the work they had finished.

For example, when they arrive at the checkpoint of week3, they are supposed had already finished the homework of project 3- already built the single-cycle processor support the MIPS-Lite1 instructions. They were asked to design a single cycle processor that support instructions - {MIPS-Lite1, jal} based on their homework. This could be used to test whether the learner grasp the skill they need to finish the Project 3 at this checkpoint. Since adding one instruction need they to understand the work flow and data path of this instruction, so if the learner know how to add one instruction to the basic work, they can do the whole work from zero.

After the test (like Kung Fu belt test), the learner who passed it would pace on to the next project, and who got stuck could get the face-to-face help from teacher or TA. In this iteration, students spent much more time on the project after class than last several iterations, and can have their own pace in the study.

As we shown in TABLE II. , from Project 5, design of a pipelined processor is stead of the multi-cycle processor. This work is much harder since learner need to understand all the hazards would happen in the pipelined architecture.

TABLE II. PROJECTS IN FALL 2014

	Project Name	Project Content	Checkpoint
P1	CPU component design using **Logisim**	Design 4bit/8bit/32bit Adder, GPR and ALU module	week1
P2	MIPS assembly language exercises using Mars	Learn how to code and debug assembly programs in the MARS	week2
P3	Single Cycle CPU design using Logisim	This single cycle CPU should support the MIPS-Lite1 instructions: {addu, subu, ori, lw, sw, beq, lui}. Learn how to use sub-circuits to demonstrate the schematic, datapath and control	week3
P4	Single Cycle CPU design using Verilog-HDL	Support MIPS-Lite2 instructions: {MIPS-Lite1, j, jal, jr}	week4
P5	**Pipelined processor** design with full hazard handling	Separate the hazard unit from controller module Support MIPS-Lite2 instructions	week5
P6	**Pipelined processor** design support MIPS-C3 instructions	MIPS-C3 instructions: {MIPS-Lite2, lb, lbu, lh, lhu, sb, sh, add, sub, mult, multu, div, divu, sll, srl, sra, sllv, srlv, srav, and, or, xor, nor, addi, addiu, andi, xori, slt, slti, sltiu, sltu, bne, blez, bgtz, bltz, bgez, jalr, mfhi, mflo, mthi, mtlo}	week6-7
P7	MIPS micro-system-V1 support exceptions and interrupts	Micro-system including MIPS-processor, bridge and timer. Support MIPS-C4 instructions: {MIPS-C3, ERET, MFC0, MTC0}	week8
P8	MIPS micro-system-V2 support exceptions and interrupts	Micro-system including micro-system-V1, 8bit-LED segment, 32bit-toggle switch and RS232-communicate-system. Support MIPS-C4 instructions: {MIPS-C3, ERET, MFC0, MTC0}	week9-11

C. *Pipelined processor in Fall 2015*

After the practice of Fall 2014, we found that students who always stuck on the work, usually have the following problems:

- Problem 1, they could not use the learning-aid tools properly.
- Problem 2, they did not do the complete self-test after finishing the homework.
- Problem 3, someone stuck on the programming with Verilog-HDL.
- Problem 4, the hardware device for the final project became the compete resource. And just use the device in class could not help them in the final succeed.

In the Fall 2015 iteration, we set up our MOOC course based on open edX platform to assist students' learning.

The basic skill is to reading the MIPS instruction set in order to understand each instruction behavior. Then understand the five-stage of the datapath, such as instruction fetch, instruction decode, execute, memory operation and write back. Learners should also be aware of the datapath control signals for each instruction.

MARS 4.5 (released on Aug. 2014) has a new feature called MIPS X-RAY as shown in Fig. 3. Learners could connect the X-RAY to the instructions and assemble the file. Then step through the code, that will visualize the datapath while learners are running the instruction.

The improvements in Fall 2015 are shown below:

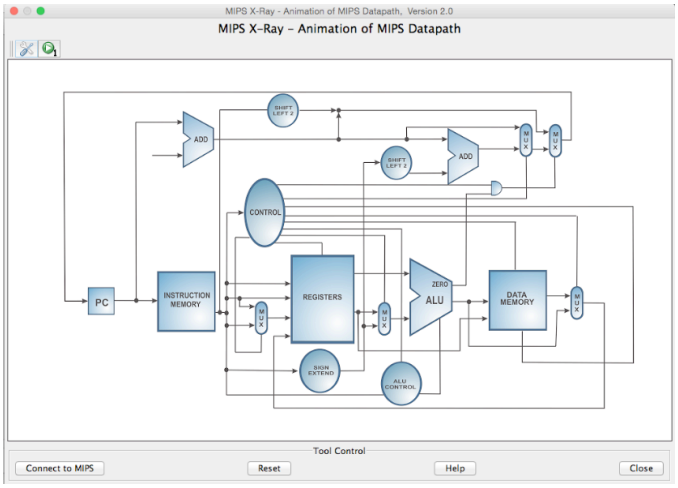

Fig. 3. MIPS X-RAY in MARS 4.5

- Videos were recorded to introduce the learning-aid tools, such as MARS, Logisim and ISE. These videos with etext were used to show how to use them effectively.
- We added week0 for Project P0, in this checkpoint we tested the students' skill of Verilog-HDL programming, together with the ability of writing the testbench. At the checkpoint of week1, we test learners' design of CPU components - 4bit/8bit/32bit adder module, GPR module and ALU module in Verilog-HDL. We using 2 weeks to check P5 and just 1 week to check P6. Since when they succeed in building 10 instructions pipelined processor, it is just need some more time to adding more instructions into the basic one.
- We developed an online test platform connected to the open edX platform. When learners finished their homework, they could upload their program in Verilog-HDL onto the test platform. Then they will get the error feed back.
- We built an online virtual laboratory system, this helped sharing the hardware resources, and also helped in the mastery-based learning.

III. LAB BASED ONLINE COURSE COMPONENTS

Our laboratory-based online consists of web pages with instructional content, videos, quizzes, online homework with automatic testing, online labs and discussion forum.

A. *Videos of Learning-aid Tools' Operation*

As we introduced in section II, learning-aid tools like MARS and Logisim, could help the learners in the understanding of ISA with the datapath and control unit of processor. These videos included the basic introduction and how to use these tools to facilitate in the later projects.

B. *Quizzes*

We set centralized quizzes from week0 to week2, the start time for these quizzes are set the same as the classroom

session's starting time. We used them to test the learners' ability of using Verilog-HDL in programming. On the other hand, these quizzes helped the learners in reviewing the knowledge points.

Quizzes included basic number representations, generally grammar questions, correspondence between waveforms with code, binary decoding, and MIPS assembly code reading.

C. *Online homework with automatic testing*

Homework projects of varying difficulty are found at the end of each week. We developed an online automatic testing system for the program written in Verilog-HDL.

When the design (uploaded by the learner) need to write into GPR or Memory, the testing system output the GPR number/ Memory address and the content using $display system task. All the output information will be compared with the standard program.

This online automatic testing system could help learners to find the errors in their design. And this system also used in the on-campus testing, which had reduced the teachers' burden on the evaluation.

D. *Online labs*

As we mentioned in section II, students need to download their packages to the FPGA board, and observe the behavior to judge their correctness in the final project.

The online lab system as shown in Fig. 4, which is composed of the hardware system and the software system. The hardware system included the master FPGA, slave FPGA and host computer.

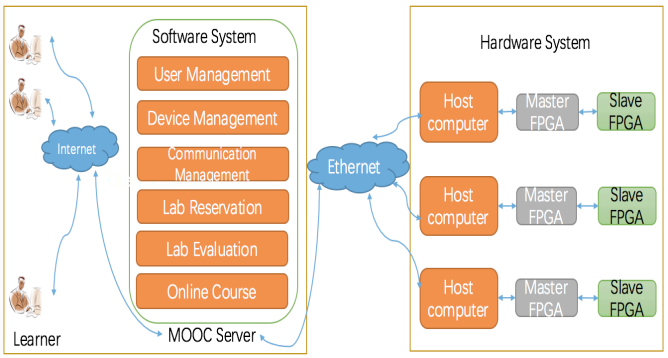

Fig. 4. Online lab system

These FPGA board which customized in our online laboratory course is shown in Fig. 5. The SYS AREA shown in the board is the master FPGA, and USER AREA is the slave FPGA.

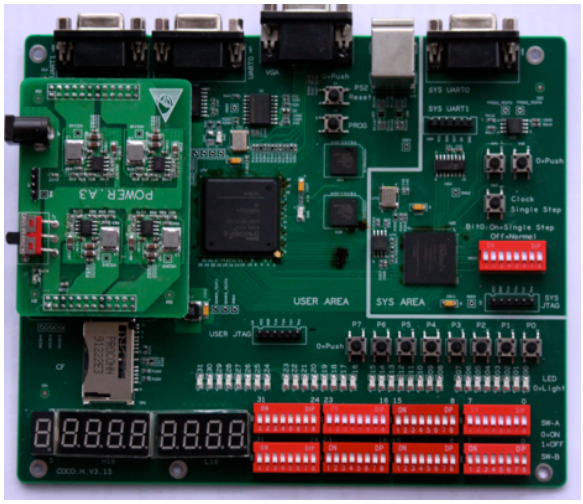

Fig. 5. FPGA Board used in the online lab

Learners need to make a reservation when they want to use the device hardware, and MOOC server would feed back the scheduled lab time.

When doing the lab, students need to download the .bit file to the remote host computer, which will transport it to the master FPGA. The master FPGA will decode the download command, then store the .bit file in RAM, and transport the file to slave FPGA.

When the slave FPGA finish the loading of target file, master FPGA will monitor the status of output device in slave FPGA, and record the change status of registers, which will also be fedback to host computer. Then host computer will transport the output information to client. This allow students to complete the laboratory activities, such as running the programm, observing the output on remote device and debugging.

When debugging online, students operates on the input client software, this client will transfer the operations to the remote host computer in order to generate the driving command to the master FPGA. After decoding, the system will simulate the electrical signal into slave FPGA.

E. *Discussions*

Participants could post questions, answers or comments in the discussion forum. Here participants included the teachers, TAs, and learners. All of them discuss problems and concepts with each other and to alert course staff about issues with the material.

We encouraged our students to post the problems that they encountered, and all the students are stimulated to answer the questions. Another important thing was, we welcome the post about how to get unstuck. All these posts formed like a checklist, which helped learner move at their own pace.

IV. Evaluation and Conclusion

We evaluated our hybrid teaching mode with the traditional course format in terms of excellent rates, pass rates and learning assessments.

In this section, we conclude how to establish the high-quality blended learning, how to evaluate students' ability at scale, and how the discussion forum become positive in the teaching and learning.

A. Education Learn from Kung Fu

As we described in section II. B, we found it was important for students to move on and receive credit only after they've mastered a core concept. In our course, we design this Kung Fu style project-based competency education.

The course was organized by 8 projects (from easiest to hardest), before learners start to do the next project, they need pass the test of current one. Students in which project shows their level, they start with Project X and as they master new content and skills they are awarded to Project X+1. Learner must demonstrate mastery of several different elements, what students are expected to know and be able to do.

For instance, at the checkpoint week 4, learners first finish their single cycle CPU design, which need support MIPS-Lite2 instructions. If they succeed, one instruction that does not include in MIPS-Lite 2, will be asked to add into their basic design. Again, this new design should pass through the test. Then there is a face-to-face discussion with teacher or TA. In this stage, several questions related the project are discussed between the learner and teacher. Once the instructor is satisfied that the learner has mastered all elements of this project level, then he/she could move forward to the next project.

We define our grades according to the completion degree of project. If learners could pass the requirements of Project 5, they would get Grade 'D' at least. In 2013, project 5 is to build a multi-cycle processor while in 2014 is to build a pipelined processor. Here, our course in 2014 is much harder than that in 2013. Instructor grades the student as 'C' for passing through project 6, 'B' for project 7, and 'A' for project 8. Parts student who passed project 8 would be awarded as 'excellent'.

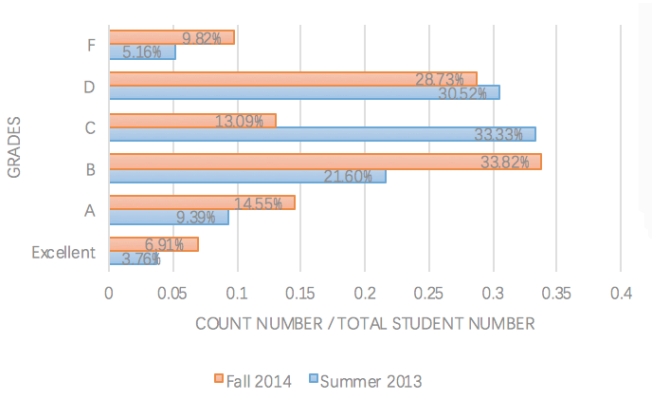

Fig. 6. Grades distribution compared between Fall 2014 and Summer 2013

As we shown in Fig. 6, we can tell that even the course is much harder in Fall 2014, our students had a better performance in the course. The amount of learner who are awarded of 'excellent' in Fall 2014 is nearly 2 times the number in Summer 2013. 14.55% of the learners got Grade A in 2014 compared just 9.39% in 2013. Learners awarded with Grade B from 46/213 in Summer 2013 to 93/275 in Fall 2014.

B. Learning-aid tools with automatic testing system

When impelling our mastery-based education, we defined standards in each project. These empowered learners to see the path ahead. On the other hand, assessment process is separate from the learning process, and we found the assessment session is an opportunity to reinforce learning.

We have introduced the learning-aid tools in section II.A, learners could compare their own design with the MIPS simulator MARS. When both work are stepped in by one instruction, the output and status transitions in learners' design should be same as what happened in the MARS. This learning-aid tool helped a lot in self-assessment.

In Summer 2013 we had 213 learners, Fall 2014 the number increased to 275, and in Fall 2015 we had 264 learners. We only have 4 hours on-campus classroom time to assess whether the learner could move advance, although we have 4 teachers with 4 TAs. We found we still need an efficient mechanism to assess every student's ability in each checkpoint. And our students also need to assess themselves properly before attending the checkpoint.

We integrated an automatic testing system into the open edX platform in 2015. Student upload their design to the automatic testing system, it will feedback whether they pass through with the error report. Using this testing system, teachers have keen awareness of each student's current stage of learning. This testing system also helped in their self-test at home, resulting in better performance.

As shown in Fig. 7, the number of learners who arwarded with 'excellent', 'A' and 'B' in Fall 2015 is higher compared to Fall 2014. We also compared the pass rate of P6 and P7 at the first checkpoint in these two years. In Fall 2015, students' homework perfromance is better due to the error finding under the help of automatic testing system. So the pass rate is higher in the complex project P6 and P7 at the first checkpoint as shown in Fig. 8.

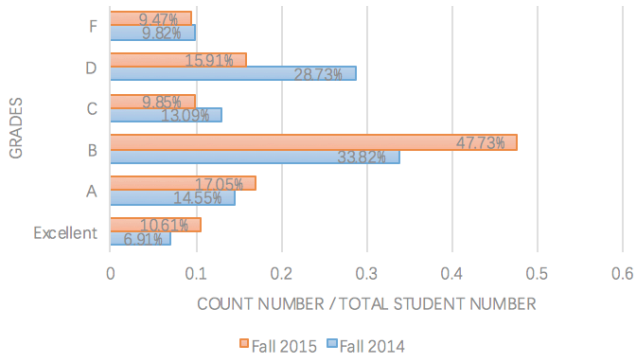

Fig. 7. Grades distribution compared between Fall 2015 and Fall 2014

Fig. 8. Pass rate of P6 and P7 at the first checkpoint

Furthermore, the automated test technology made our blended learning possible at scale and also financially sustainable.

C. *Positive asynchronous online discussion forum*

Since activities are parallel across projects (all have promgramming, ISA understanding, datapath and control unit building, and etc.), there are many opportunities for students to help each other.

As we metioned in section III.E, we encouraged students to post unclear issues when they read project instructions and the problems they encountered when doing the design. Since advanced students do common activities first, the less advanced could first to check trouble-solution list, this helped them in the study.

Teachers monitored the discussion forum in order to improve the instructions or online resources according to the feedbacks from learners. We show the post number of Fall 2015 in Fig. 9.

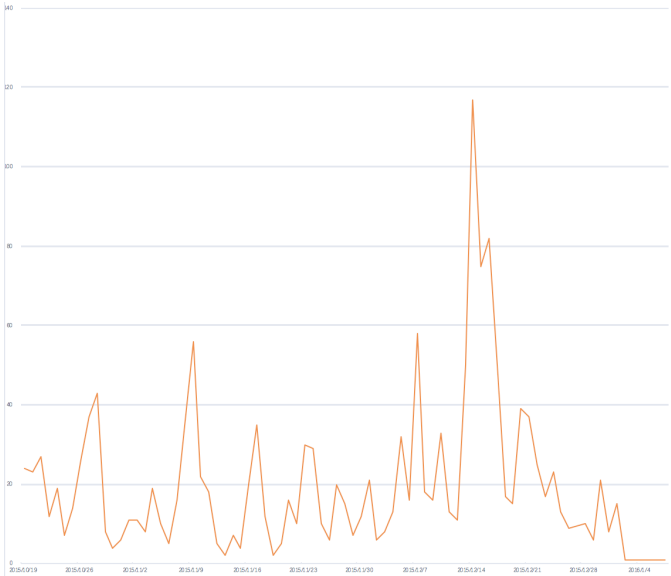

Fig. 9. Number of forum posts in the Fall 2015

From the statistics, we found the post hotspots happened at the design week of P8, P4, P2, and P5. We dive into the posts in these projects, and found following issues:

Learners need design MIPS assembly program in P2, posts in this week discussed: the understanding of MIPS instructions, how to use the tool MARS, and how to program/debug with it. Then we added resources such like tool operation video on these facets. From our survey, the less advanced learners said these new resources did important promotion in their design.

P4 is the first time they use Verilog-HDL to design the processor, through the feedback from forum, we added quizzes to ensure learners have the basic programming skill using Verilog-HDL; we also added this skill assessment during the face-to-face class.

Most discussion of P5 is about how to separate the hazard unit from the controller module, this pushed teachers added more explanations in the classroom. And we found the learners whose goal is to finish P8 already formed a positive asynchronous forum.

D. *Summary*

In this paper, we introduced our hybrid teaching mode for lab-based computer structure course. We show the lessons learned from Summer 2013, Fall 2014 to Fall 2015, and the solutions we designed to form a high-qulity blended learning course.

We integrated the virtual laboratory technique into the MOOC platform, and used learning-aid tools with automatic testing system. All these course designs empowered the learners with the skills, information, and tools that they need to manage their own learning.

We also show online experience is actually informing what's happening in the classroom. The data from each part, whether it's teacher observations or actual outcomes, informed the other side. And these two parts become an integrated whole.

We re-conceptualized the role of the teacher for the blended learning. We shifted from the lecturer to the facilitator. Since we not just explain the concepts, but intend to intervene the students' learning at the right time for their needs. We tried to teaching skills using learning-aid tool instead of just teaching content.

The comparsion in terms of excellent rates, pass rates and learning assessments, had shown the blending learning experience had more rewarding for students.

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REFERENCES

[1] Kim Manturuk and Quentin M. Ruiz-Esparza, "On-Campus Impacts of MOOCs at Duke University", retrieved from http://er.educause.edu/articles/2015/8/on-campus-impacts-of-moocs-at-duke-university

[2] "The Results of Integrating a MOOC Into On-Campus Teaching", retrieved from https://www.class-central.com/report/integrating-a-mooc-into-on-campus-teaching/

[3] Rebecca Griffiths, Christine Mulhern and Richard Spies, "Adopting MOOCs on Campus: A Collaborative Effort to Test MOOCs on Campuses of the University System of Maryland", Online Learning Journal, Vol19, No 2 (2015).

[4] S. Rayyan, C.Fredericks, K.F. Colvin, and et al. , "A MOOC based on blended pedagogy",Journal of Computer Assisted Learning, doi: 10.1111/jcal.12126

[5] Carlos, Hoyos, and et al., "Mixing and blending MOOC Technologies with face-to-face pedagogies", 2015 IEEE Global Engineering Education Conference (EDUCON), pp. 967-971, March 2015.

[6] D. Helic, H. Maurer, and N. Scerbakov, "Discussion Forums as Learning Resources in Web-Based Education," Advanced Technol- ogy for Learning, vol. 1, no. 1, pp. 8-15, 2004.

[7] Bonnie Ferri, Joyelle ,Mary Ann Weitnauer and David Majerich. "A Feedback-Based Approach for Evolving a Blended Class Model for Large Enrollment", 2015 IEEE Frontiers in Education Conference, pp. 285-292, Otc., 2015.

[8] Luis Neri, David. E, and Julieta N., "Improving the Learning of Physics Concepts by Using Haptic Devices", 2015 IEEE Frontiers in Education Conference, pp.293- 299, Otc., 2015.

[9] MARS screnshot 4.0.1, retrieved from http://courses.missouristate.edu/KenVollmar/mars/screenshot_4_0_1.jpg

[10] Logisim a graphical tool for designing and simulating logic circuits, retrieved from http://www.cburch.com/logisim/

[11] Luis R., Mikko Honkala, and Anu Lehtovuori. "Applying the Problem-Based Learning Approach to Teach Elementary Circuit Analysis", IEEE Transaction on Education, Vol. 50, No. 1, Feb, 2007.

[12] David Baneres, Robert Clariso, Josep Jorba, and Montse Serra. "Experiences in Digital Circuit Design Courses: A Self-Study Platform for Learning Support", IEEE Transaction on Education, Vol. 7, No. 4, Oct. – Dec., 2014.

[13] Martin Kaluz, Javier Garcia Miroslav Fikar, and Lubos Cirka. "A Flexible and Configurable Architecture for Automatic Control Remote Laboratories", IEEE Transaction on Education, Vol. 8, No. 3, July – Sept., 2015.

[14] Great ideas in Computer Architecture (Machine Structures), UC Berkeley EECS, CS62C Spring 2016, retrieved from http://inst.eecs.berkeley.edu/~cs61c/sp16/ .

[15] 6.004 Computation Structures, Spring 2016 at MIT, retrieved from https://6004.csail.mit.edu