Using the Basys-3 Trainer to Support VHDL in Digital Logic Fundamentals Course

Jennifer L. Bonniwell and Susan C. Schneider
Department of Electrical and Computer Engineering
Marquette University
Milwaukee, WI, USA
jennifer.bonniwell@mu.edu and susan.schneider@mu.edu

***Abstract*—The "bring your own experiment" movement is being incorporated in universities all over the world. This movement is centered on students purchasing low cost hardware for use in their courses. This paper discusses the inclusion of the Basys-3 FPGA Trainer available through Digilent in a lecture only, sophomore year, Digital Logic Fundamentals course. The enhancements to this course also include the introduction of a hardware description language, VHDL, which is becoming an integral part of the Electrical and Computer Engineering curricula. This paper describes the redesign of the course in Spring 2016 as well as the studies to be completed at the end of the semester.**

Keywords—BYOE; VHDL; FPGA; Digital Logic

I. Introduction

In the "Bring Your Own Experiment (BYOE)" movement, which advocates the use of low-cost hardware for students to investigate topics and concepts on their own, it is anticipated that the use of BYOEs can increase student knowledge retention [1]-[4]. Historically at Marquette University, the hands-on component of the Digital Logic Fundamentals Course involved discrete logic gates or programmable logic devices, breadboards, and a lot of wires. These discrete gate projects are being replaced with a BYOE hands-on experience that uses Very High Speed Integrated Circuit Hardware Description Language (VHDL) to program Artix-7 Field Programmable Gate Arrays (FPGAs) on the Digilent Basys-3 Trainer [5]. This evolution is supported by the 2016 draft guidelines for computer engineering curriculum which has explicitly added instruction in hardware description languages at the introductory level into the digital design knowledge area [6] for the first time. Other studies have been performed in this area such as the study in [7], which considers incorporating FPGA development boards in multiple courses in their curriculum. Their initial results encourage them to continue their study to determine the best way to obtain good learning results while minimizing equipment cost.

In Spring 2016, the use of VHDL to program FPGAs is incorporated into nearly every topic covered in the Digital Logic Fundamentals Course, covering both combinational and sequential designs. Accompanying the chapters that include the use of VHDL, the students are presented with a slide show tutorial on a topic in the chapter and then asked to produce a similar implementation of another digital circuit. As the course moves on, the complexity of the projects increases and the students are expected to work more independently, with less support from the slide shows. In addition to using the Basys-3 Trainer in the Digital Logic Fundamentals Course, it is being incorporated into two other courses, Digital Electronics Laboratory and Computer Hardware. This gives the students a lot of experience mastering different aspects and uses of VHDL to accomplish digital system design.

The following studies are to be conducted via surveys at the end of the course as the metrics to determine modifications of the next offering of this course in Spring 2017: (1) the students' perception of the ease of use of the VHDL trainer compared to their experiences working with wiring circuits with discrete gates; (2) the students' opinions of the BYOE experience and their engagement with course materials due to immediate access of the hardware; (3) the instructor's opinion on the range of projects that can be accomplished with the trainer compared to the historical hands-on activities with discrete gates and (4) the instructor's perception of ability of the Basys-3 Trainer in assisting the students to achieve the learning outcomes for the course.

The paper is organized as follows: section II describes the history of the Digital Logic Fundamentals course at Marquette University; section III provides the details of the hardware used by each student in the course; section IV describes the various hands-on activities and projects assigned to the students; section V provides preliminary qualitative assessment on the effectiveness of the course modifications; and section VI concludes the paper and discusses the plan for future work.

II. Digital Logic Fundamentals Course

The Digital Logic Fundamentals course at Marquette University has transitioned from traditional lecture, to self-paced learning. Since the 2010-2011 academic year, this course has been taught using an instructor-paced learning model which is essentially self-paced learning with a rigorous schedule set up by the instructor. This model has many of the attributes of a flipped classroom environment where students carry out readings and homework in preparation for the in-class experience. Throughout these transitions, two aspects of the digital electronics courses have remained constant, (1) the content reflects the "usual" progression of topics from combinational logic design through sequential circuit design covered in most of the popular "Fundamentals of Digital

Electronics" textbooks such as [8]-[10] and (2) students do several hardware experiences in which the students design, build, test and demonstrate working digital electronics circuits. There were four hardware experiences, two each in combinational logic circuit design and sequential logic circuit design. The first of the two hardware exercises in the combinational or sequential category involved design and build of a smallish scale design with discrete components while the second hardware experience was a larger system design with multiple inputs and multiple outputs done with programmable array logic (PAL). Specifically, students (a) implemented several Boolean functions using AND/OR/NOT gates and NAND gates; (b) created a binary coded decimal (BCD) to seven-segment decoder; (c) built a four-bit counter using JK flip-flops and compared it to the same counter designed with D flip-flops and (d) a final design project which implemented an algorithmic state machine (ASM) for systems such as an elevator controller. These hardware experiences were done as part of the Sophomore Circuits Laboratory. Students purchase a component kit for the class which contains a selection of AND, OR, NOT, NAND, NOR gates, as well as two General Array Logic devices, a 16V8 and 24V10. Switches, resistor arrays and light emitting diodes (LEDs) are also included in the kit so the students can build 4-bit digital input and output networks. Students use experimenter's breadboards from a previous laboratory class on which to build their digital circuits and they have access to standard laboratory test and measurement equipment including DC power supplies, function generators (for clocks), logic probes, and oscilloscopes. In addition, the hardware needed to program the PAL chips is also available to the students in the laboratory.

Because of the march of technology, in Fall 2014, the department's Undergraduate Committee recommended that the content of Digital Logic Fundamentals course be "refreshed" as soon as possible to more fully incorporate modern digital circuit implementation technologies, specifically the use of VHDL. This foresight has been subsequently validated by the update to the guidelines for computer engineering curriculum [6]. In Spring 2016, a redesign of the course was implemented. This redesign continues to use the instructor-scheduled learning format while also introducing VHDL and the use of an FPGA trainer, the Basys-3, in the BYOE format. The FPGA/VHDL experiments are included in the Digital Electronics course proper, while students continue to do the discrete gate hardware experiences (a and c above) in the Sophomore Circuits Laboratory.

III. Hardware

The FPGA trainer used in Digital Logic Fundamentals is the Basys-3 provided by Digilent, [5]. This printed circuit board (PCB) is designed to be exclusively used with the Vivado® Design Suite and contains:

- the Xilinx Artix-7™ FPGA
- serial FLASH
- USB-UART bridge
- four 12-pin Pmod™ connectors
- 12-bit VGA output
- Digilent USB-JTAG port for FPGA programming and communication
- 16 switches
- 16 LEDs
- 5 push buttons
- a quad seven-segment display

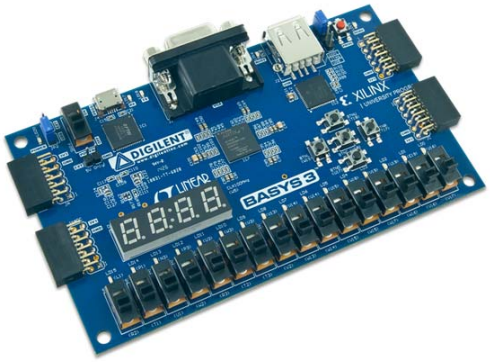

Fig. 1 Basys-3 PCB [1]

This FPGA trainer was chosen as it (1) requires no additional hardware to operate, (2) is relatively inexpensive – and could, in the future, be added to the list of required materials for the course, and (3) provides adequate peripherals for use in advanced digital logic courses. For Spring 2016, eighty kits, consisting of the Basys-3 trainer and the USB cable with a project box, were purchased. Each student is issued their own kit, to be returned at the end of the semester.

IV. Course Projects

The redesign of the Digital Logic Fundamentals course offers a great opportunity to incorporate the need of industry into the electrical and computer engineering curricula at Marquette University. This section describes the various hands-on activities and projects assigned to the students throughout the Spring 2016 offering of this course.

The first hands-on activity assigned to the students is to control an LED by a switch, which is the "Hello LED" tutorial. One of the objectives of this activity is to familiarize the students with the Vivado® Design Suite software by generating and modifying code, writing a testbench (code specifically for behavioral testing of their design), running simulations, and generating a programming file. Another objective from this simple activity is to highlight various best practices early on in their experience with VHDL. A slide show is provided to the students that explains the project's goals and objects, and describes the various components of an FPGA project. The slide show concludes with a demo video of the project in action.

The next two activities are relatively similar; they both incorporate the design of multiple-input functions. The accompanying slide shows to these activities provide demonstration of similar circuits, but the level of detail in each step has been reduced in comparison to the "Hello LED" tutorial. This main objective in these activities is to provide straight forward designs, giving students the chance to focus on practicing their interactions with VHDL and the Vivado® software. In the latter of the two activities, the students are also asked to interface with the seven-segment display on the Basys-3 PCB to display the output of their function, a zero or a one.

Now that the students are familiar with using switches as inputs and utilizing various outputs available on the PCB, they are tasked with designing a four-bit subtractor circuit. To give the students an example of a design with similar complexity, the slide show explains the design of a four-bit ripple-carry adder. This activity emphasizes multiple instantiations of a single component and using signals to interconnect these multiple instantiations.

Prior to the next hands-on activity, the students learn about encoders in their lesson material. Their hands-on activity is to design a BCD to seven-segment display encoder using switches for inputs. The quad seven-segment display unit on the Basys-3 PCB is designed with a common cathode. To control each of the four displays separately, the students would have to add sequential circuitry to their design that they have not been introduced to yet, so it is acceptable for all four displays to show the same value.

With all of this experience creating various circuits for functions and some arithmetic circuits as well, the students are assigned a design project for an arithmetic logic unit (ALU). The maximum grade possible for each student is dependent on the number of operations implemented in their ALU. For maximum credit, students were asked to implement: clear; adder; subtractor; logical OR; logical AND; logical XOR; and preset. There is no slide show to accompany this project, which incorporates various combinational design techniques, since the students are to use their knowledge gained up to this point to complete their designs.

Following the project is the introduction to sequential circuits. The first activity for sequential design to use the datasheets for the 74LS74A D flip-flop and the 74LS109A JK flip-flop to obtain the necessary design requirements to implement these two flip-flops on the Basys-3. After gaining experience implementing flip-flops in VHDL, the students design a BCD counter, with the option to output to the LEDs or to the seven-segment display. The objectives for these two activities are to give students experience reading and interpreting datasheets as well as using multiple concepts together in the BCD counter design.

The final project is a state machine design. The students are given five designs that they can choose from to implement on their Basys-3. This project combines all of the concepts covered in the course and prepares students for future courses that incorporate VHDL.

V. Project Evaluation

Since the course has not come to an end, the surveys for assessment have not been given to the students yet. However, some qualitative assessments from the instructors are provided based on informal discussions with students. A few of the outcomes from these discussions are provided in the following.

"A student stated that he spent an entire day (8 hours) learning how to multiplex the quad seven-segment display on the Basys-3 trainer so that he could individually control each seven-segment rather than all four displaying the same value. He said he now knows more about clocks in VHDL than he ever thought possible. This action on his part WELL preceded your presentation on the seven-segment display, let alone we had not even discussed clocking at this point. I was impressed because he also followed up his comments with the words "it was fun". About one third of the students continue to play with these hardware kits when they get the chance. This is what we want!"

"When working with various students during my office hours, I believe that the joy that crosses over a student's face when they observe their design functioning properly on the Basys-3 Trainer provides a spark for these students to be intrinsically motivated to continue to tinker with the boards for designs of their own."

The culminating combinational design project requires the students to build an ALU. As mentioned, the other hardware experiences prior to this design project emphasized multiple instantiations of a single component. There were no specific requirements in this design project to create the multi-bit adder and subtractor using this multiple instantiation technique. This gave the students the ability to choose how to implement these operations. The teaching assistants and the instructor have noted that it appears that at least 50% of the students did significant additional research and used the IEEE arithmetic library to create their ALU even though no mention of this possibility had been given in the previous hardware experiences. And – best of all – almost all of the students are successfully completing the A-level ALU design.

VI. Conclusions and Future Work

The first implementation of VHDL and an FPGA trainer as a BYOE in Marquette University's Digital Logic Fundamentals course has been successful up to this point in the semester. Various students have voiced their opinions that it is "so exciting" to see their projects come to life on the PCB.

As the semester comes to an end, two surveys on VHDL and the Basys-3 will be provided, one to the students and one to the instructors, who are also the co-authors on this paper. The surveys will contain questions relating to the following studies: (1) the students' perception of the ease of use of the VHDL trainer compared to their experiences working with wiring circuits with discrete gates; (2) the students' opinions of the BYOE experience and their engagement with course materials due to immediate access of the hardware; (3) the instructor's opinion on the range of projects that can be accomplished with the trainer compared to the historical hands-on activities with discrete gates and (4) the instructor's

perception of ability of the Basys-3 Trainer in assisting the students to achieve the learning outcomes for the course.

Additional work will be completed this summer to incorporate the use of the Basys-3 Trainer into the Digital Electronics course. The goal will be to develop multiple projects that will interface an external sensor to the FPGA on the Basys-3 Trainer.

REFERENCES

[1] Yi Zhu, Thomas Weng, and Chung-Kuan Cheng, "Enhancing learning effectiveness in digital design courses through the use of programmable logic boards," IEEE Trans. Educ., vol. 52, no. 1, Feb. 2009.

[2] Kimberly E. Newman, James O. Hamblen, and Tyson S. Hall, "An introductory digital design course using a low-cost autonomous robot," IEEE Trans. Educ., vol. 45, no. 3, pp. 289-296, Aug. 2002.

[3] Ney Laert Vilar Calazans and Fernando Gehm Moraes, "Integrating the teaching of computer organization and architecture with digital hardware desgin early in undergraduate courses," IEEE Trans. Educ., vol. 44, no. 2, pp. 109-119, May 2001.

[4] Shawki Areibi, "A first course in digital design using VHDL and programmable logic," Proceedings of the 31st ASEE/IEEE Frontiers in Educ. Conf., pp. T1C-19-23, Oct. 2001.

[5] Digilent Inc., Basys 3 Development kit, http://www.digilentinc.com/Products/Detail.cfm?NavPath=2,400,1288&Prod=Basys3. Last accessed 10/29/2015.

[6] Association for Computer Machinery and the IEEE Computer Society, Interim Curriculum Report - Computer Engineering Curricula 2016, Version 2015 October 25, from https://faculty-web.msoe.edu/durant/ce2016/2015-10-25-FullReport-RandC.pdf.

[7] C. G. Haba, "Using FPGA development boards for multi-course laboratory support," Proceedings of the Global Engineering Education Conference, April 2014, pp. 794-797.

[8] S. Brown and Z. Vranesic, *Fundamentsl of Digital Logic with VHDL Design, 3rd. ed.*, McGraw-Hill Higher Education, Boston MA, 2009.

[9] C.H. Roth, Jr., and L.L Kinney, *Fundamentals of Logic Design, 6th ed.,* Cengage Learning, Stamford CT, 2010.