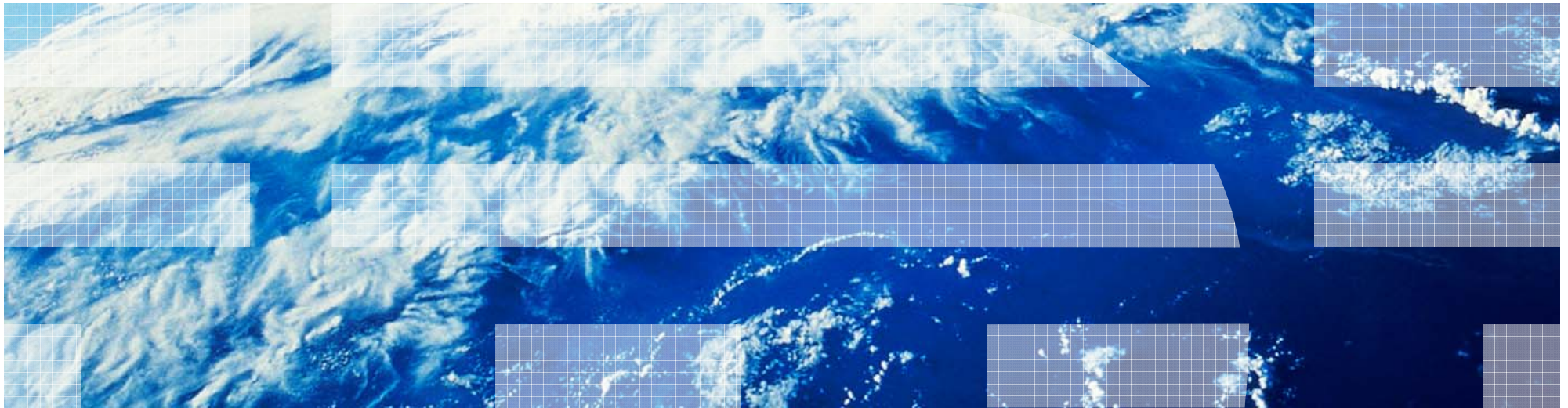
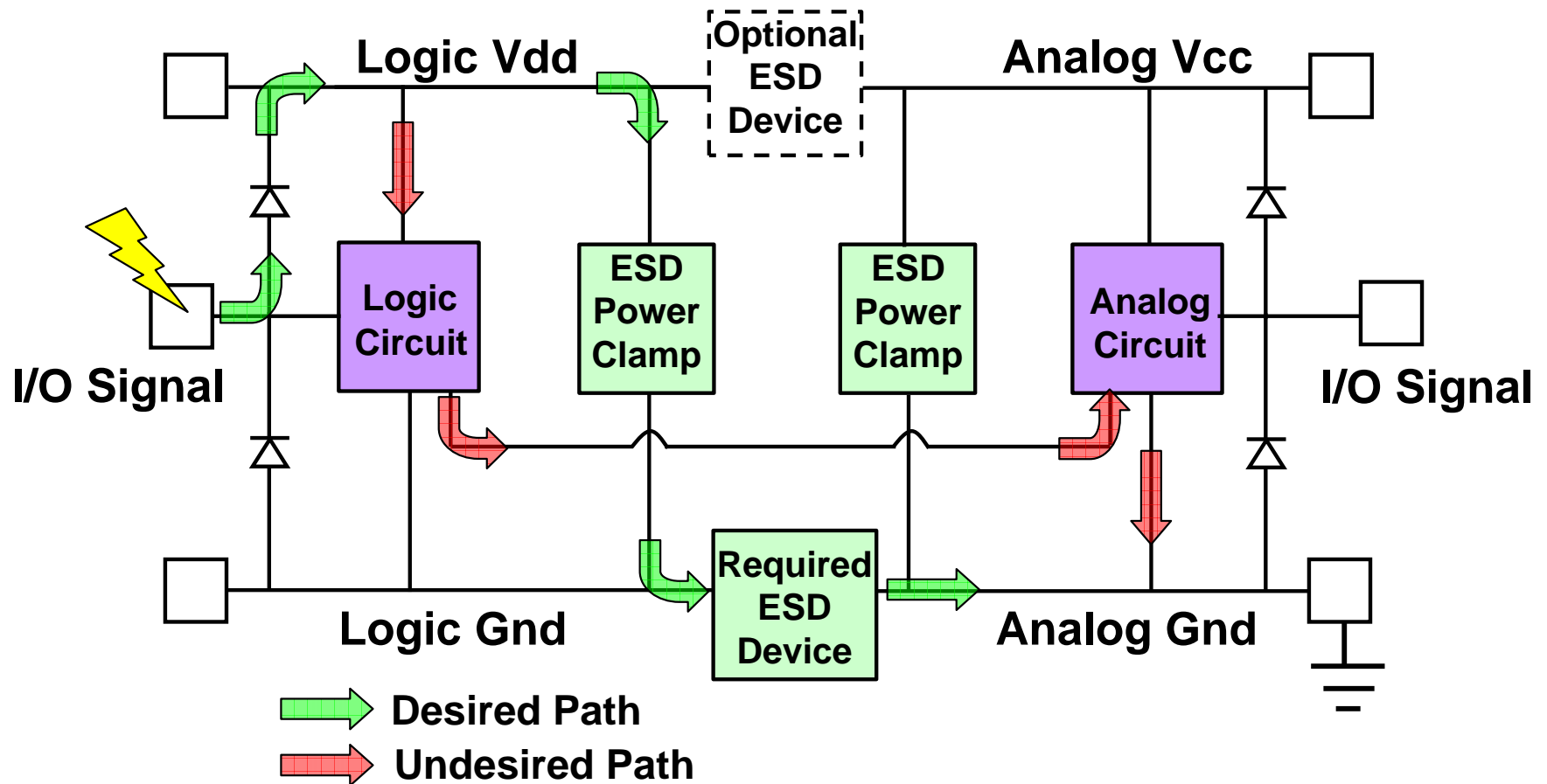


A Comprehensive ESD Protection Design Flow Utilizing Suite of ESD Verification Tools in Advanced Technologies

M. Muhammad, R. Gauthier, J. Li, A. Ginawi, J. Montstream, S. Mitra, A. Joshi, K. Henderson, N. Palmer, B. Hulse

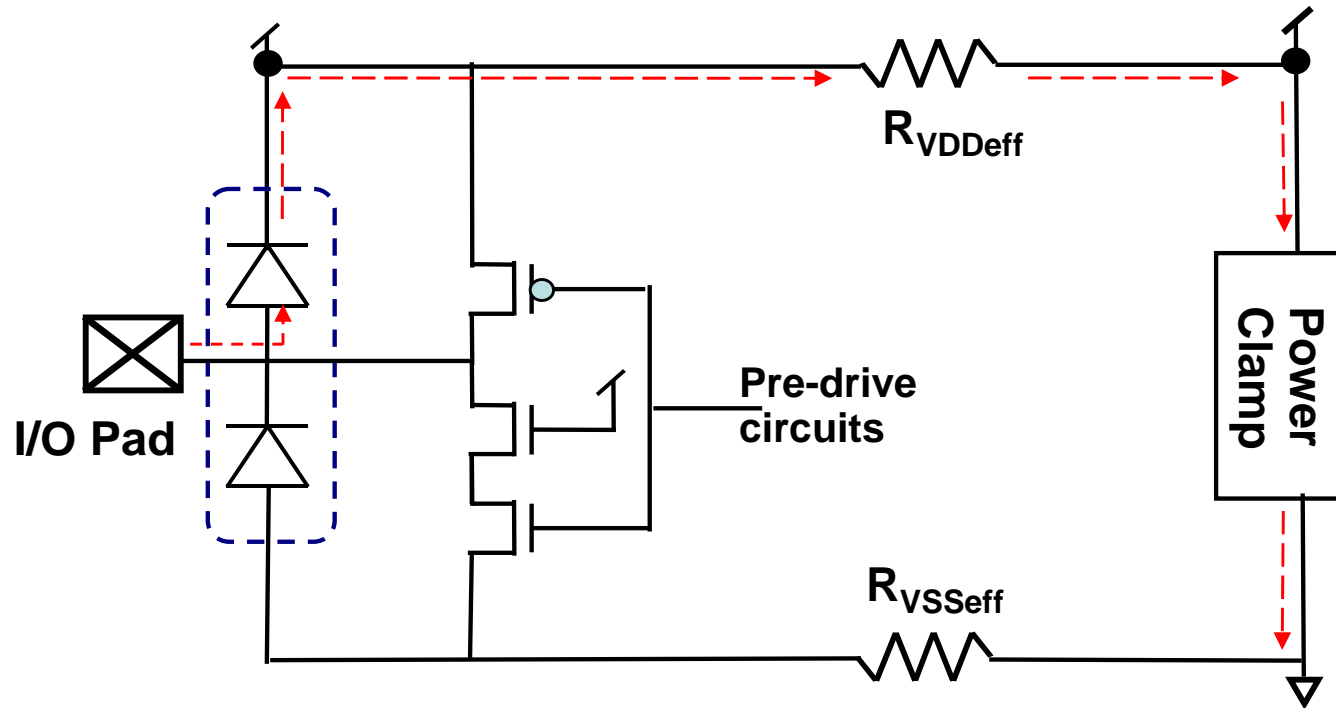


Full chip ESD Protection requirements



- Robust current handling, low resistance path for conduction of ESD current between any two pads
- Ensure that during an ESD event, the voltage drops across any internal device should not lead to the failure of the device

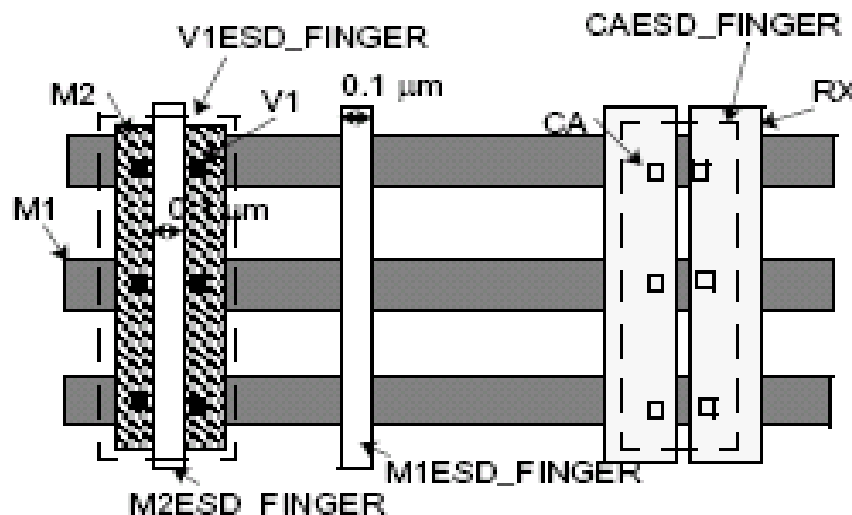
Key ESD Design Parameters



- Robust wiring between pad and ESD devices
- Appropriate sized ESD devices
- Low power/ground bus resistance
- Optimized internal circuit devices

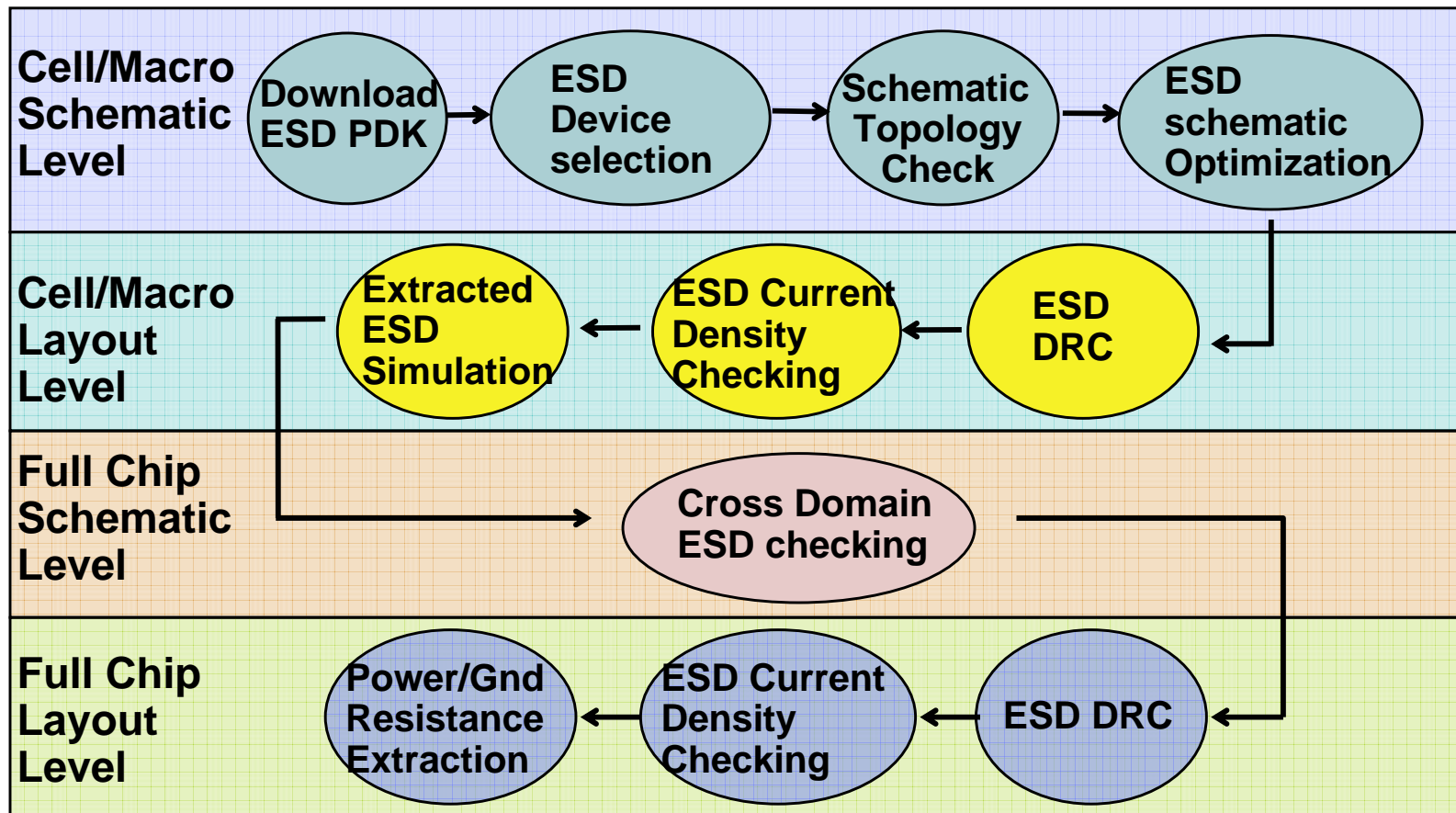
Existing ESD tools and limitations

- ESD Design Rule Checker (DRC)
- Limited ESD path-only simulation ---- Impact on internal devices ignored
- Problems with current approach
 - DRC cannot be used until layout level
 - ESD FEOL and BEOL rules too complex for DRC decks
 - ESD DRC rules limited by the number of testcases used
 - Rigid, non-flexible ESD solutions



Example of a complex case when using DRC to check for minimum BEOL wire width from pad to ESD device

ESD Design Methodology

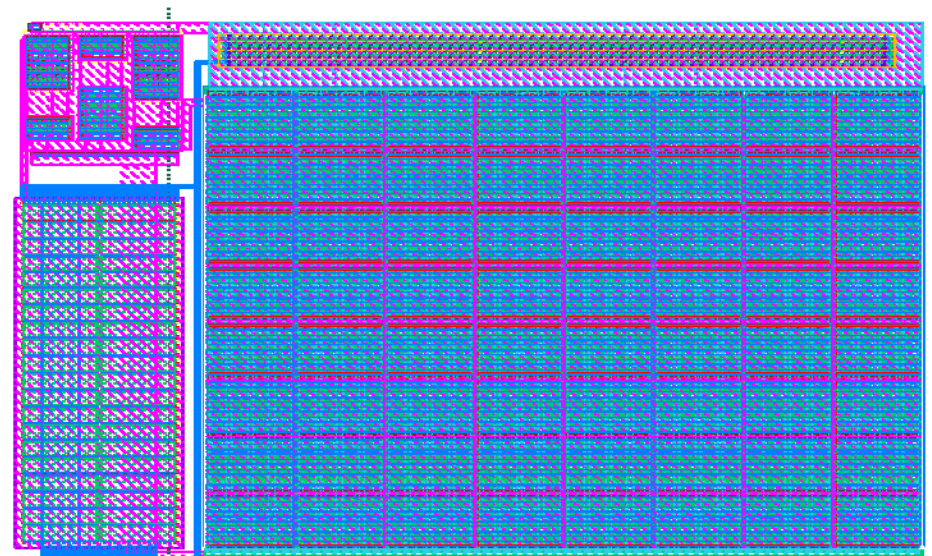
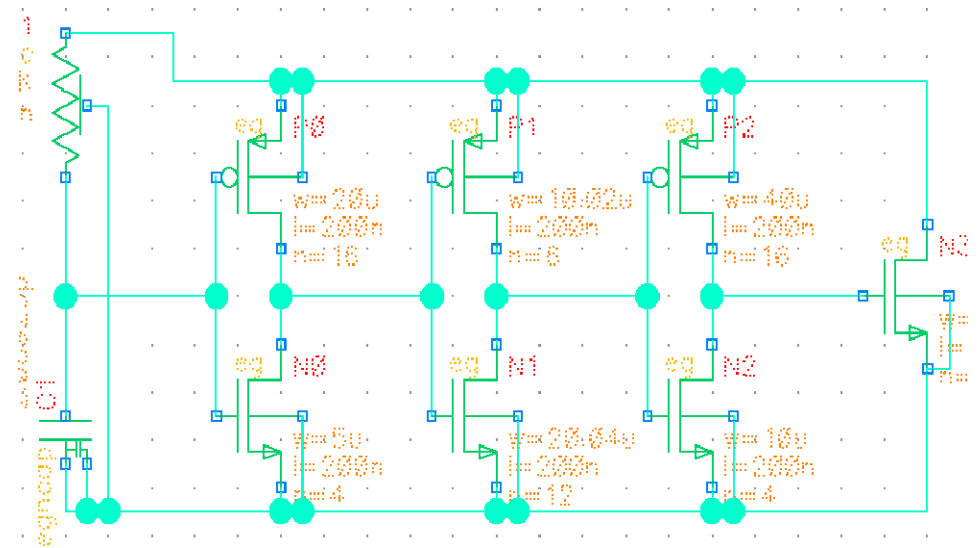


- ESD robustness evaluated and verified at each stage of a standard circuit design flow
- Right tool used to check the right rule

ESD Physical Design Kit (PDK)

Checking Level	Design/Checking Tool
Cell Schematic	ESD PCell from ESD PDK
	ESD Schematic check tool
	ESD Simulation tool

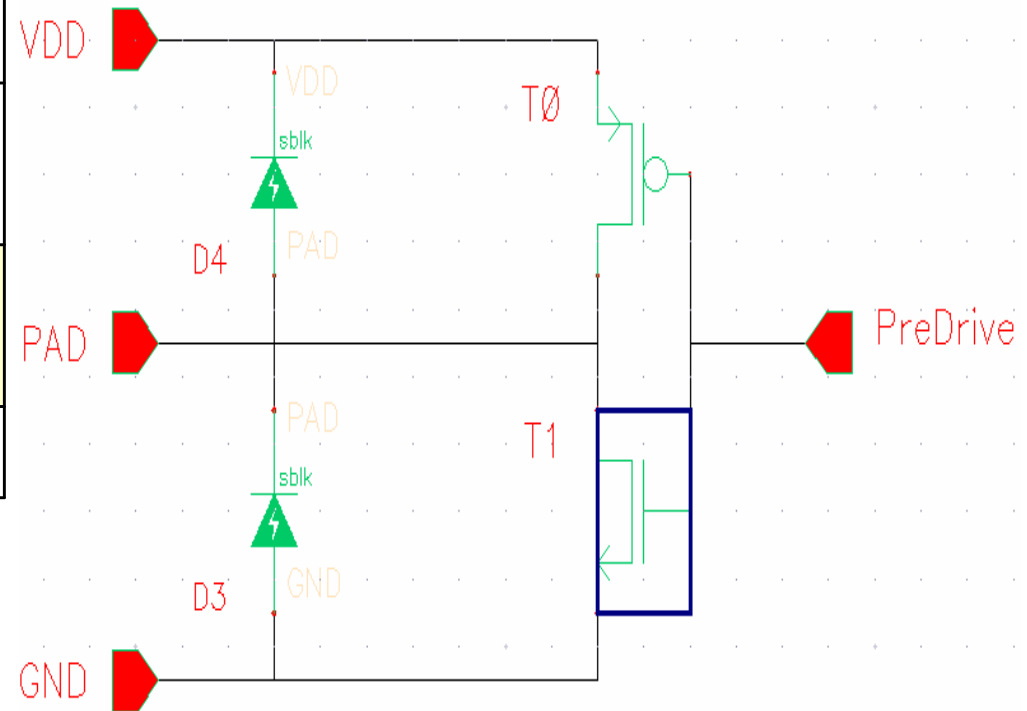
- ESD PDK consists of flexible ESD PCell with their schematics and layout
- Multiple design parameters can be varied such that the device can be optimized to the area available
- Example shown of an ESD RC-triggered Power Clamp PCell schematic and layout



ESD Schematic Topology Checks

Checking Level	Design/Checking Tool
Cell Schematic	ESD PCell from ESD PDK
	ESD Schematic check tool
	ESD Simulation tool

- Tool reads schematic netlist to determine the configuration of the active circuit devices
- Configurations checked for valid characteristics like parameters, net types etc.
- Example shown of a check which highlighted the single NFET driver when the ESD rule required it to be stacked



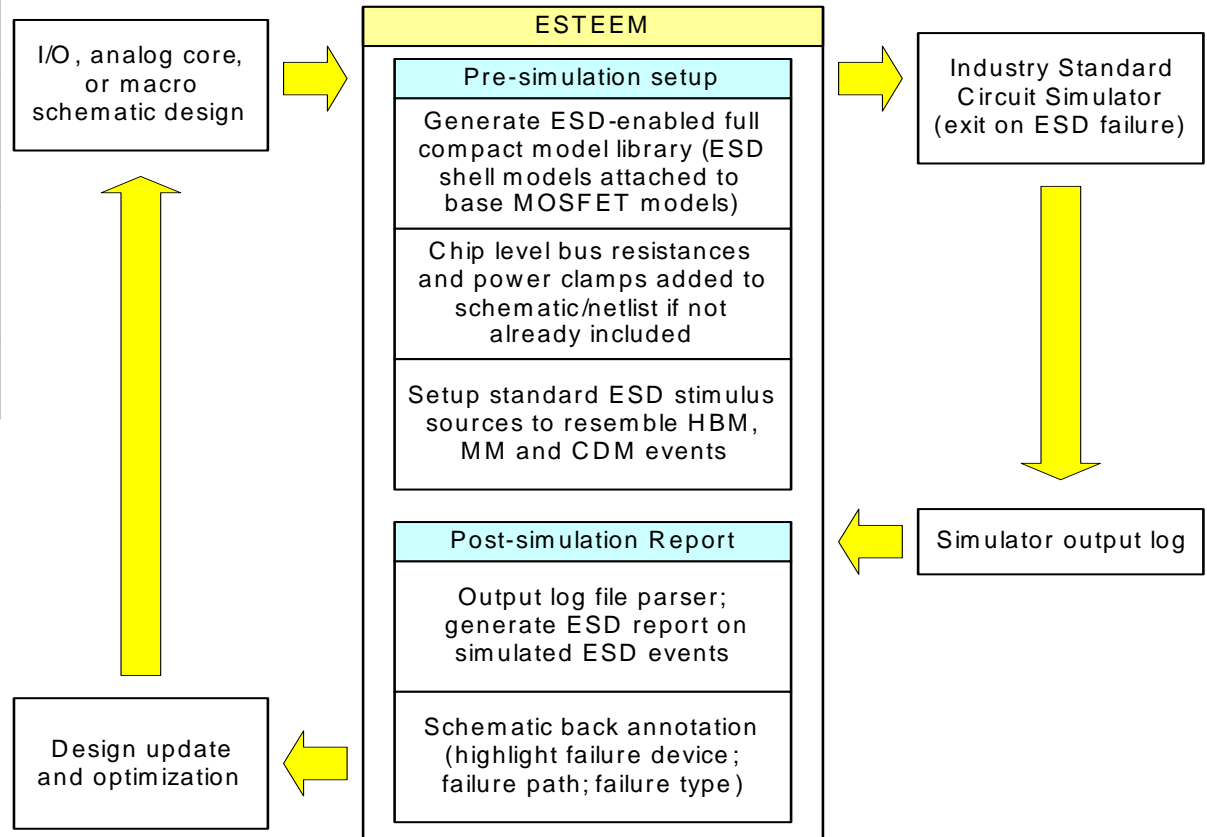
ESD19a: The number of driver fets, minus pass through transistors, connected to pad net 'PAD' must be stacked

Found fets in series 'MT1'

ESD Schematic Optimization

Checking Level	Design/Checking Tool
Cell Schematic	ESD PCell from ESD PDK
	ESD Schematic check tool
	ESD Simulation tool

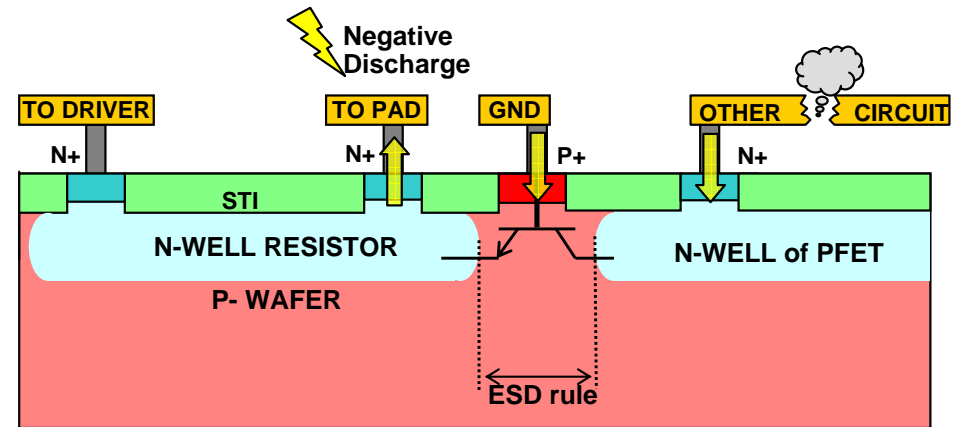
	HBM (kV)	MM (V)
IP	Testing/Simulation	
PLL pin	4.0*/7.0	200/250
12.8G RX pin	4.0/4.0	225/200
12.8G TX pin	4.25/4.0	200/200
1.8V bi-di I/O pin	>4.0/5.4	270/245
3.3V bi-di I/O pin	>4.0/7.3	340/350



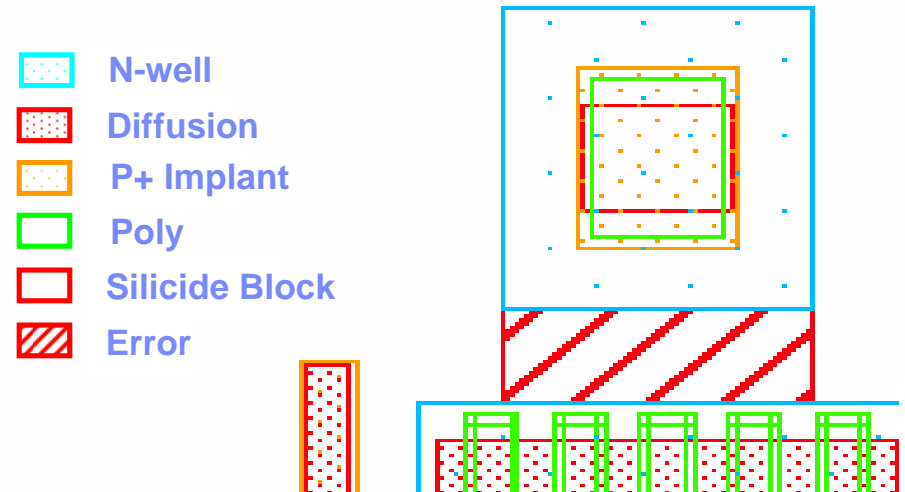
- Simulation tool highlights any failures in ESD device or internal circuit devices
- Simulation results correlate well with actual ESD testing data

ESD Design Rule Checker (DRC)

Checking Level	Design/Checking Tool
Cell Layout	ESD DRC
	ESD BEOL current-density checking tool
	Extracted ESD Simulation



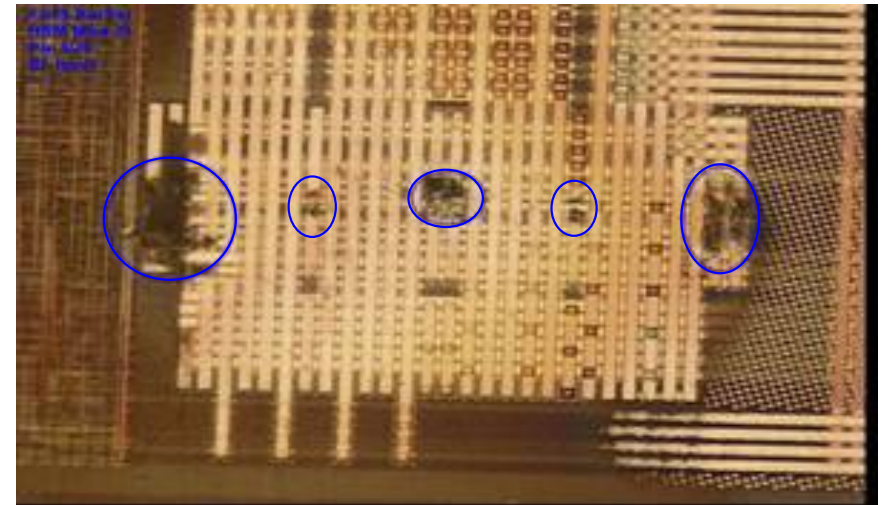
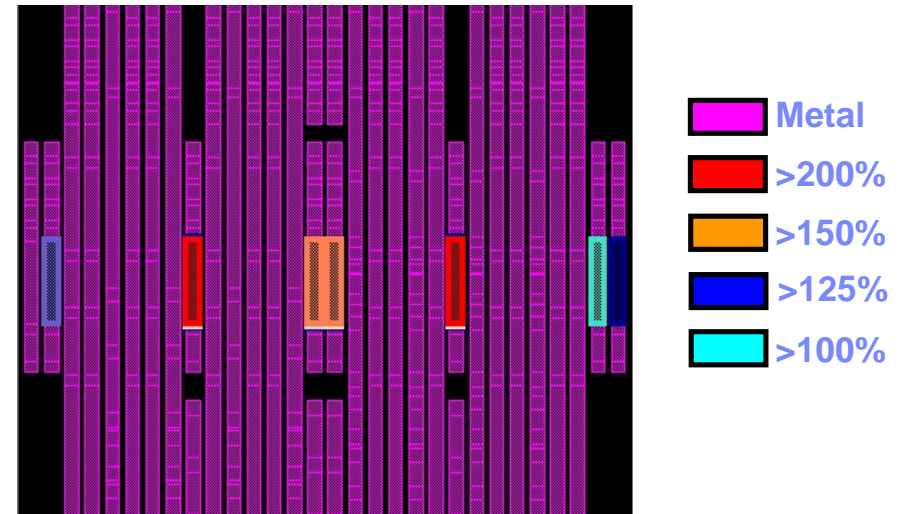
- **Example 1: Parasitic npn bipolar that can occur when 2 N-well (connected to different pad) are close to each other**
- **Example shown of a DRC error between N-wells of a N-well resistor and a PFET**
- **Example 2: Presence of appropriate sized latchup guardrings**



ESD Current Density Tool

Checking Level	Design/Checking Tool
Cell Layout	ESD DRC
	ESD BEOL current-density checking tool
	Extracted ESD Simulation

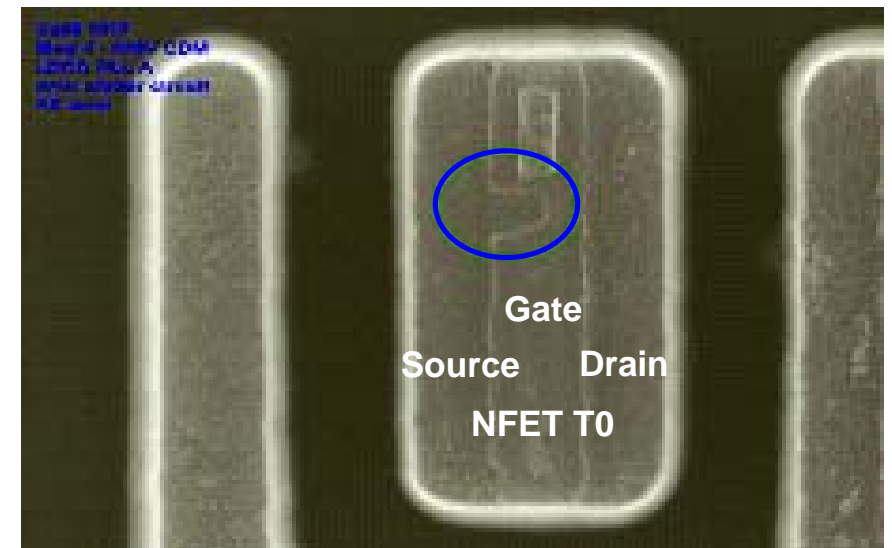
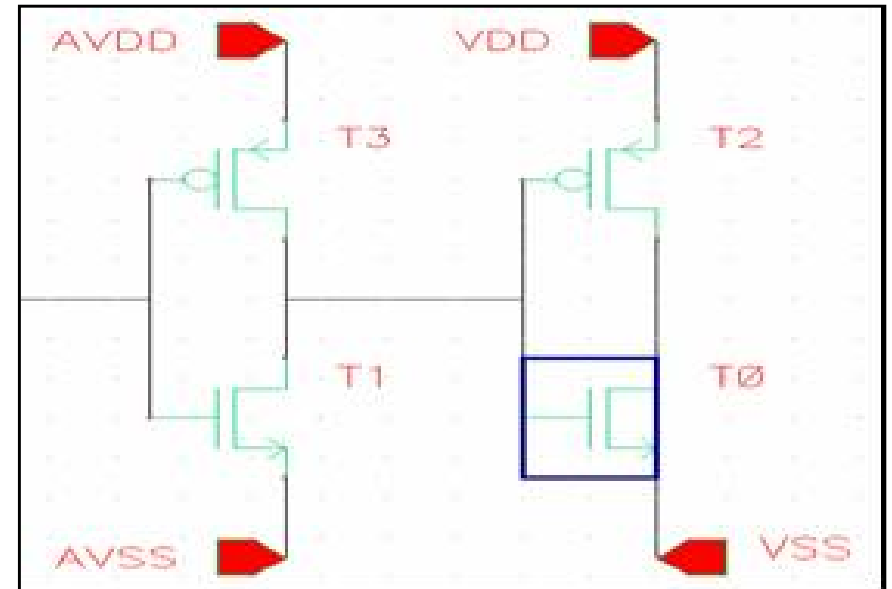
- Tool performs static current density analysis using specified maximum allowed values
- Improved and flexible error analysis for fast designer debug
- Example shown of a correlation between results from tool and PFA image after ESD test



Cross-domain Schematic Checking Tool

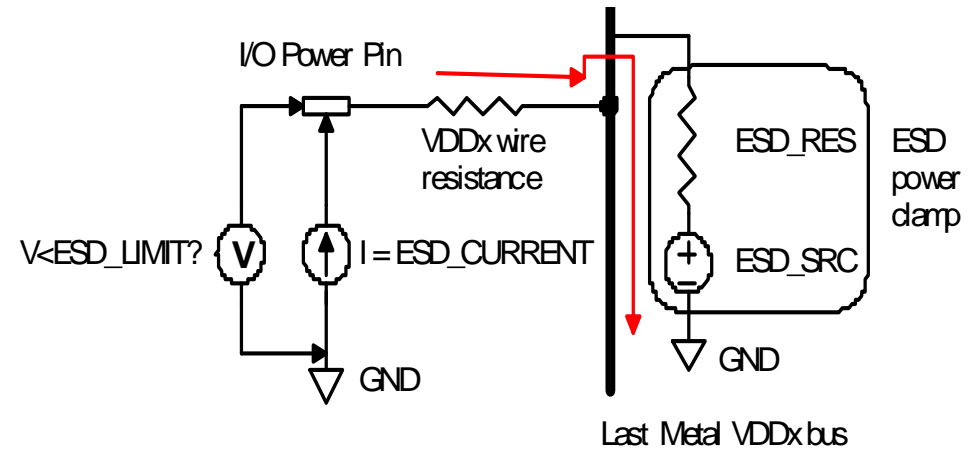
Checking Level	Design/Checking Tool
Full Chip Schematic	Cross-domain ESD schematic checking tool

- Cross-domain devices have their terminals connected to 2 different power domains
- Tool reads in full chip schematic netlist to identify cross-domain device
- Example shown of a correlation between results from tool and PFA image after ESD test



Power bus resistance extraction Tool

Checking Level	Design/Checking Tool
Full Chip Layout	ESD DRC
	ESD BEOL Current-density checking tool
	Power/Ground bus resistance extraction tool



- Tool extracts bus resistances to each instance of power clamps
- Effective bus resistance compared against specified maximum allowed bus resistance
- Example showing excellent correlation between low CDM experimental results and I/Os that had excessive power bus resistance

