

Analysis of Power Delivery network of Multiple Stacked ASICs using TSV and Micro-bumps

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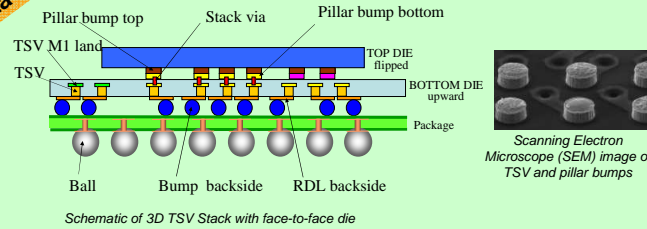
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Introduction: 3D Integration

Why ?

- Reduced area
- Increased performance
- > signal transmission pathways
- Heterogeneous die assembly:
 - functionalities (memory, processor, power management,...)
 - technologies (ideally the best techno for each module)

What ?



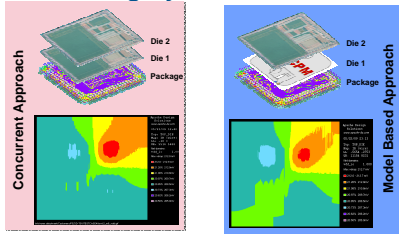
How ?

- 3D integration → new challenges in Power Delivery Network (PDN):
- Thermal Integrity
 - Signal Integrity
 - Bottom die switching and package distance
 - noise impact on top die
 - Power Integrity
 - ...
- need 3D Design Solutions

3D Power Integrity Solution

- Challenges:**
- Missing full-design database of one or more die
 - Support dies of different technologies
 - Early analysis to optimize TSV density and placement

Power Integrity flow



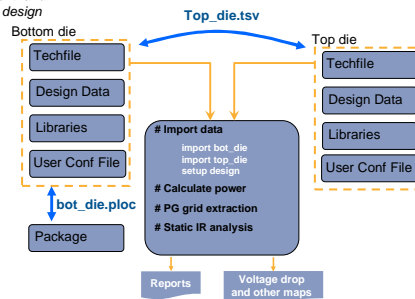
Two Simulation approaches

Concurrent Simulation Flow: Full design database available for both dies

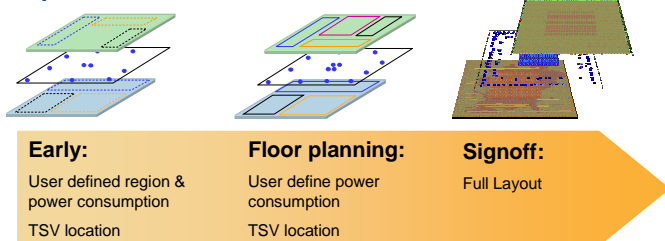
Model Based Simulation Flow: a Chip Power Model (CPM) replaces the design database of the missing die

Flow overview

- 2 die stack
- Different technology support
- Voltage Source Location files:
 - bot_die.ploc: define bottom die location and metal layer where the package is plugged (for both top and bottom die power/ground nets)
 - Top_die.tsv: define top die position and connexion to the bottom die



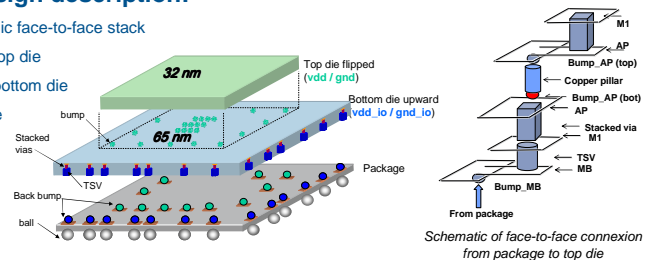
TSV Optimization flow



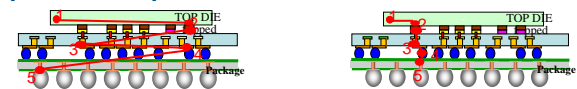
3D Power Integrity Results

3D Design description:

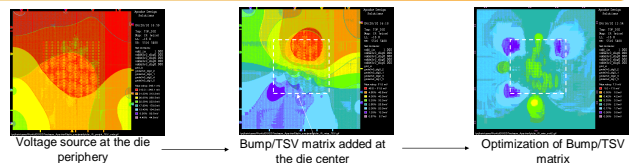
- logic/logic face-to-face stack
- 32 nm top die
- 65 nm bottom die
- package



TSV placement optimization

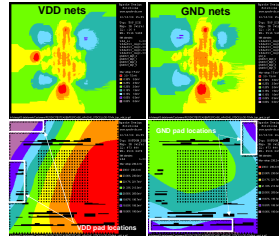


Static IR-Drop analysis to optimize current distribution of the top die

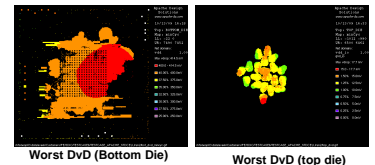


Static and Dynamic results

Top Die IR map with bottom die included



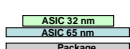
Bottom die IR map with top die included
Dynamic drop results from bottom die and top die PG mesh (VDD and GND)



Dynamic drop results from bottom die and top die PG mesh (VDD and GND)

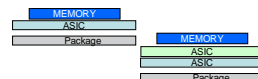
Conclusion

TODAY ...



- Dynamic and Static IR Drop analysis
- Two stacked dies + package
- Heterogeneous technology system
- Two simulation approaches
- TSV placement optimization

... TOMORROW



- Extend the number of stacked die analysis
- Heterogeneous functionality : memory/ASIC
- New topics to investigate: Signal Integrity, Reliability, Thermo-Mechanical effects,...