

Managing Variation at Advanced Nodes in Timing Verification

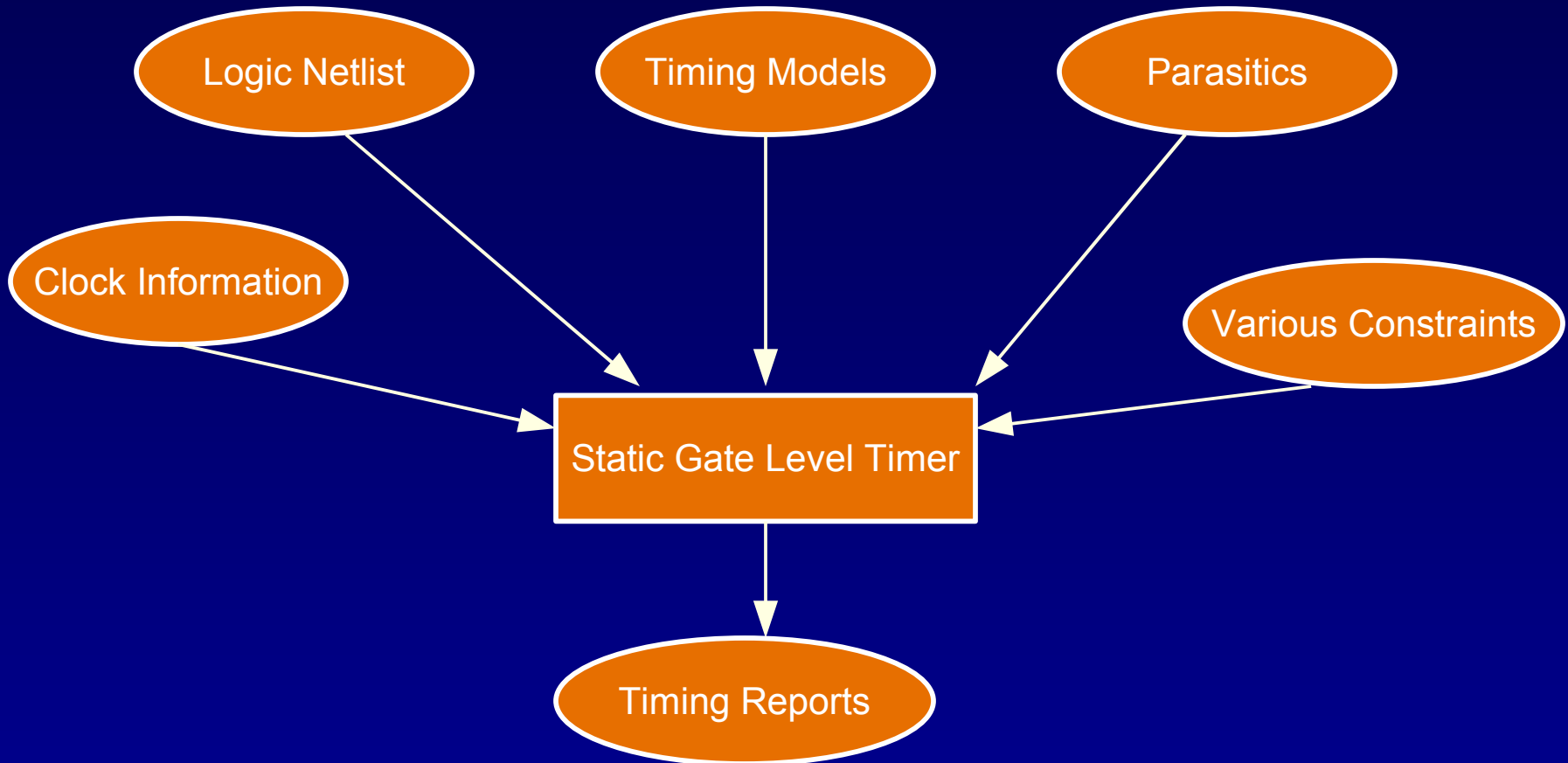
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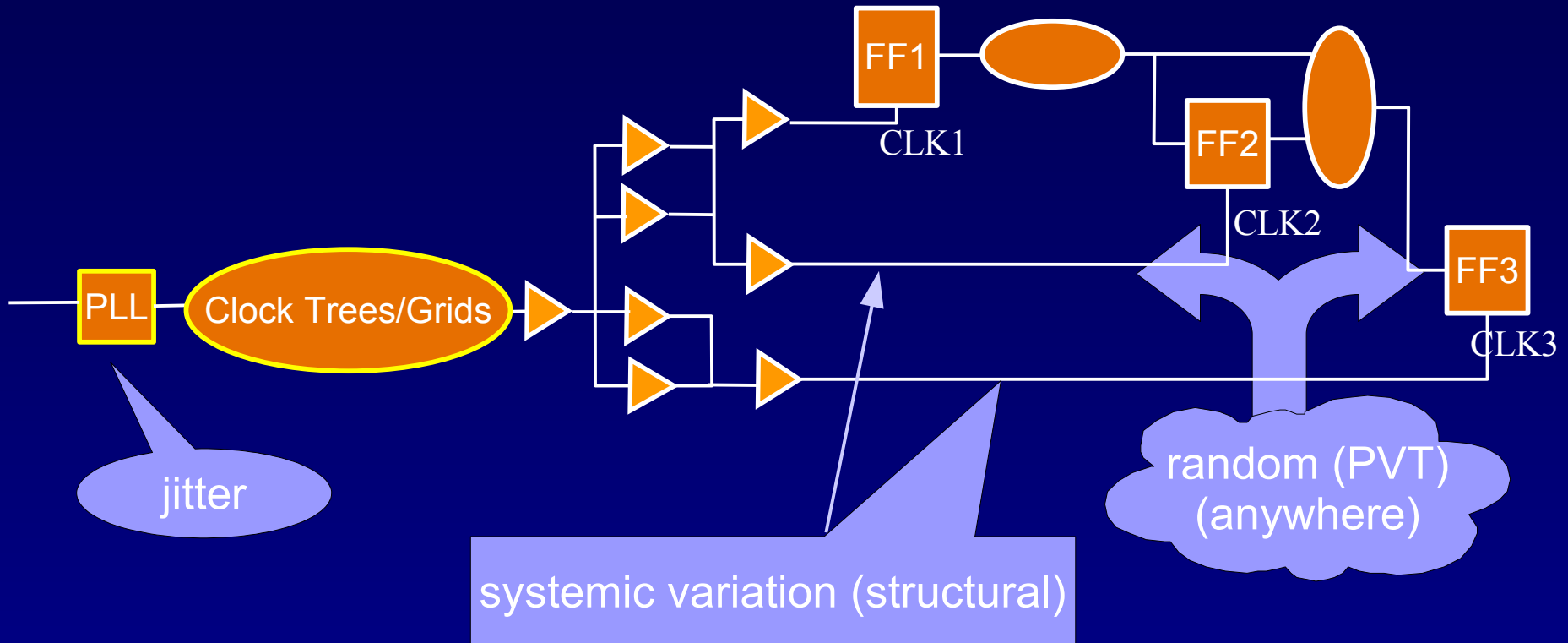
Outline

- **Motivation**
- **Multi-corner timing verification**
- **New hybrid flow including statistical timing analysis**
- **Case study of microprocessor design at 40nm**
- **Summary & discussion**

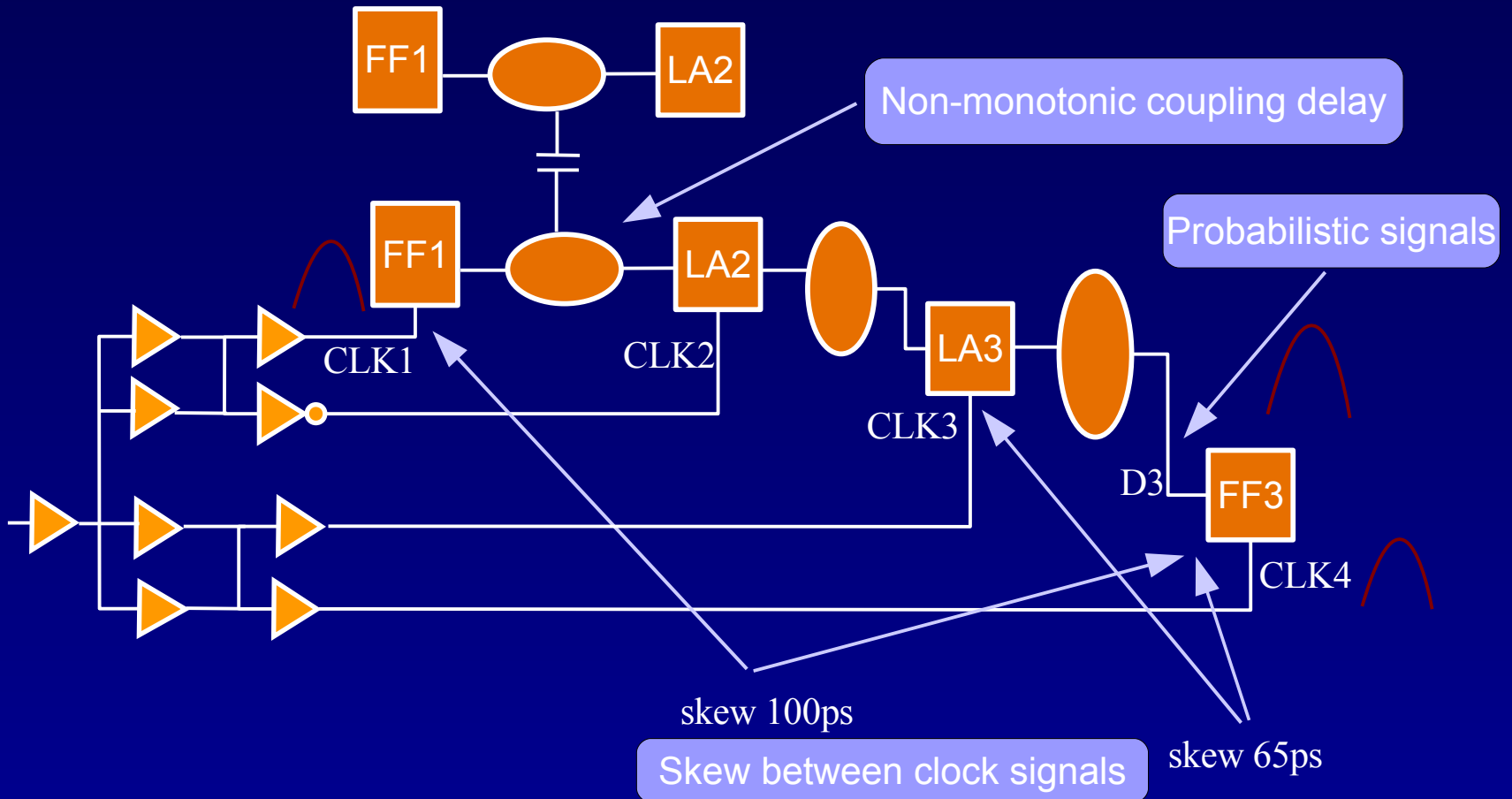
Timing Verification



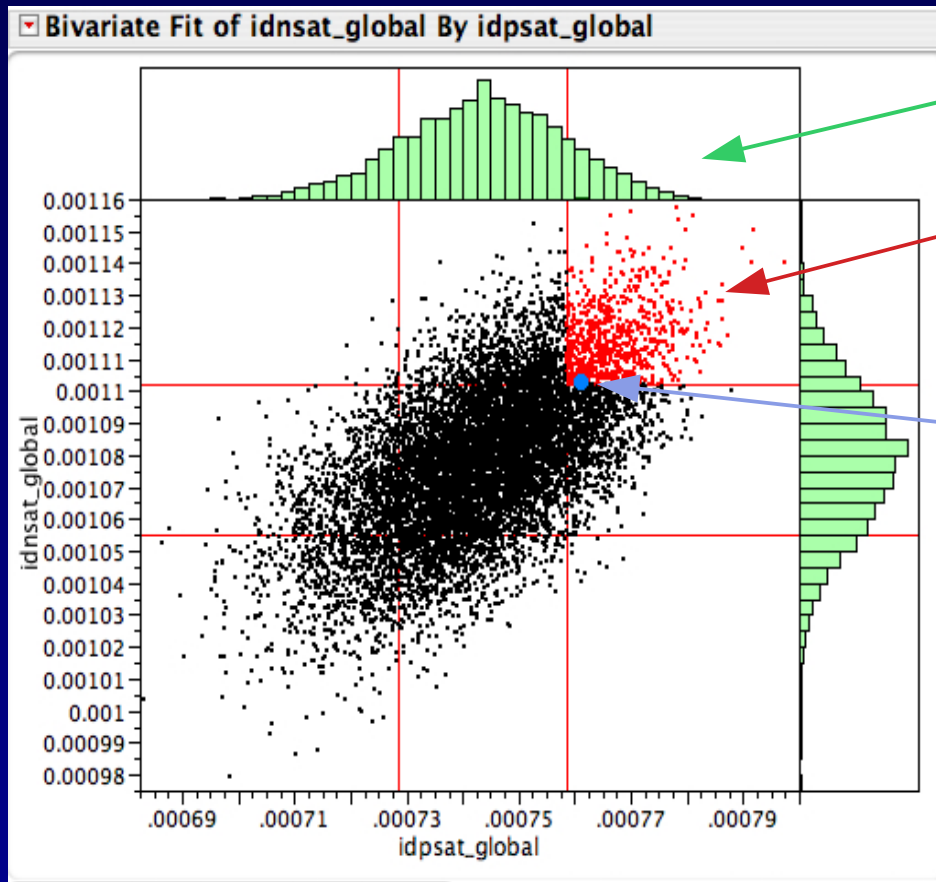
Sources of Variation



Impact of Variation



Process Corner Derivation *



distribution of IdSat

candidate corners
(beyond certain probability)

highest probability – chosen
as fast-fast process corner

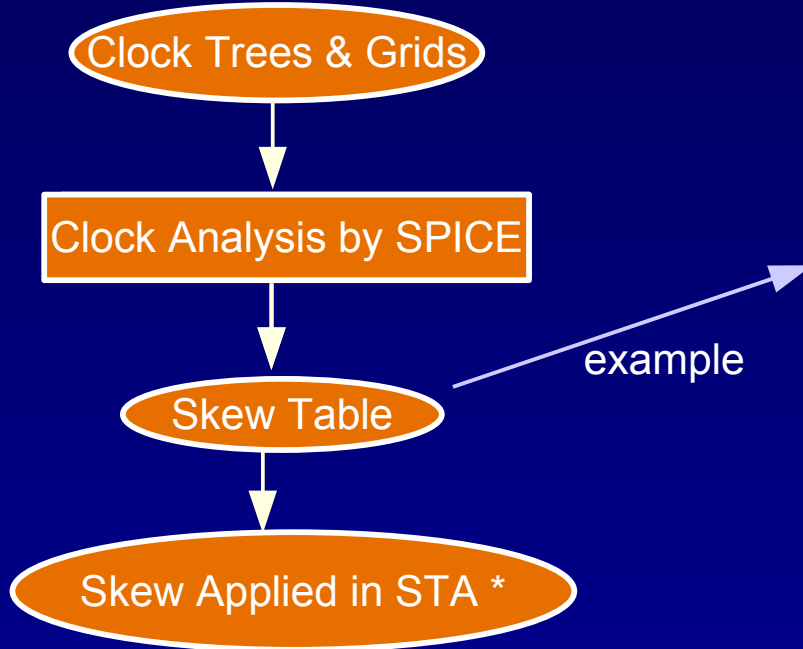
* Barker, patent pending

Pmos and nmos IdSat relationship

Statistical Analysis in Existing Flow

Memory design

Clock network analysis



		Same L2 **		
Min skew*	L1 _{same}	L1 ₁₀₀	L1 ₂₅₀	L3 _{same}
L2 Min Skew (ps)	0	1.2	2.4	12
L1 Min Skew (ps)	2	6.0	7.6	16

* Xiao etc. DAC 2009 UT

Previous Min Timing Verification*

1. Min PVT: fast process corner, high voltage, low temperature

2. Characterization at min PVT

4. Clocks skew at min PVT

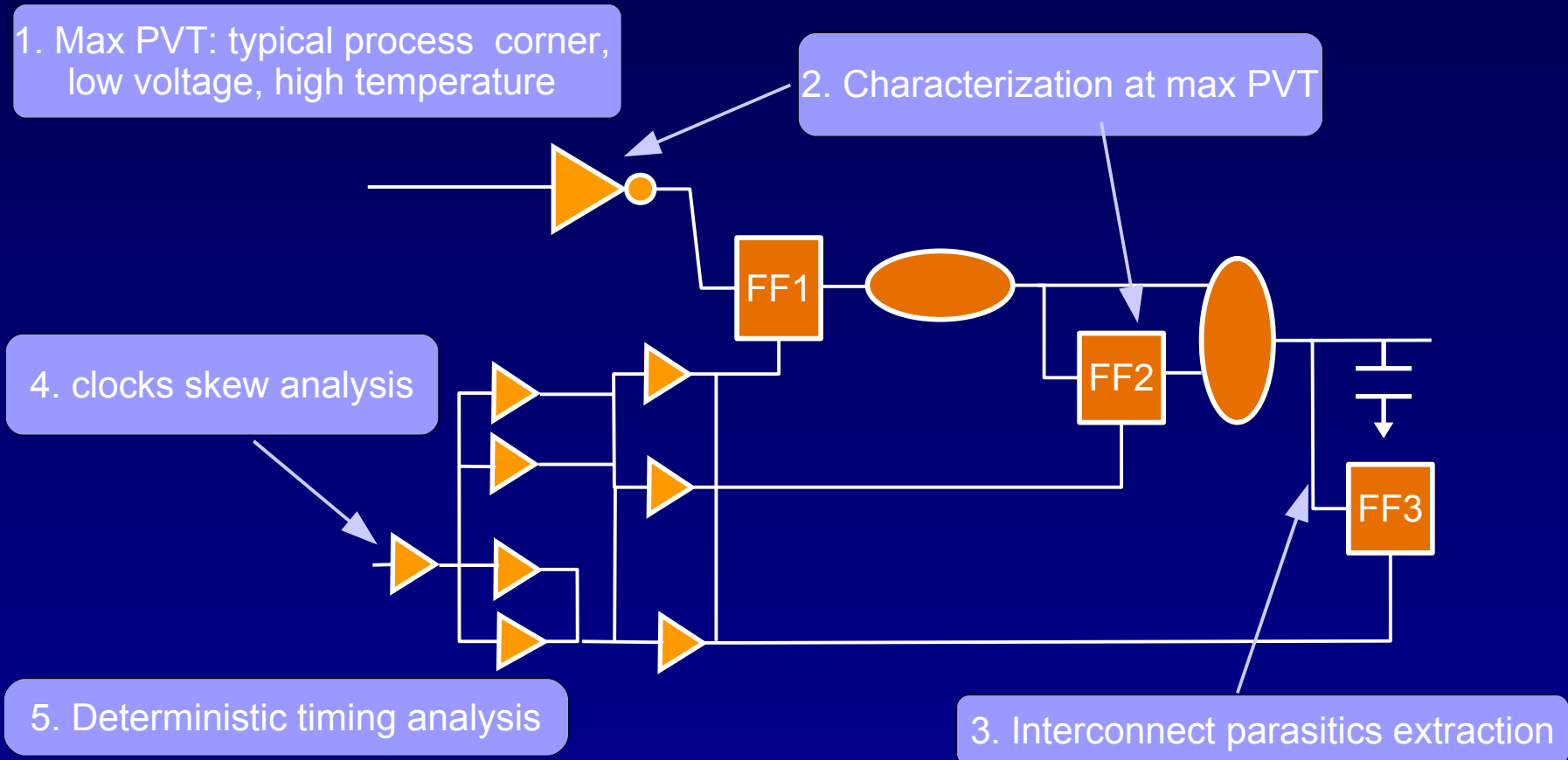
5. Deterministic timing analysis with additional margins

3. Interconnect parasitics extraction (for smallest delay)

Pessimistic. Possibly waive violations.

*Nawathe, JSCC, Jan. 2008

Previous Max Timing Verification*



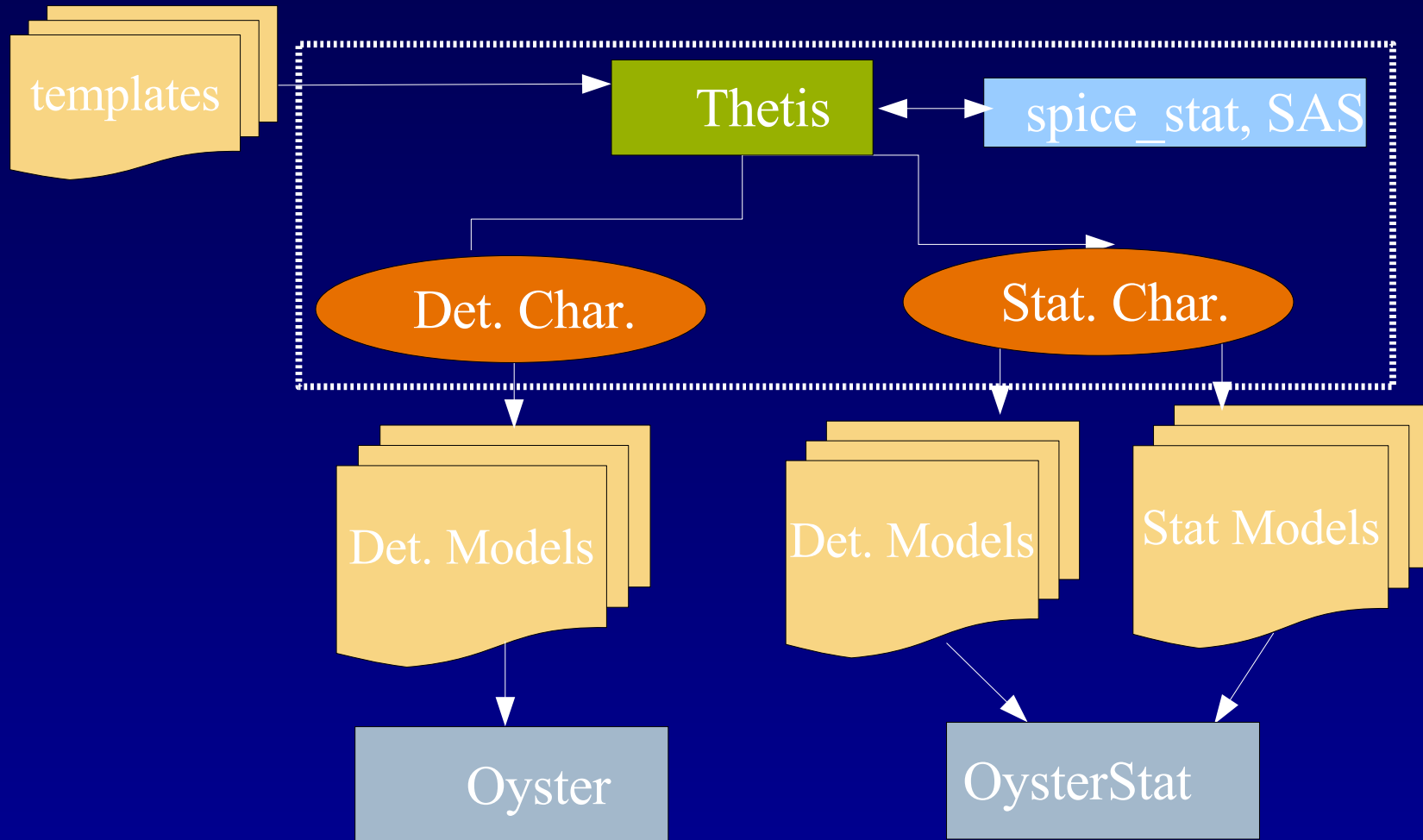
Actual speed of a manufactured chip?

***Nawathe, JSCC, Jan. 2008**

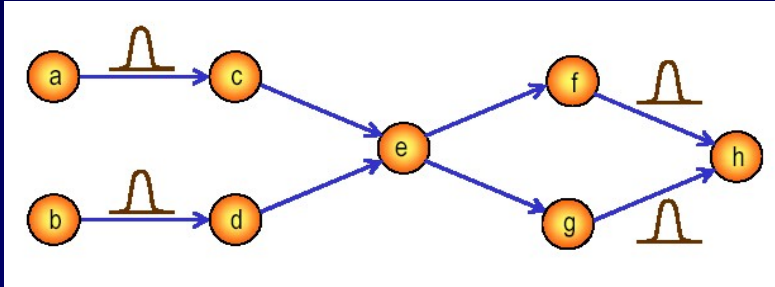
SSTA Survey

- **Extensive research in the last decade**
 - Blauuw, "Statistical Timing Analysis: From Basic Principles to State of the Art", TCAD, April 2008S
- **Commercial & in-house tools available**
 - Ito, DAC UT 2009
 - Marhsal, DAC UT 2009
 - Results shown on 65nm designs
- **Challenges remain**
 - Immature statistical spice models
 - Moving from conventional flow to a full statistical flow
 - Benefits of statistical analysis at advanced nodes

New Hybrid Flow: Statistical Characterization *



New Hybrid Flow: SSTA Signals



$$RSM : Delay(tx, cl, X_i, R) = d_0(tx, cl)$$

$$+ \sum_{i=1}^n a_i(tx, cl) \cdot X_i$$

$$+ b(tx, cl) \cdot R$$

Nominal delay
from deterministic model

Global process variations

Local process variations (mismatch)

$$a_i = a_{i,0} + a_{i,1} \cdot tx + a_{i,2} \cdot cl + a_{i,3} \cdot tx \cdot cl$$

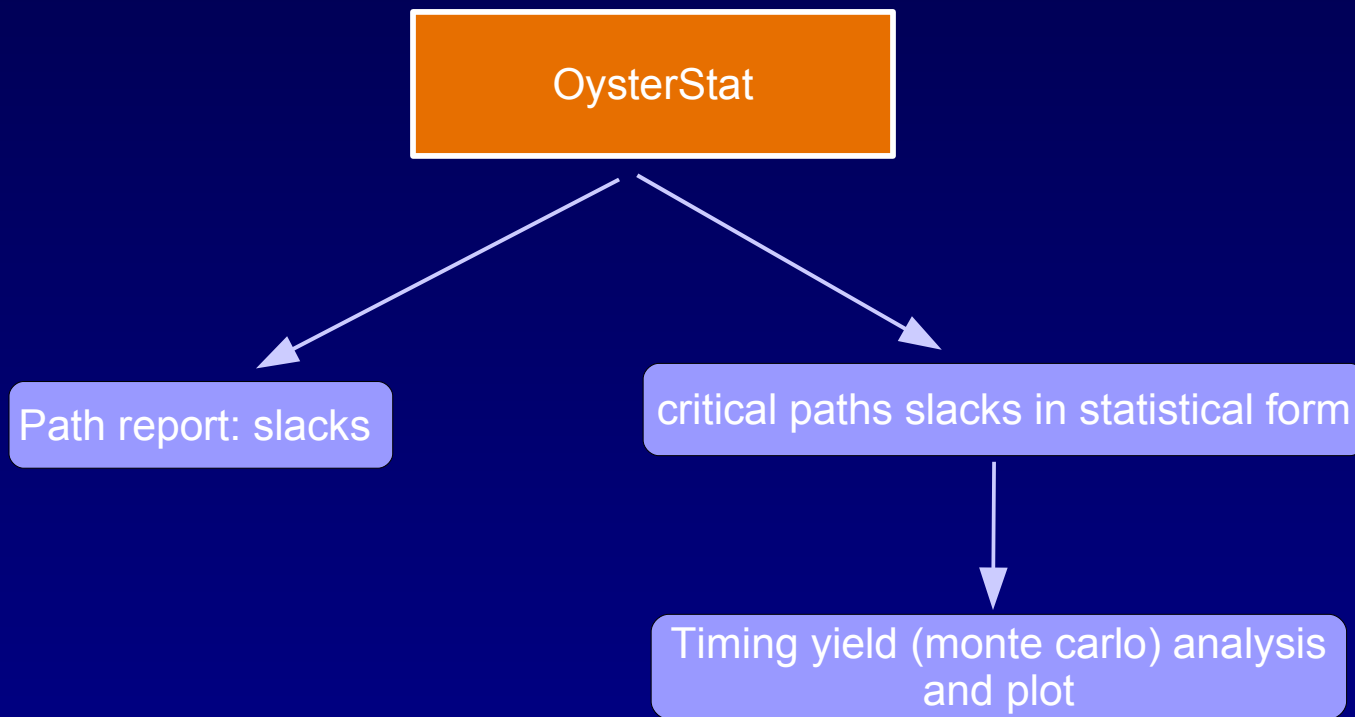
tx = Risetime at input

cl = Output load capacitance

X: variables for global process variation

R: variable for local process variation

New Hybrid Flow: SSTA Results



Timing yield: probability of chip running at a specified clock frequency

Chip yield: probability of chip working functionally after manufacturing

New Min Timing Verification

1. Min PVT: **typical** process corner, high voltage, low temperature

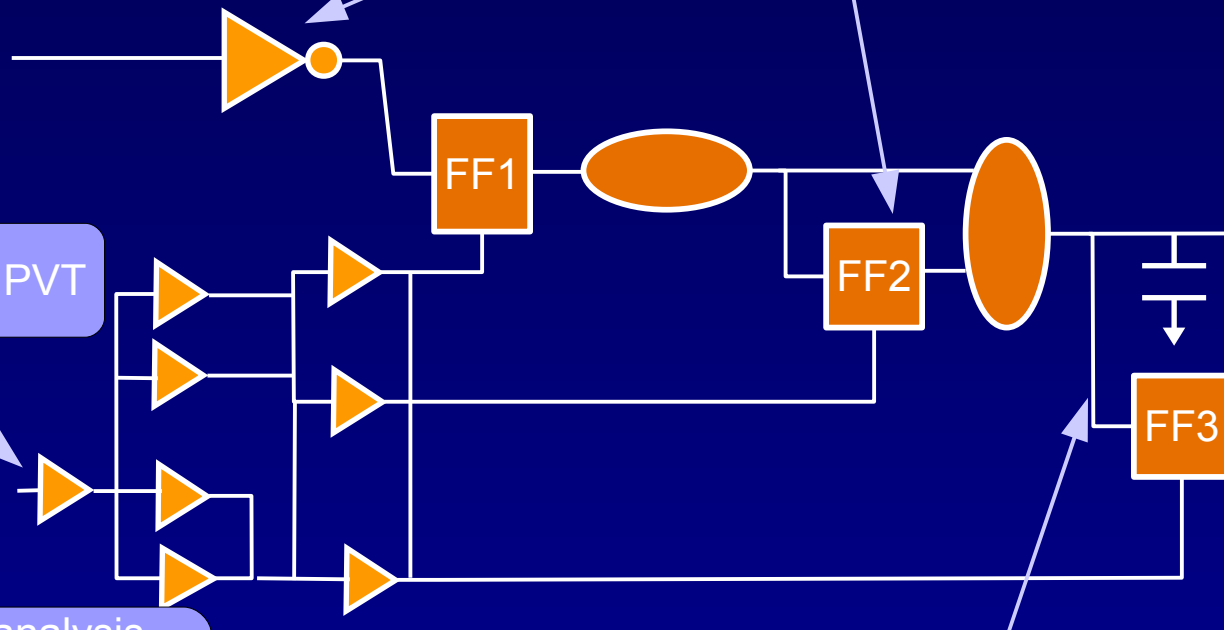
2. Characterization at min PVT : deterministic and **statistical** models*

4. Clocks skew at min PVT

5. **Statistical** timing analysis (no need to use process margin)

3. Interconnect parasitics extraction (for smallest delay)

* **statistical** models: in RSM for delay variaton



New Max Timing Verification

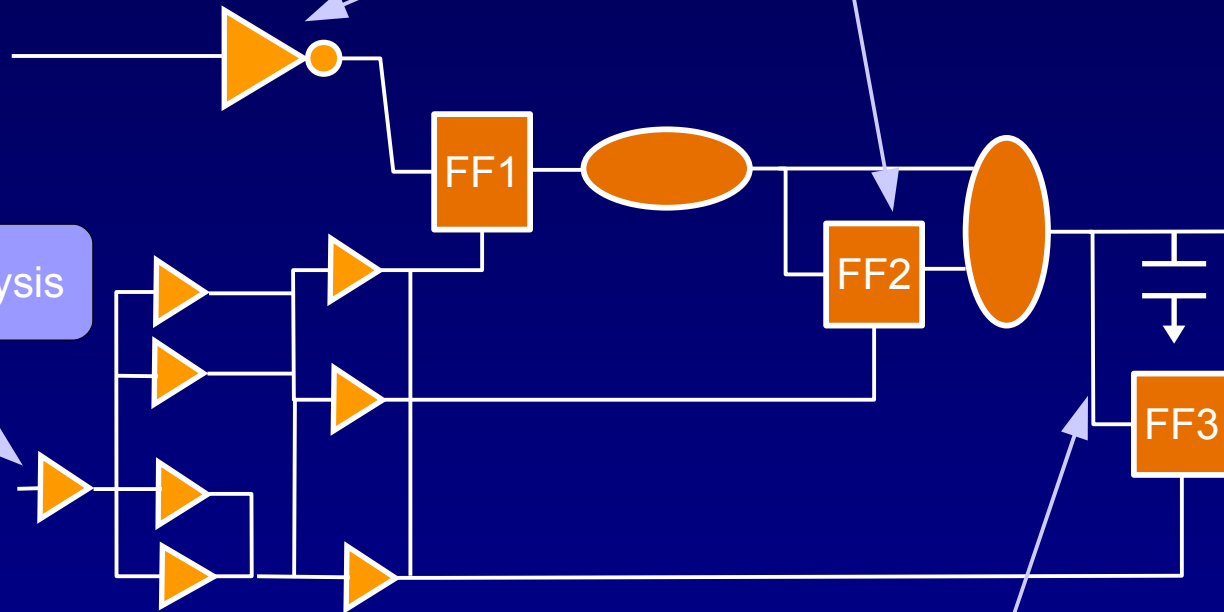
1. Max PVT: typical process corner, low voltage, high temperature

2. Characterization at max PVT: deterministic and **statistical** models

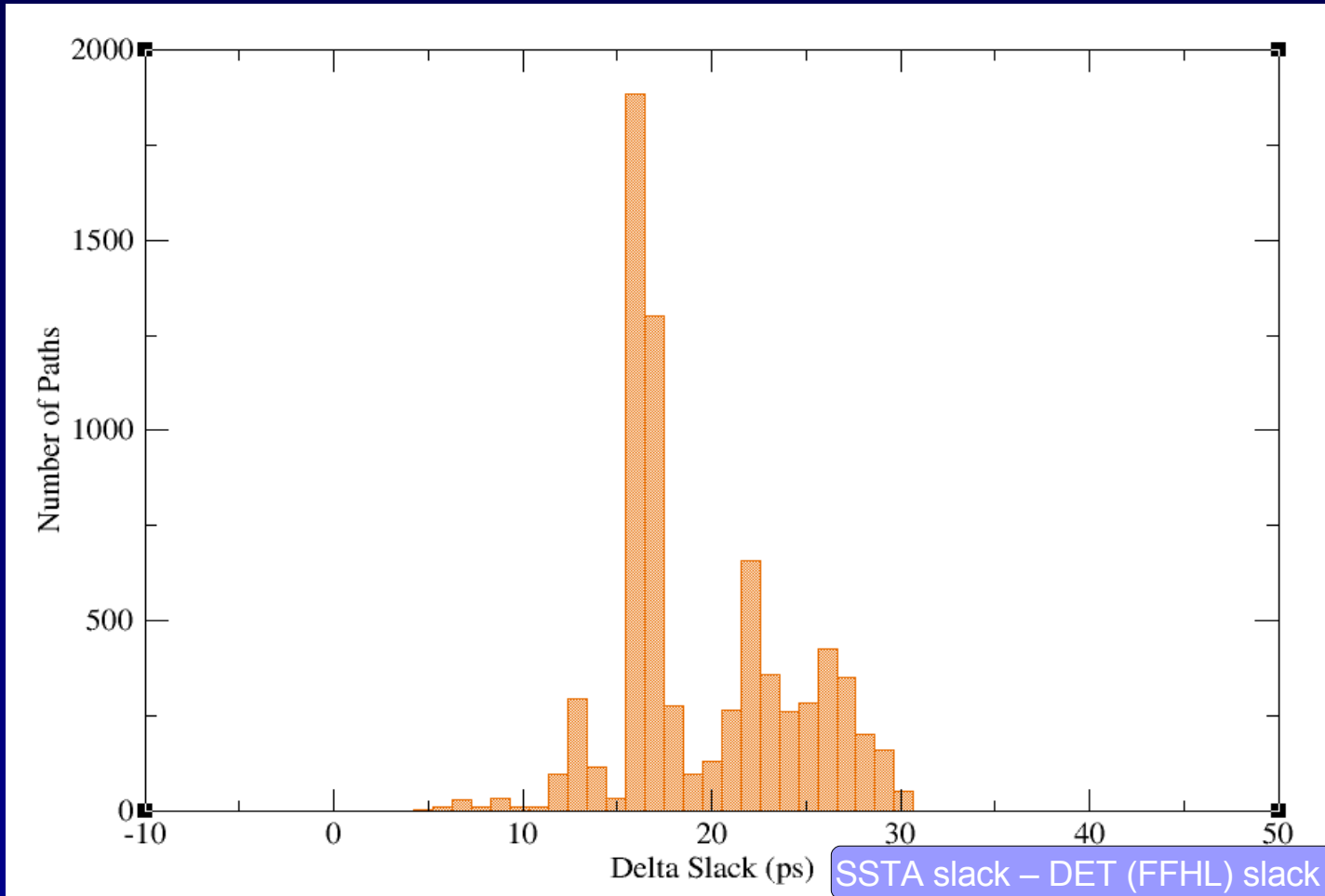
4. clocks skew analysis

5. **Statistical** timing analysis

3. Interconnect parasitics extraction

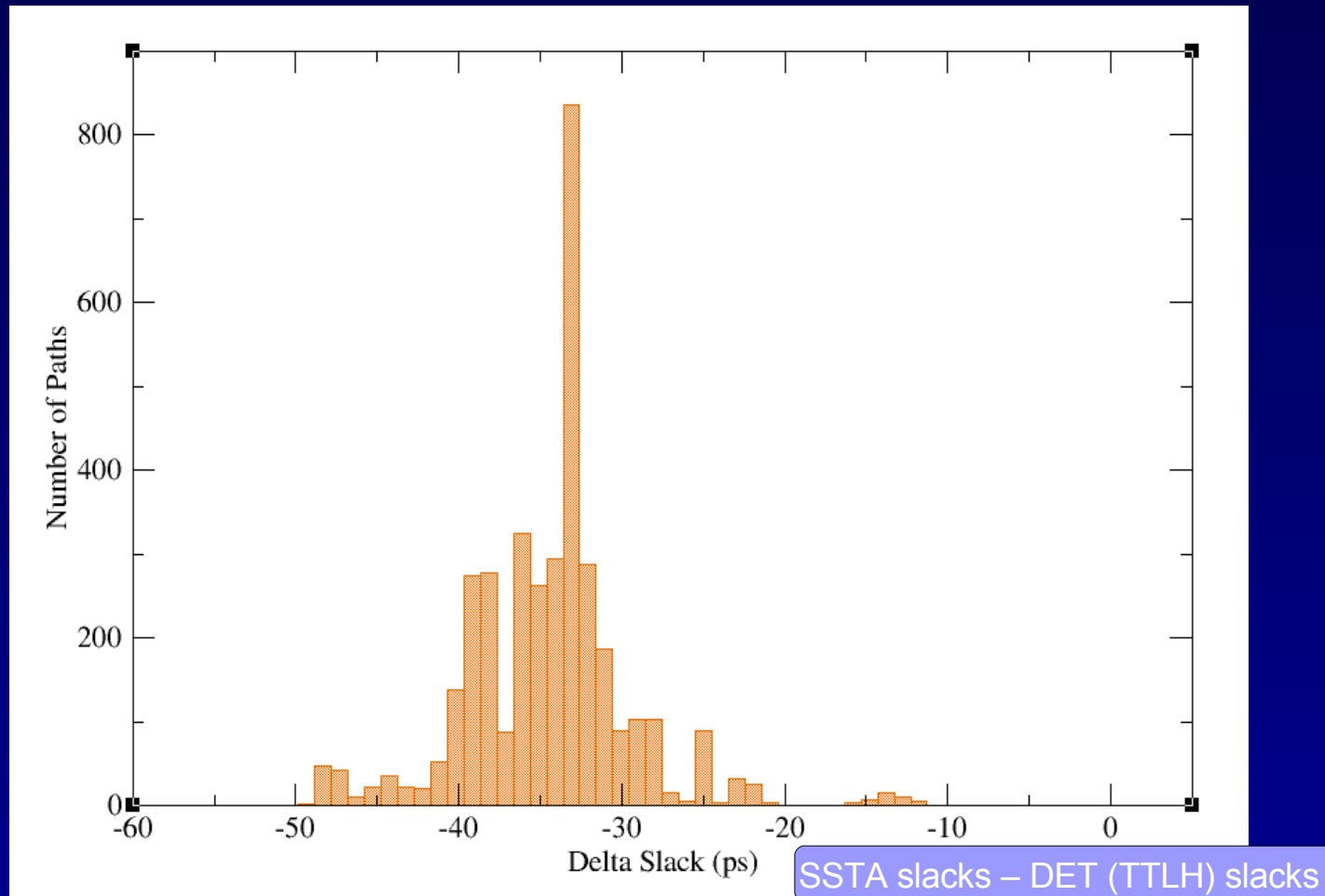


Min Timing Slack Changes



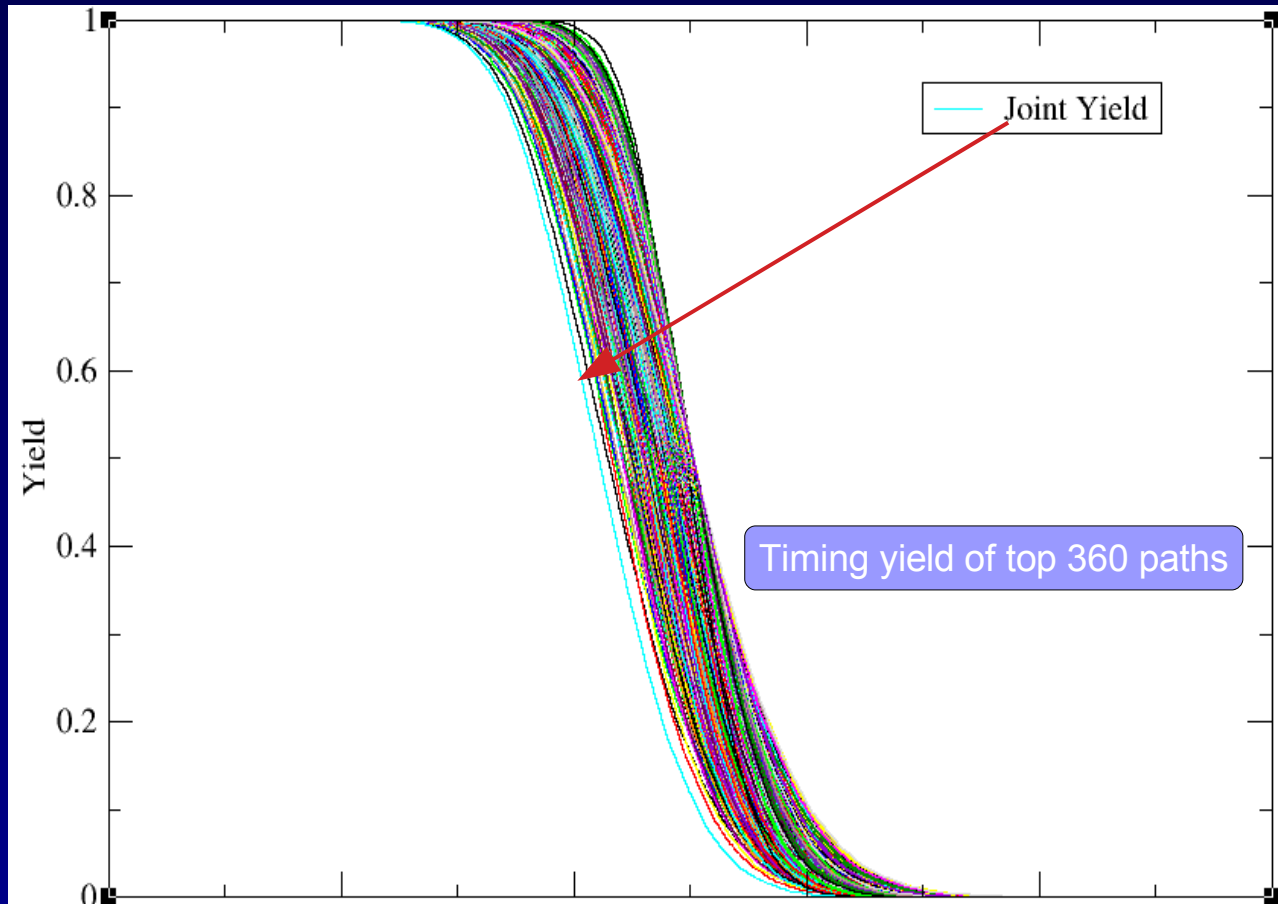
Slacks of the top 7000 paths increase in SSTA run.
(Pessimistic deterministic min timing.)

Max Timing Slack Changes



Slacks of the top 3000 paths decrease in SSTA run.
(Improvement is needed to achieve 90% timing yield.)

Timing Yield vs. Frequency



Single path timing yield: probability of a path working at a specified frequency.

Joint timing yield: probability of all paths working (reflects chip timing).

Lower than single path yield, due to local variation (mismatch).

Summary & Discussion

- **Timing flow evolving to account for PVT variation**
- **Adding SSTA in existing flow**
 - Reduce pessimism in min timing
 - Identify process sensitive paths
 - Help tune design to improve/achieve timing yield target
- **Challenges**
 - Integrate statistical clock and timing analysis
 - Dependencies between timing, IR drop and thermal conditions
 - Efficient variation aware optimization

Acknowledgment

- George Chen
- Michel Laudes
- Chung Chan