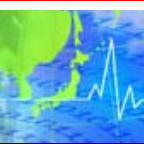




A New Generation Static Statistical Timing Analysis (SSTA) Based Design Flow for 40nm and 28nm CMOS Technology

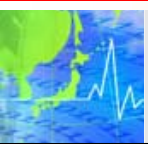
Authors: Terumi Yoshimura[†], Toshikatsu Hosono[†], Jun Li^{††}
and Janet Wang^{††}

[†]Fujitsu VLSI Limited , ^{††}Anova-Solutions Inc



Motivation

- The significance of process variation has been growing rapidly. SSTA is a very important method for designers.
 - What is the bottleneck to use of SSTA on 40nm/28nm ASIC designs?
 - Is there an available SSTA tool for huge ASIC designs?
 - Does SSTA provide advantages beyond relaxing timing?
 - What are the innovations and future plans?
- We can answer these questions!



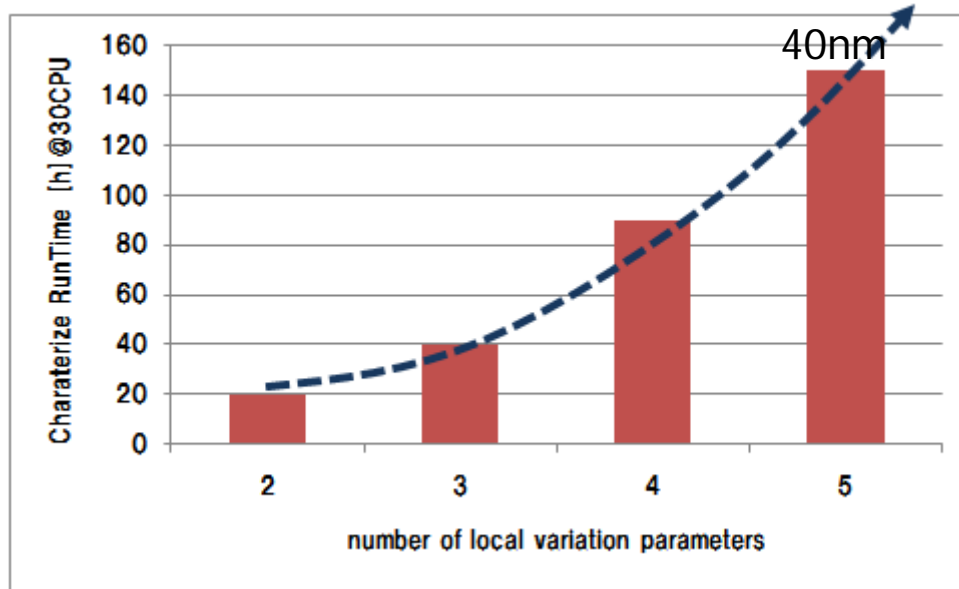
Background

■ Status of SSTA

- We began using SSTA for processors and ASICs at the 90nm node.
- We planned to integrate SSTA for 40nm/28nm as well.

However, we have serious issues

1. **Process variation and design difficulty have grown rapidly with the scaling of process.**
2. **SSTA has grown more expensive as chip size has increased and the number of process variation parameters has doubled from 40nm to 28nm.**

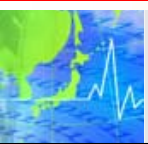


For example , runtime of characterization gets worse when number of local process variation parameters increase.

If the number of parameters increases from 2 to 5 , it makes runtime increase x8.

In 40nm with 5 parameters, the ASIC design needs 1000 cells per 3 vth kinds for 4 corners.

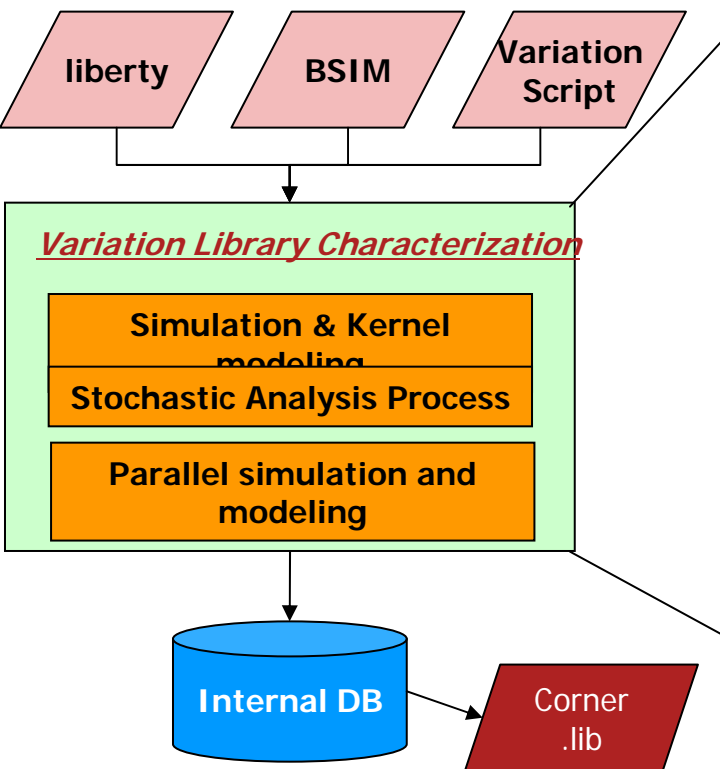
Totally 3000 cells need to be characterized for 4 P.V.T corners, which required about 3months



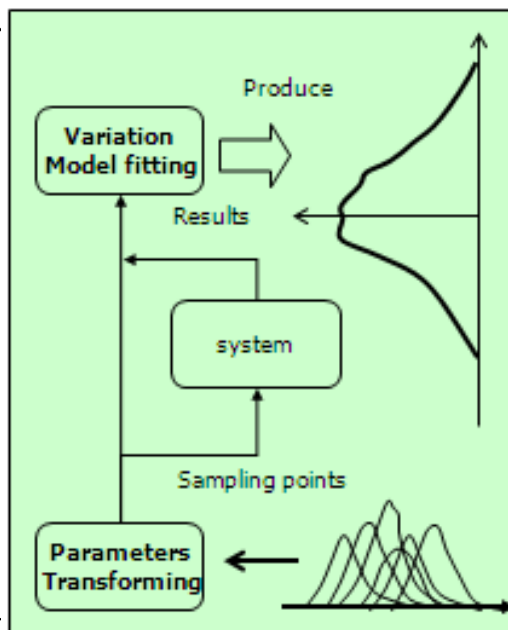
Innovation

Fast Statistical Library Characterization

Using S.A.P. for sensitivity model characterization.



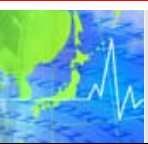
Stochastic Analysis Process – S.A.P. US PATENT



- Transform parameters' distribution to standardized distribution
- Orthogonal polynomial fitting standardized distribution parameters
- Reduced sampling points
- Weighted sampling in order to have better system distribution fitting results

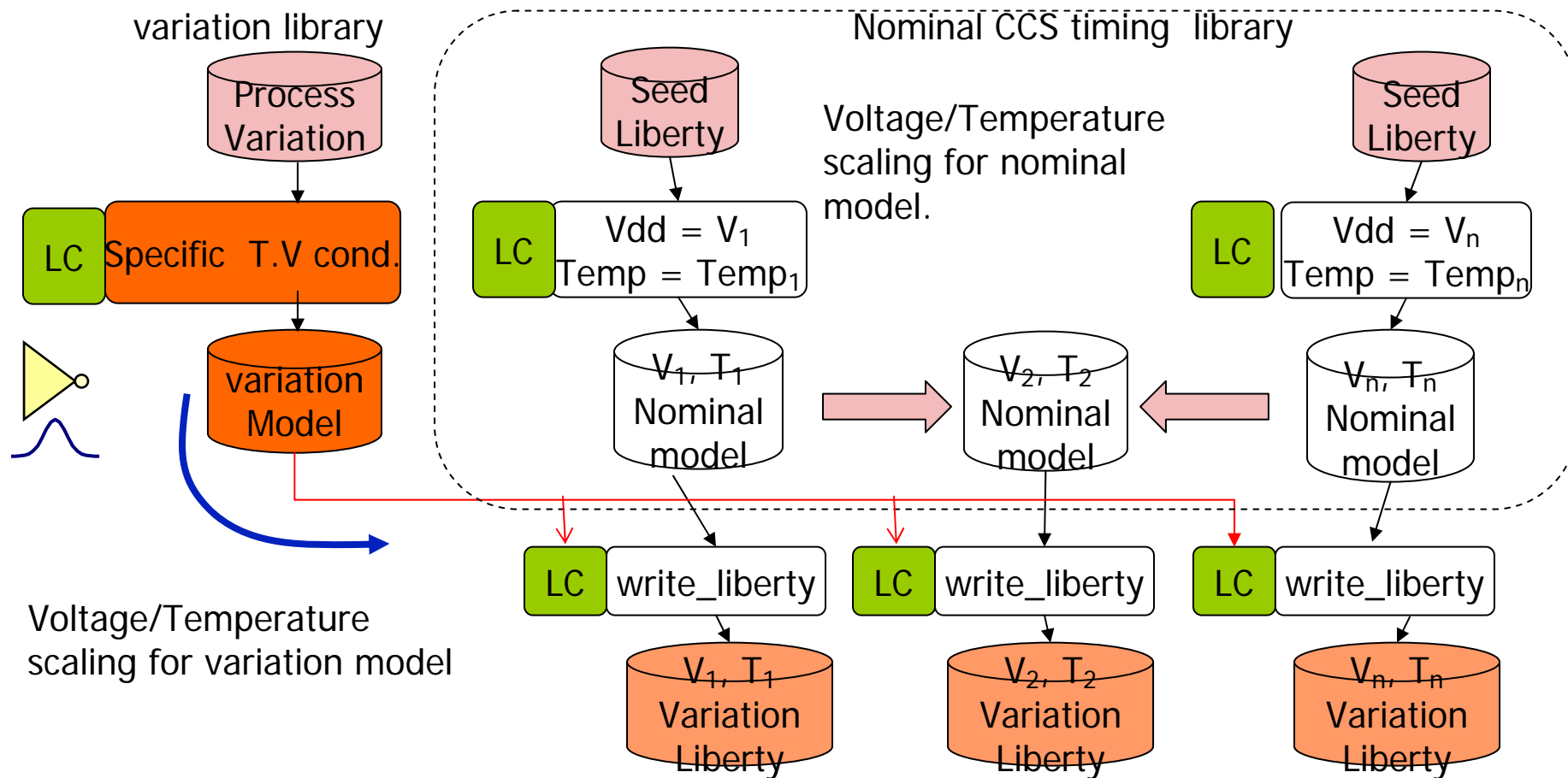
Fast, Scalable Monte Carlo

S. Y. Kumar, J. Li, C. Talarico and J. M. Wang, "A probabilistic collocation method based statistical gate delay model considering process variations and multiple input switching," *Proc. Design, Automation and Test in Europe (DATE)*, pp. 770 – 775, March 2005

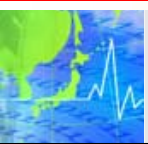


Innovation

Further run time improvements.



➤ Apply Voltage/Temperature scaling to other conditions not only nominal model but also variation model.



Innovation

■ Statistical Delay calculation, timing analysis

- Fast , Scalable SSTA : calculate each stage delay using SAP model sampling and delay, slew variation library.

- Canonical statistical formula is not used.

~~$$D = d_0 + \sum_{i=1}^n a_i \Delta X_i + a_{n+1} \Delta R$$~~

- sigma/gamma propagation instead of sensitivity parameter propagation in SSTA

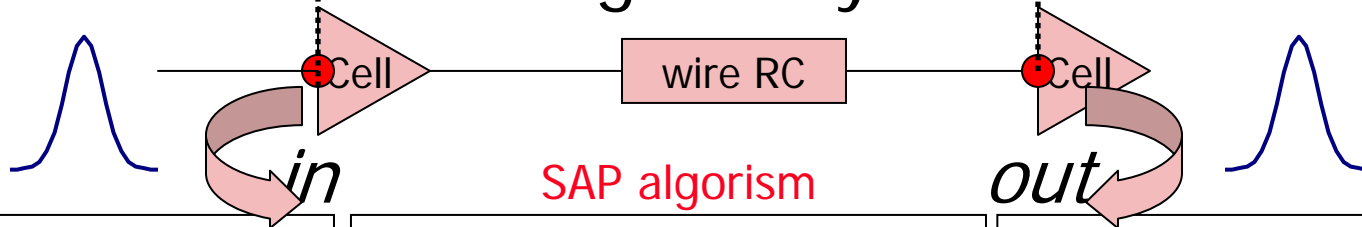
- The fast nonlinear statistical timing calculation using SAP

Index_slew(s1,s2,s3,...)
 Index_cap(c1,c2,c3,...)
 Delay: mean, sigma
 Slew: mean, sigma
 Delay & Slew correlation: gamma

Index_slew(s1,s2,s3,...)
 Index_cap(c1,c2,c3,...)
 Tr1/Parameter1: mean, sensitivity
 Tr1/Parameter2: mean, sensitivity

AT: Arrival Time
 SL: Slew Rate
 γ : correlation AT&SL

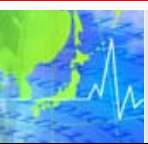
Stage delay



AT_in: mean, sigma
SL_in: mean, sigma
 $\gamma(AT_in, SL_in)$

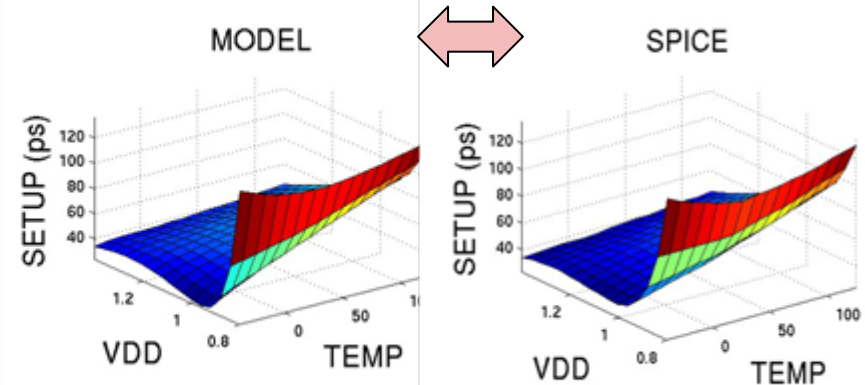
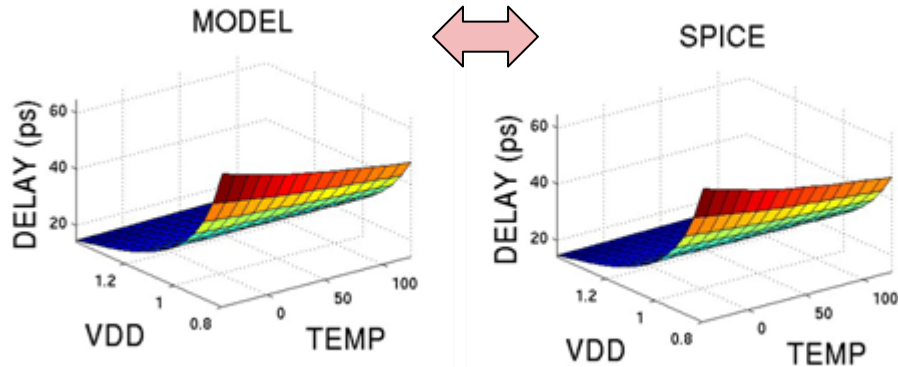
Delay_out
 $= \text{SAP1}(AT_in, SL_in, Var_cell, Var_wire)$
Slew_out
 $= \text{SAP2}(AT_in, SL_in, Var_cell, Var_wire)$

AT_out: mean, sigma
SL_out: mean, sigma
 $\gamma(AT_out, SL_out)$

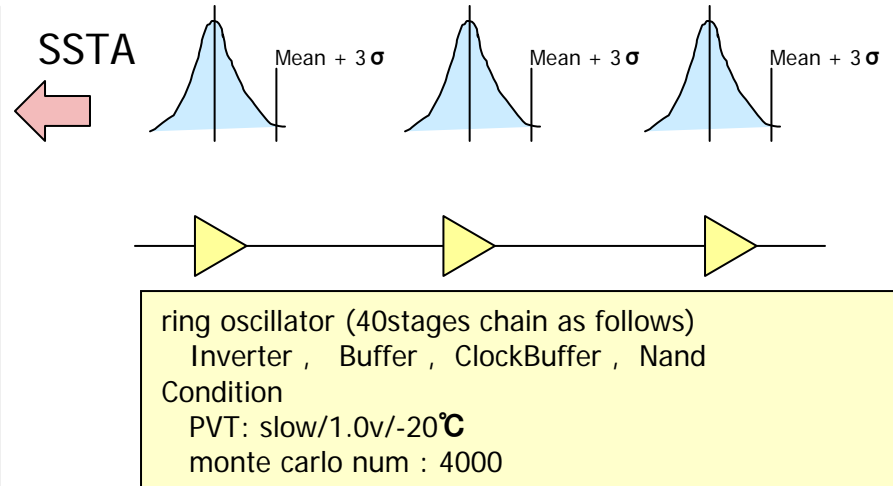
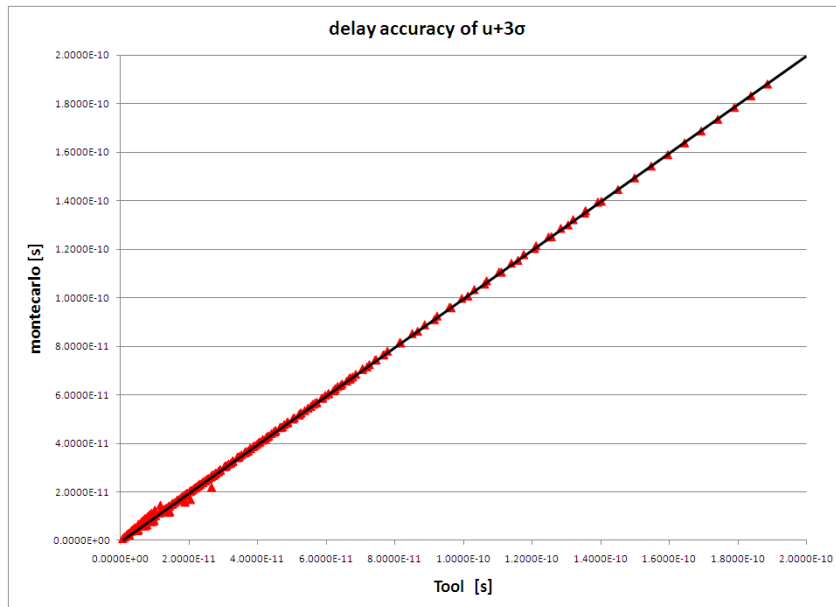


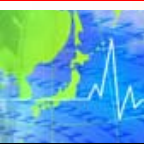
Experiment

Library Accuracy : Within 3% difference v.s. SPICE



Tool Accuracy : Within 5% v.s. spice

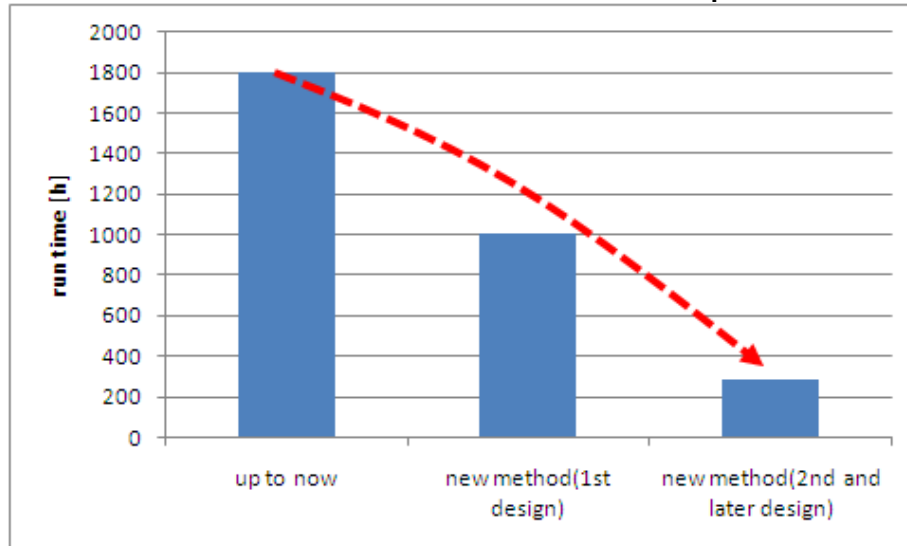




Experiment

Result (RunTime)

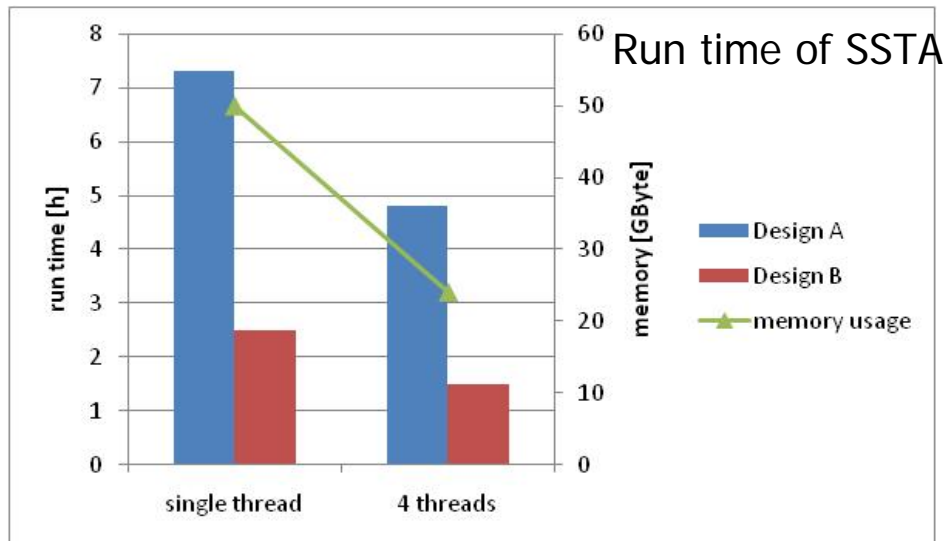
Run time of characterization@30cpu



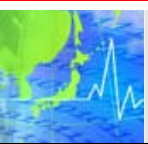
Left figure shows runtime trend of characterization in case of 5 parameters / 1000 cells per 3 vth / 4 corners.

Simulation for variation needed for 1st design, but not for 2nd or later designs since it can be appropriated.

So runtime can be improved to $1/7$.



Run time of full chip statistical analysis is about 5 hours using 4 threads for a 35Mgate ASIC design.

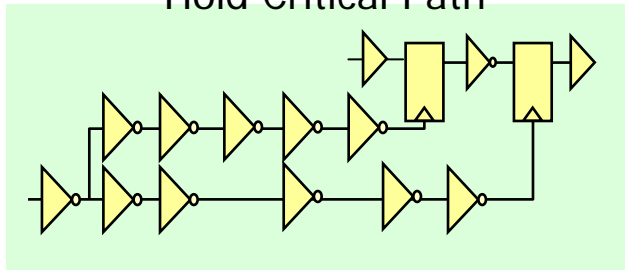


Design Experiments

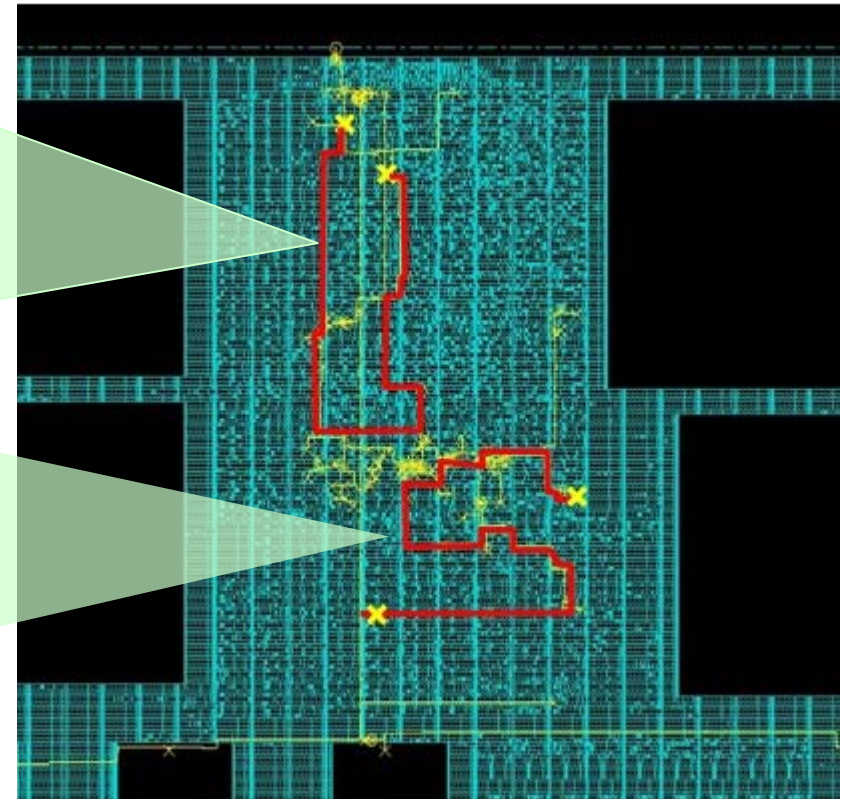
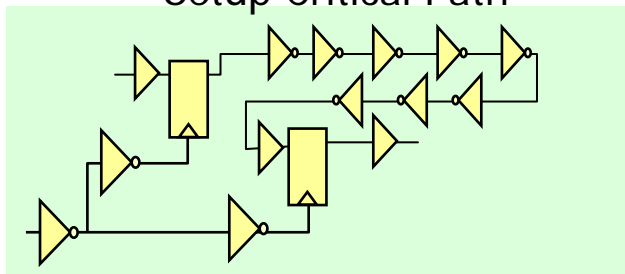
■ ASIC Design

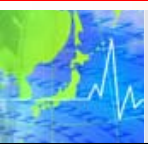
	Design A	Design B
Technology node	40nm (Vth Low/Std/High)	40nm (Vth Low/Std/High)
Layer	9	8
Logic Size	Logic: 35MGate (FF: 150M)	Logic: 15MGate (FF: 65M)
Frequency	180MHz ~ 350MHz	100MHz ~ 380MHz

Hold Critical Path



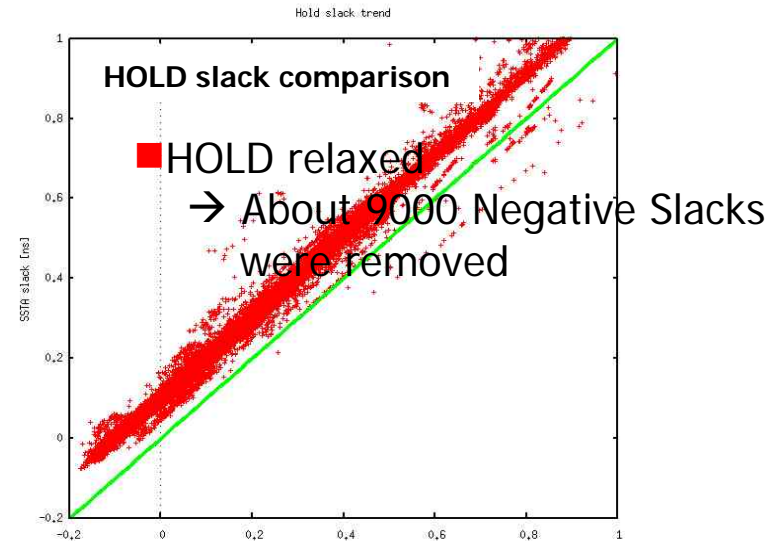
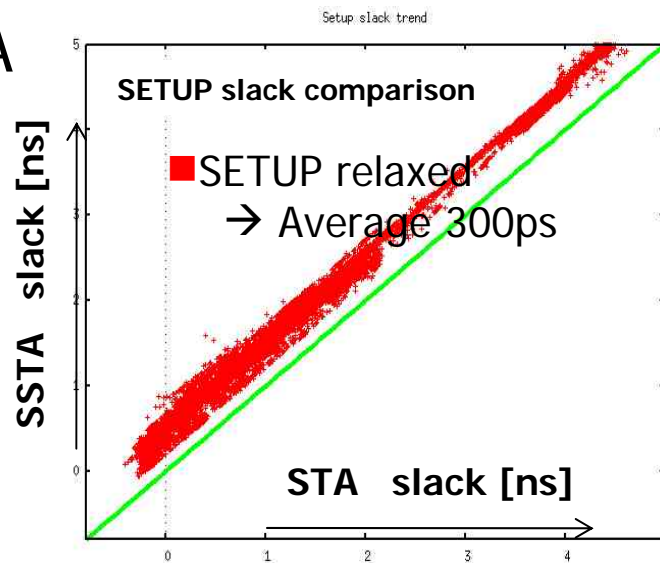
Setup Critical Path



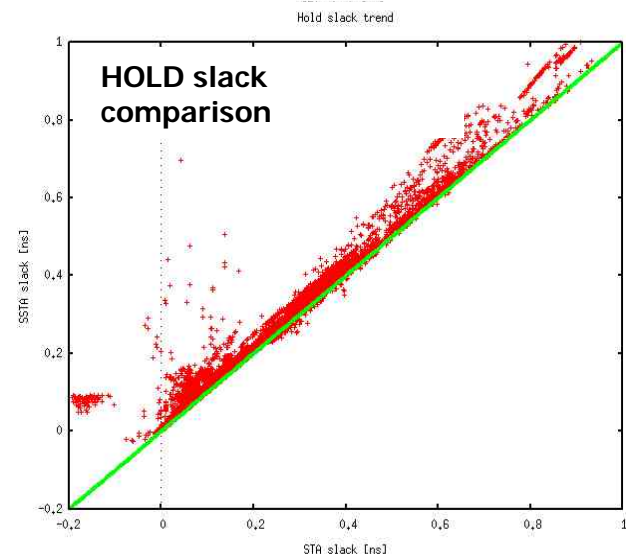
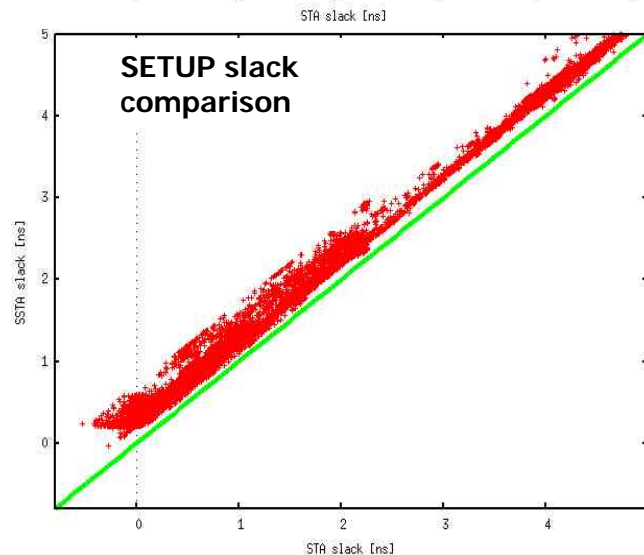


Design Experiments

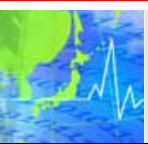
Design A



Design B



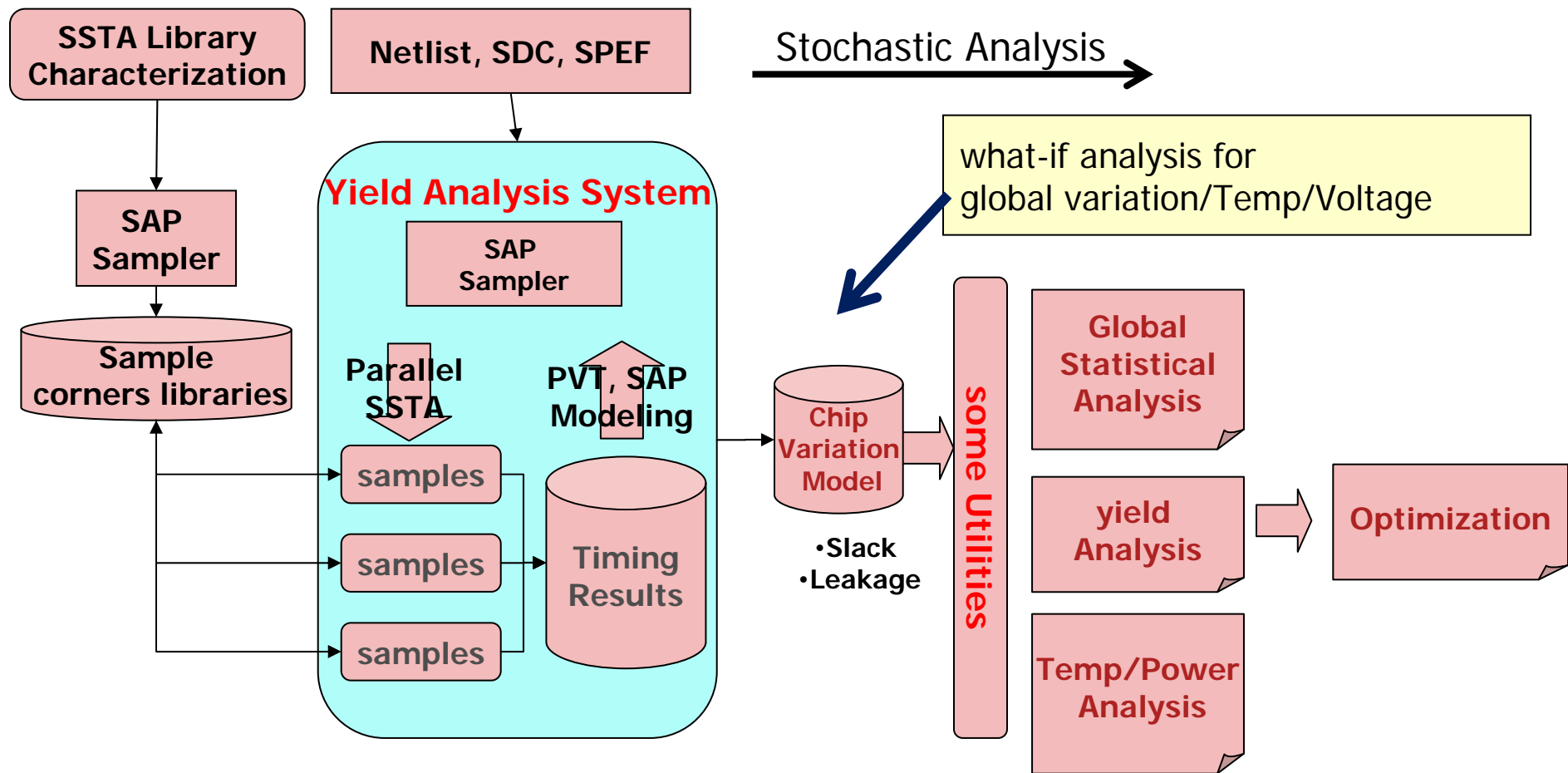
As a result , we reduced design TAT 1 week!! Cost reduction on both engineering and silicon



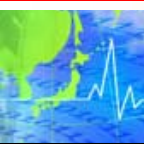
Future Plan

■ Full Chip Stochastic Analysis of Global Variation

Fast “what-if” analysis to target speed/power and timing yield



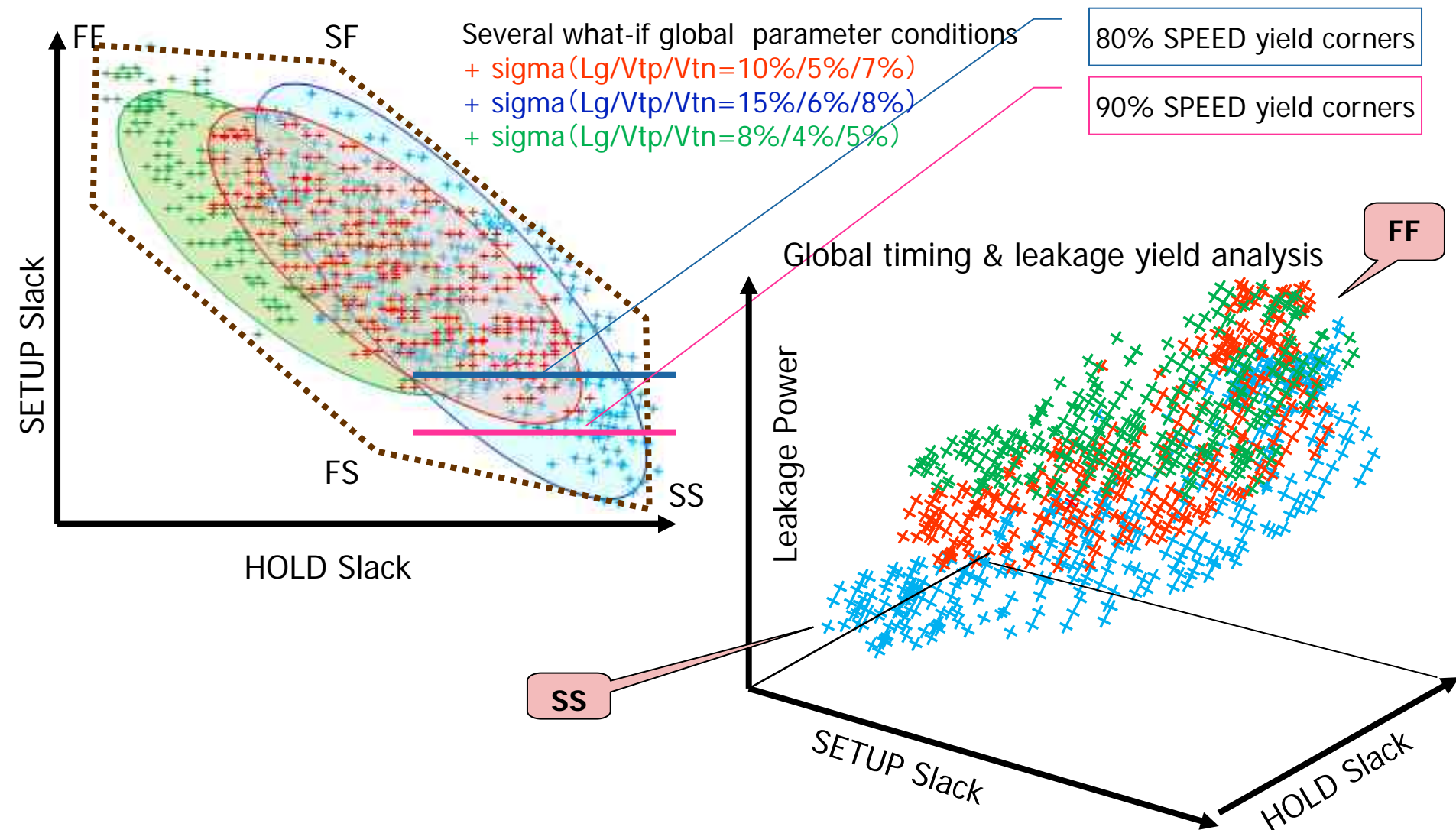
Pre-Silicon Analysis

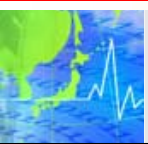


Future Plan

Timing and Leakage Yield analysis for global variation

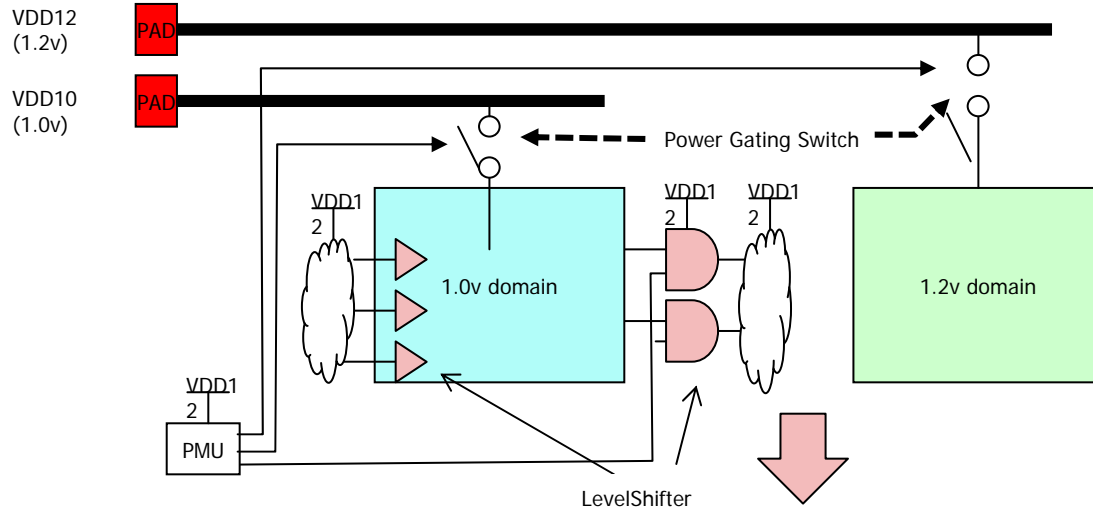
Chip global timing yield analysis





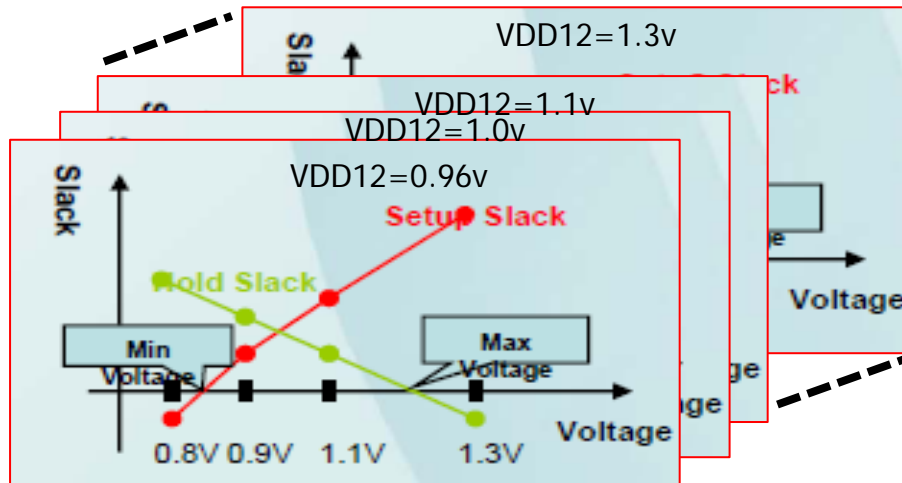
Future Plan

Timing Yield analysis for multi voltage

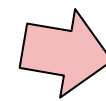


Technology node	65nm (Vth Low/Std/High)
Layer	8
Chip Size	10mm \square
Logic Size	Logic: 20MGate
Frequency	100MHz ~ 200MHz

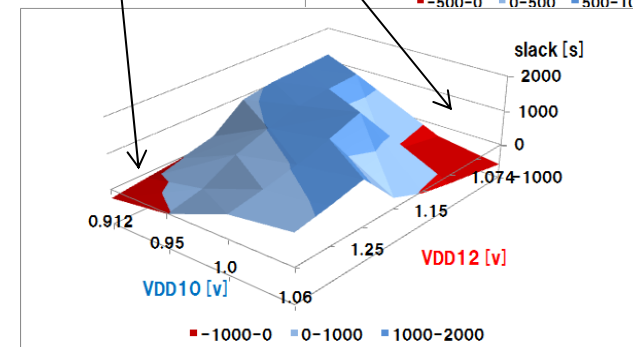
What-if analysis for adaptive voltage with SSTA



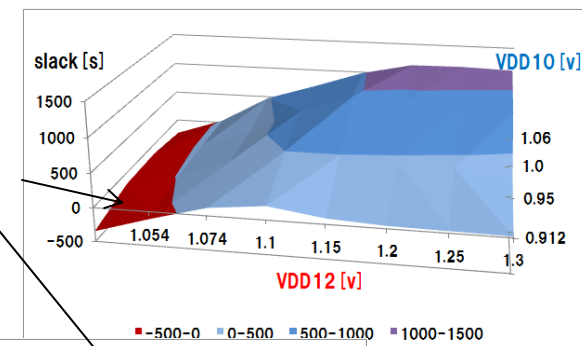
Red block:
Yield loss area

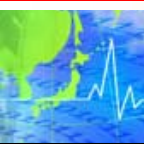


HOLD



SETUP





Conclusion

- What is the bottleneck to use of SSTA on 40nm/28nm ASIC designs?
 - ➔ Cost performance. We had to break down and re-engineer this problem to achieve practical SSTA use for 40nm/28nm ASIC designs.
- Is there an available SSTA tool for huge ASIC designs?
 - ➔ Yes, our SSTA flow is ready to be applied to huge design; we have been using it on our 40nm designs.
- Does SSTA provide advantages beyond relaxing timing?
 - ➔ Yes, SSTA can also be used for yield analysis and design optimization .
- What are the innovations and future plans?
 - ➔ We will apply SSTA to timing yield analysis for design optimization.