

## **An Efficient Method of Timing Generation for Analog IP in Mixed Signal Integration**

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One popular design trend of current semiconductor products is to make the electronic devices more user friendly, for example, through the use of a touch panel. As a result, more analog blocks are being integrated into the chips. Therefore, how to ease the integration of analog and digital blocks with efficiency and correctness has become an important issue. From practical experiences, the interface between analog and digital blocks, where subtle timing and functional bugs are prone to happen, is the main focus of verification. Traditionally, a simulation approach is applied to tackle this issue. Since analog blocks are usually represented in SPICE level while digital parts are in either RTL (Register Transfer Level) or gate level netlists, the analog-digital co-simulation methodology will be needed with vast amount of simulation patterns being applied hopefully to cover all possible scenarios. For a complicated design, weeks of simulation time is not uncommon even with the most advanced co-simulation tool. For example, to verify the data coherence for a PCIE-Gen2 design with internal PLL and calibration mechanism, it could take hundreds of hours in simulation just to get the clock stable before reaching the desired verification scheme!

Another approach is to use static timing analysis (STA) for the assurance of timing and analog-digital co-simulation for the verification of function of the interface. In this flow, timing models of analog blocks will be required to perform STA. However, due to the lack of an automatic tool, designers typically have to manually capture the timing models through extensive characterization steps. As technology node advances while process variation worsens, more and more corners and process variations must be considered in the generation of valid timing models. The terrible characterization time and huge manual effort needed to create such timing models have become the bottleneck that impacts the usage of STA flow; especially when post-layout netlist is preferred in order to have more accurate timing information.

In this paper, we present a method to speed up timing characterization and automate timing model generation for analog blocks through circuit reduction technology without degradation in accuracy. This methodology supports the characterization and generation of setup and hold time constraints, path delays of internal clock to output pins, and the generated clock information if necessary. In most analog designs, typically only 10% or lower of the entire design is related to the interface with digital blocks, either sending or receiving data. Furthermore, the timing model of an analog design consists of independent timing constraints and delay paths. Therefore, if we can only work with the parts of the design that relate to the needed interface timing constraints or delay paths, great efficiency in timing characterization can be achieved without sacrificing accuracy.

In the proposed method, each timing constraint or delay path will be dealt with individually. First, path-oriented circuit reduction technique is applied so minimum circuit is found through fan-in and fan-out cone search. Next, the characterization patterns needed to sensitize this minimum circuit will be generated using structure analysis. Meanwhile, the capacitive coupling of the minimum circuit should be carefully preserved. Then, the transistor level simulator, HSPICE, will be used to measure the path

delays or timing constraints involved. Since each timing constraint and delay path is independent of each other, we can speedup the transistor level simulation using computing farm by submitting all of the simulation jobs at once. When the characterization of all timing constraints and paths is completed, the timing model of the analog design is generated. With this method, we are able to provide much more complete and accurate timing models of analog designs in much less time. The benefit is even greater where accurate timing information under variant process/voltage/temperature and loading conditions are needed – which quickly becomes norm in sub-100nm designs.

The proposed method has been successfully applied to several cases including DAC (Digital-to-Analog Converter) and Ethernet PHY. The experimental result is shown in Table 1 where DAC1 and DAC2 are in different architecture. For DAC2 case, HSPICE is not able to finish within 4 hours while it only takes 1.5 minute for the extracted netlist. Even with the fast spice simulator, it still takes about 1 hour to simulate the full netlist shown in the last column of table 1. For all cases, more than 30X of speedup in simulation time has been observed with at most 3% loss in accuracy. In practical applications, the minor loss in accuracy can be offset by adding a small margin in the generated timing model for safeguard purpose. In table 2, the overall timing model generation time is presented. For all cases, we are able to generate the timing model within 7 hours which could be less if the computing farm was dedicated for the timing characterization only.

	Original netlist			Extracted netlist		
	number of devices	simulation run time	delay (s)	number of devices	simulation run time	delay (s)
Ethernet PHY	166K	70 minutes	229p	2.6K	1.5 minutes	222p
DAC1	67K	30 minutes	274p	1K	1 minute	270p
DAC2	256K	NA	NA	1K	1.5 minute	440p
DAC2	256K	1 hour *	488p	1K	30seconds*	486p

**Table 1. Run time and delay comparison for a single timing arc between the original netlist and the extracted netlist. \* The simulation is conducted using fast spice simulator.**

	Number of timing arcs/constraints	Number of process/voltage/temperature/input slew variations	Run time
Ethernet PHY	12	243	3.5 hours
DAC1	10	243	1.5 hours
DAC2	24	243	7 hours

**Table 2. The timing model generation time.**

## Reference

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