

# A Practical Statistical Timing Characterization System in 40nm

---

---

Sam C. Lo ([sam.lo@oracle.com](mailto:sam.lo@oracle.com))

Sridhar Premkumar, Ray Y. Shr, Aaron Barker, Ebrahim Khalily

June 16, 2010

Processor Tools Group – Microelectronics,  
Oracle Corporation, Santa Clara, CA 95054, USA.

# Posters Outline

---

- Introduction to Statistical Timing Characterization
- Approaches Overview
- Statistical SPICE Environment
- Models for Library Cells
- High Throughput Characterization System
- Full 40nm Statistical Library Characterization
- Summary

# Introduction to Statistical Timing Characterization

---

- Statistical Static Timing Analysis (SSTA)
  - ⊙ Becoming mainstream since 65nm technology
  - ⊙ Foundry support with statistical SPICE models
- SSTA Benefits
  - ⊙ Reduce design uncertainty
  - ⊙ Reduce pessimism
- Library Characterization
  - ⊙ Covers more process space
  - ⊙ Requires a lot more simulation
  - ⊙ High characterization runtime cost
  - ⊙ Efficient solution needed

# Approaches Overview

---

- Existing Approaches

- ⊙ Characterize less data with smarter interpolation algorithm
- ⊙ Carefully selection on slew and load index, with less points
- ⊙ Both risk accuracy by improving runtime
- ⊙ Not particular for sensitive circuits such sequential cells

- Our Statistical Characterization Approach

- ⊙ Maintain accuracy. Maximize hardware usage. Easy setup
- ⊙ A Characterization system designed for production
- ⊙ Speed-up simulation with pre-compiled model interface
- ⊙ Seamless integration between statistical SPICE simulation
- ⊙ Intelligent job scheduler to use all possible hardware resource

# Statistical SPICE environment

---

- Binary SPICE Model Interface

- ⊙ SPICE simulation dominates SSTA characterization time
- ⊙ Proximity effect modeling further increases runtime
- ⊙ Pre-compiled binary model interface helps SPICE speed-up
- ⊙ 2~3X speed-up vs. traditional macro models

Cell timing arc	Nand delay	Flop delay	Flop setup
Speed-up (X)	2.3	2.8	2.1

- Statistical simulation environment

- ⊙ Automatic parameter seeds selection and range definition
- ⊙ Advanced statistical sampling methods
- ⊙ ~50 simulation samples per slew and loads

# Models for Standard Cells

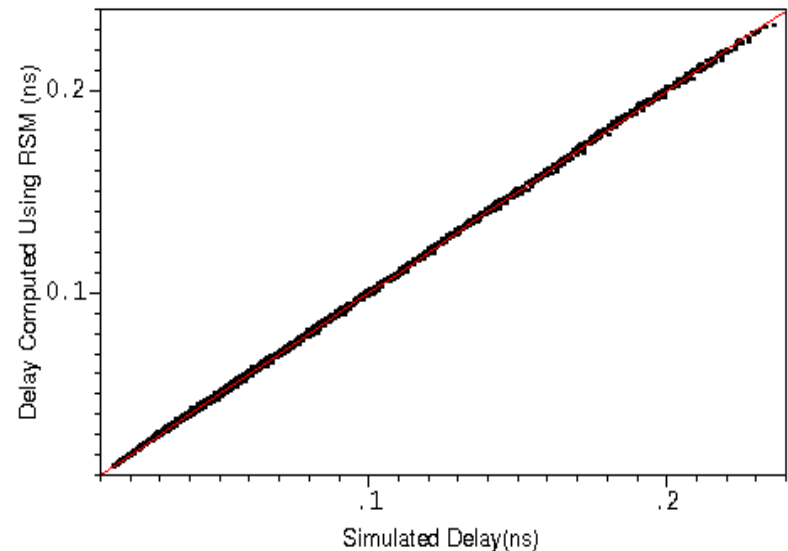
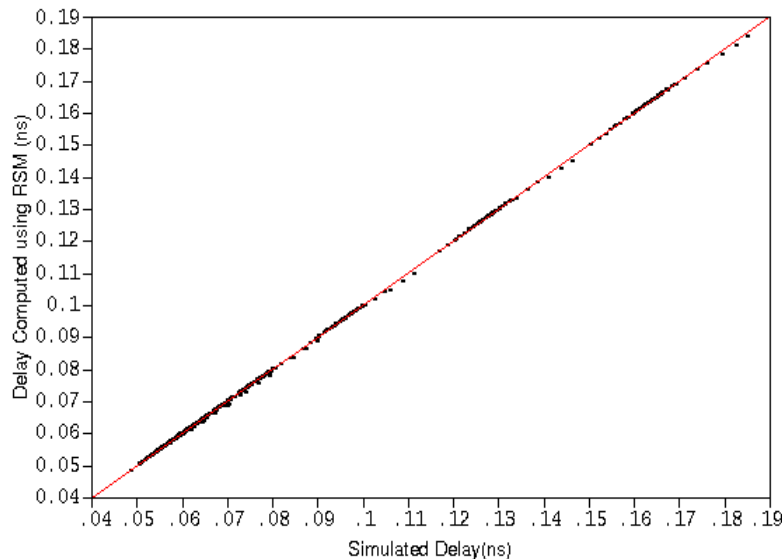
---

- Arc delays, output slew, and input capacitance are modeled
- Setup-time and Hold-time are modeled
- An example for the propagation delay is shown here and includes:
  - ⊙ Nominal delay variation as a function of input slew tx and output load cl.
  - ⊙ Global process variation terms  $X_n$  as functions of input slew tx and output load cl.
  - ⊙ Standard deviation R of local process parameters as function of input slew tx and output load cl.

$$\text{delay}(tx, cl, X_1, X_2, \dots, X_n, R) = d_0(tx, cl) + \sum_i^n a_i(tx, cl) \cdot X_i + b(tx, cl) \cdot R$$

# Verifying Model Accuracy

- Models for clock-q and propagation delay is evaluated at various slew and load values for sample flop and buffer standard cell respectively.
- The computed delay is then plotted against the SPICE simulated delay for verifying accuracy of models as shown in the plots below.



# High Throughput Characterization System

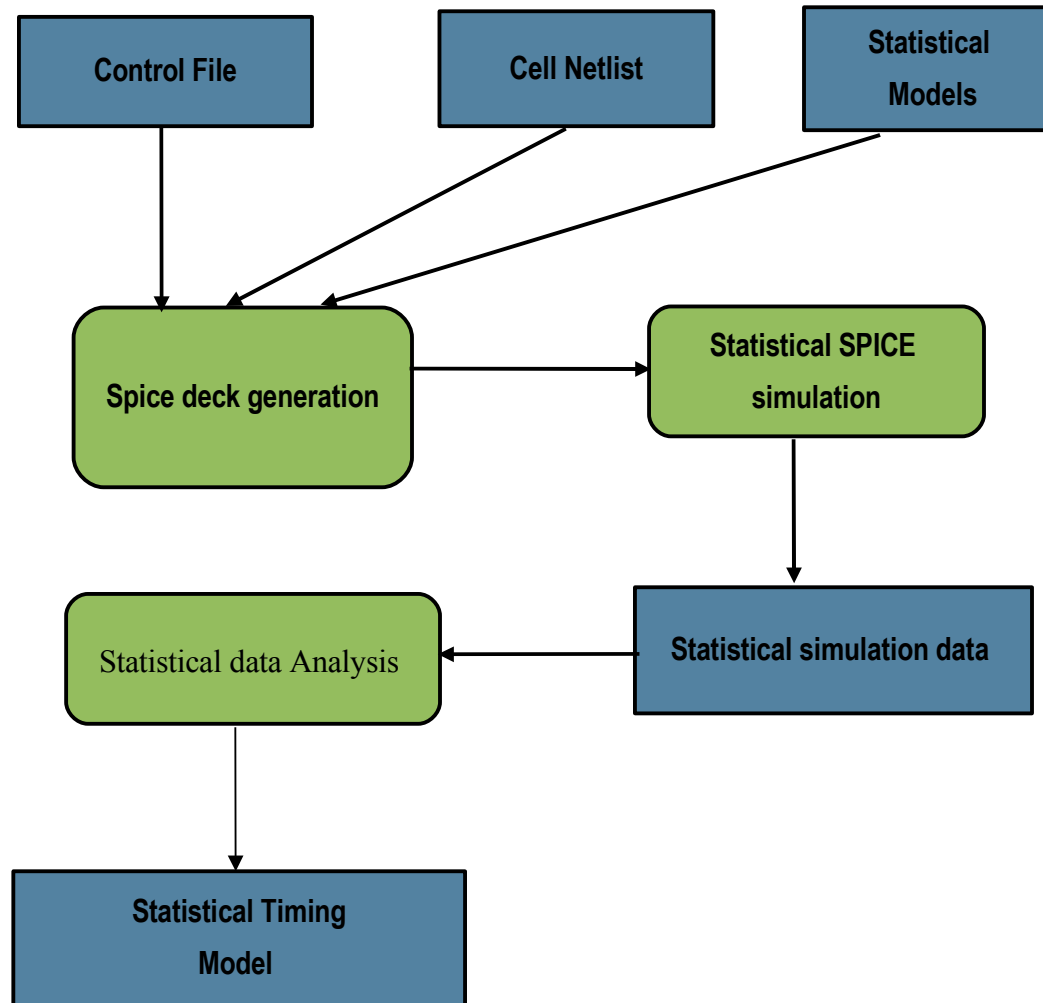
---

- Statistical timing characterization for a cell requires orders-of-magnitude more simulations than corner-based cell characterization. Therefore, an enhanced methodology in characterization flow is needed to reduce the overall characterization run time.
- Corner-based library data can be used to reduce the over-all statistical characterization run-time. Experience shows that this type of adaptive technique reduces the over-all run-time by about 30%.
- Statistical timing characterizations for Delay, Input Capacitance, Setup/Hold time are independent of each other, So these are characterized in parallel using multi-threading and multi-processing modes.
- Advanced job scheduler is used to maximize the hardware resource utilization by dispatching the SPICE jobs in parallel for all cells in the library to various high performance machines for fast simulation thus providing fast turn-around time for complete statistical library.



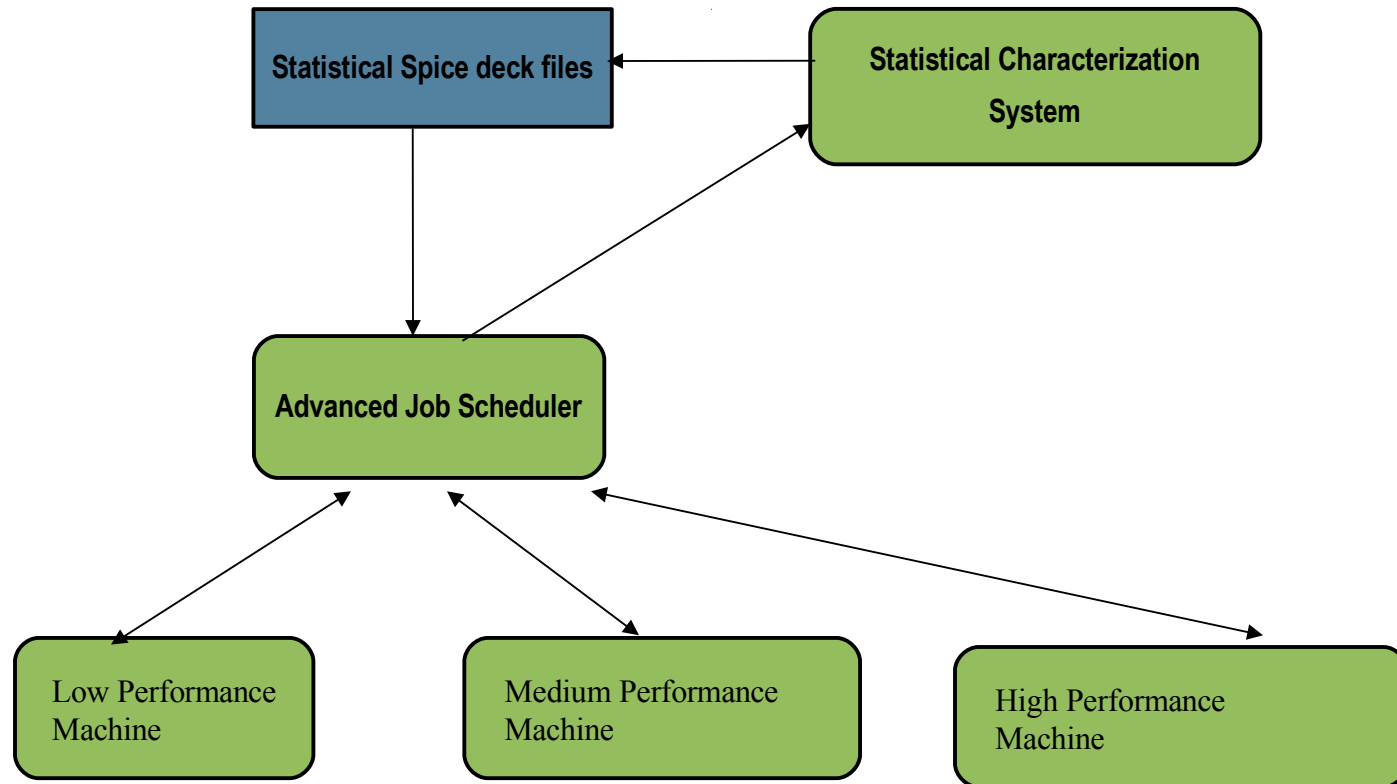
# Statistical Characterization System Flow

---



# Efficient Parallel Characterization System Flow

---



# Full 40nm Statistical Library Characterization

- Completed full 40nm statistical library characterization
  - ⊙ Over 1000 cells, including high-order mux, sequential cells
  - ⊙ No additional setup required. Finished within one week.
- Library QA for every cells
  - ⊙ Compare delta and variation
  - ⊙ Make sure within defined range
- Observation
  - ⊙ Good SSTA correlation with SPICE
  - ⊙ Can adopt less number of slew and load
  - ⊙ MUX cells dominate run-time
  - ⊙ Can further reduce runtime
  - ⊙ Without accuracy loss

Timing Arc	Deterministic	Statistical	
		Delta	Variation
in0_cap	0.629	0.015	0.998
in1_cap	0.674	0.037	0.997
in2cap	0.664	0.632	0.996
in0_delay_fall	10.110	0.114	0.985
in1_delay_fall	11.220	0.091	0.986
in2_delay_fall	12.940	0.101	0.987

Group	Combo1	Combo2	Mux	Seq
Runtime %	27.6	12.1	<b>50.2</b>	10.1
Cell count %	48.9	18.7	23.9	8.5

# Summary

---

- SSTA can reduce design uncertainty and pessimism
  - ⊙ Statistical characterization high runtime cost is a concern
- Our characterization system focuses on practical aspects
  - ⊙ Improve SPICE runtime using pre-compiled model interface
  - ⊙ Maximize usage of all possible hardware resource
  - ⊙ No accuracy Loss. High throughput
- Completed characterization on full 40nm library
  - ⊙ Over 1000 cells for high-end CPU design
  - ⊙ Library used for statistical STA analysis on full chip
  - ⊙ SSTA results correlate well with SPICE simulation