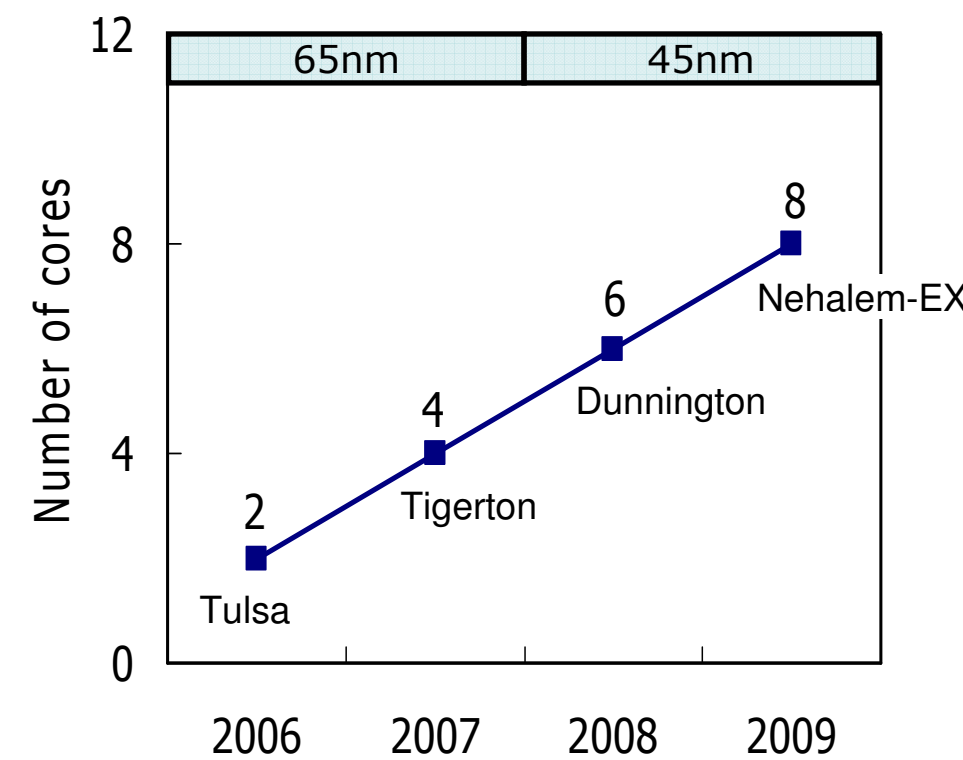


Superblock: A Method for Synthesizing Large High Performance Designs without Hierarchy Limits

Murali Seshadri, Chris Mabee, Madhur Maheshwari, Raj Varada
Intel Corporation, Santa Clara, CA

Design Efficiency

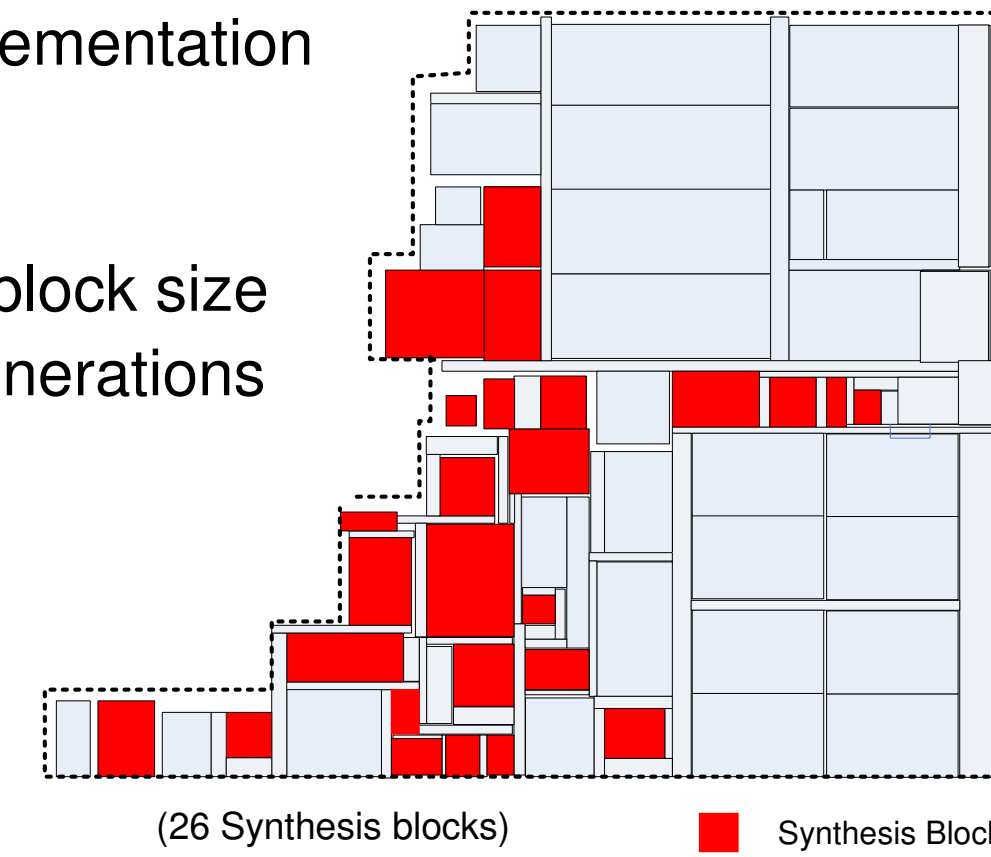
Design Efficiency
lags tool /
infrastructure
capabilities



Synthesis Blocks in Processors

Microprocessor Implementation

- Hierarchical RTL implementation
- Smaller synthesis block size
- Reuse between generations (legacy)



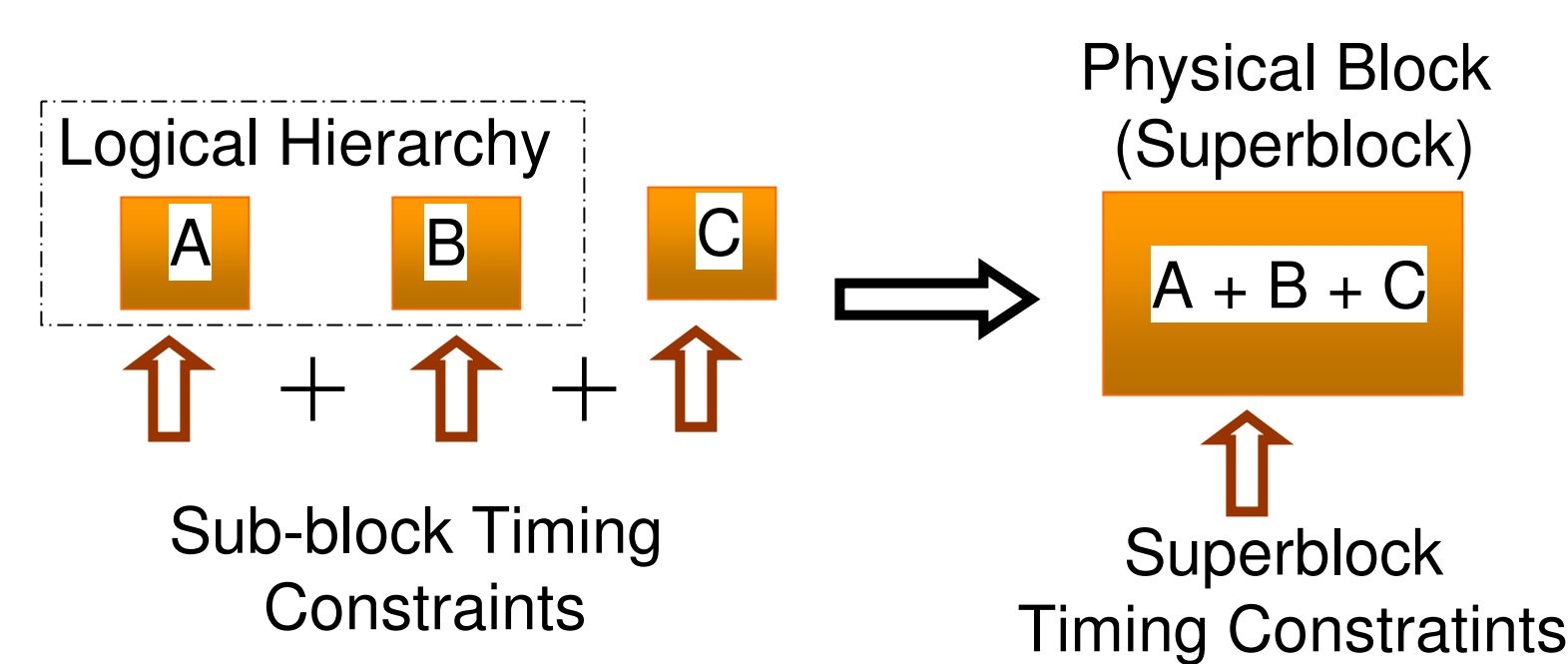
Better Design Efficiency?

- Better design efficiency through larger blocks?
- How to transition from small blocks to larger block with legacy RTL?
- How to define the interfaces of the larger block?
- How to achieve good timing constraints for the larger block?

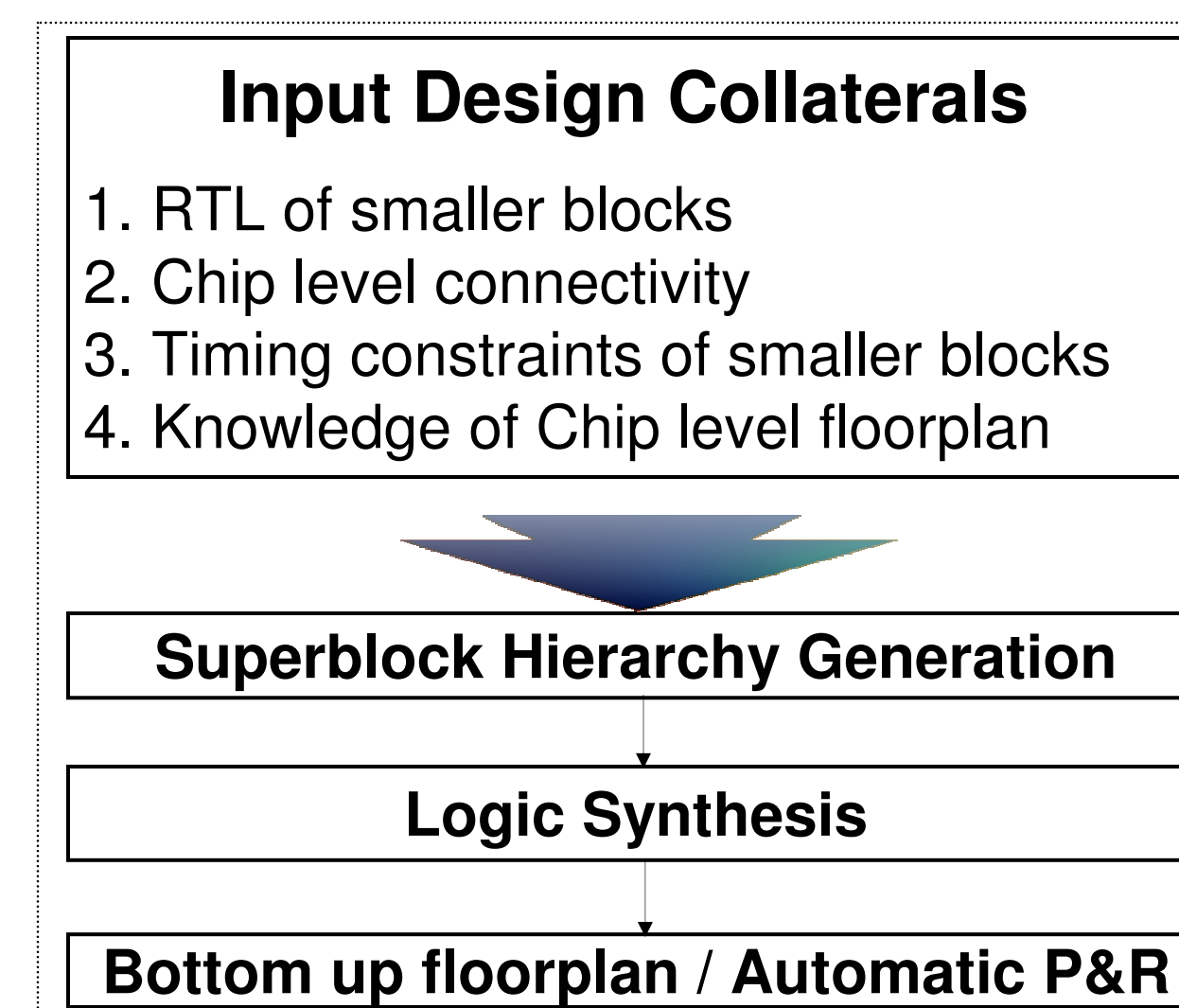
We present a synthesis methodology to use legacy RTL yet achieve higher design efficiency

Solution: Superblock...

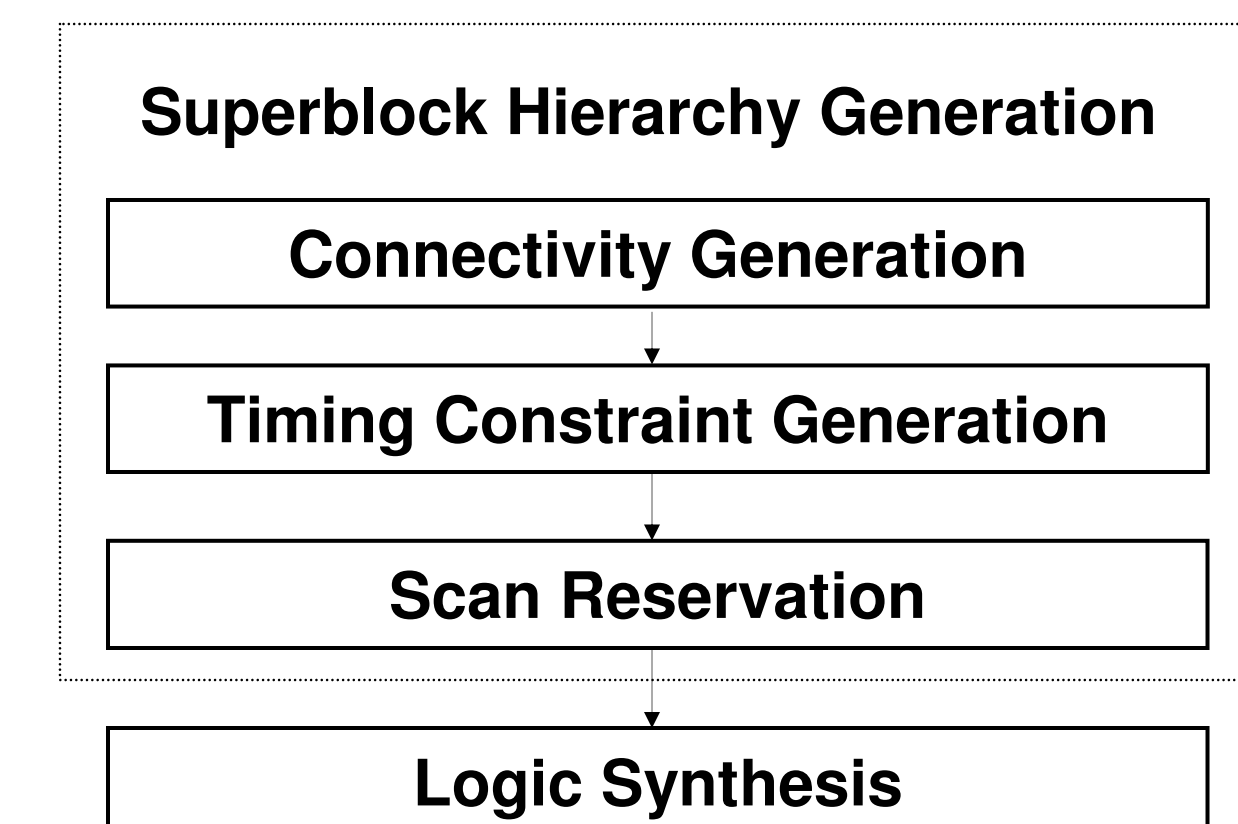
- Create a large block – “Superblock”
 - Maintaining the same RTL structure
 - Using the sub-block constraints



Superblock Flow

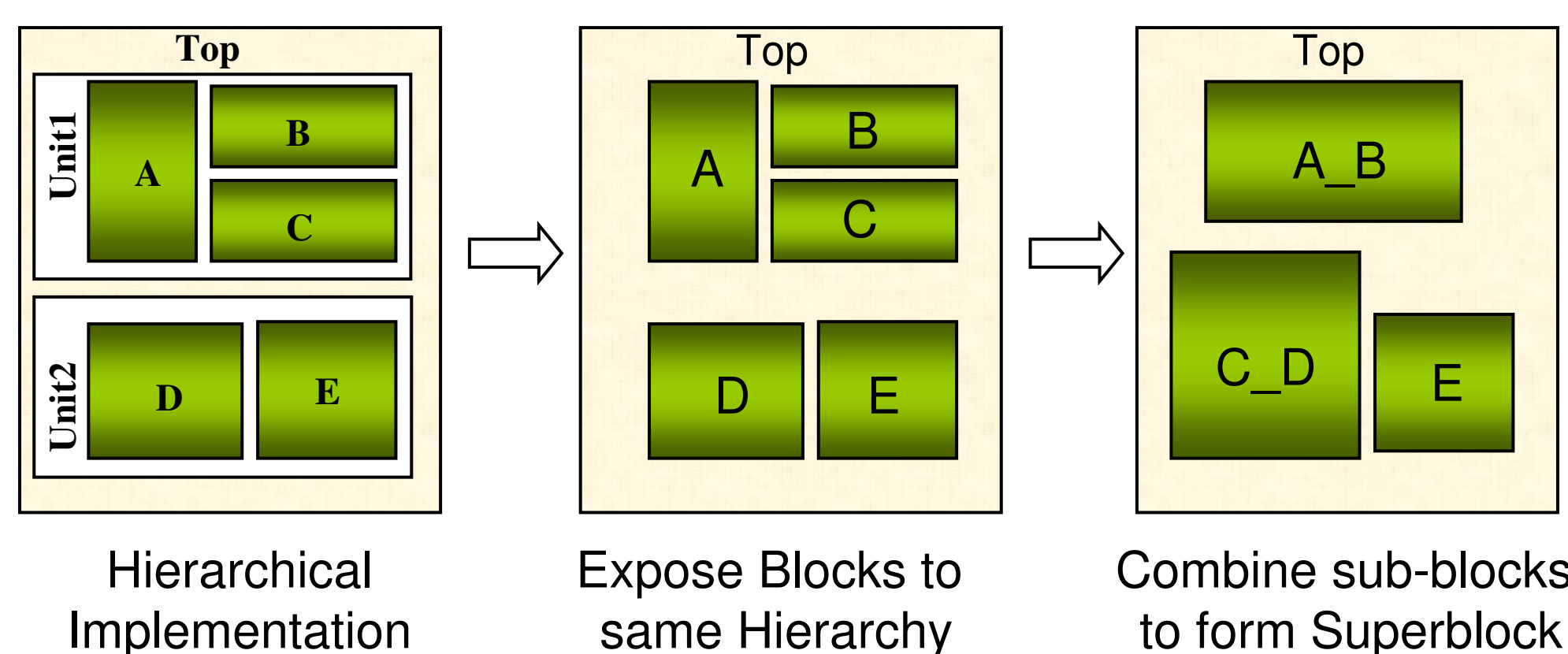


Superblock Flow Internals

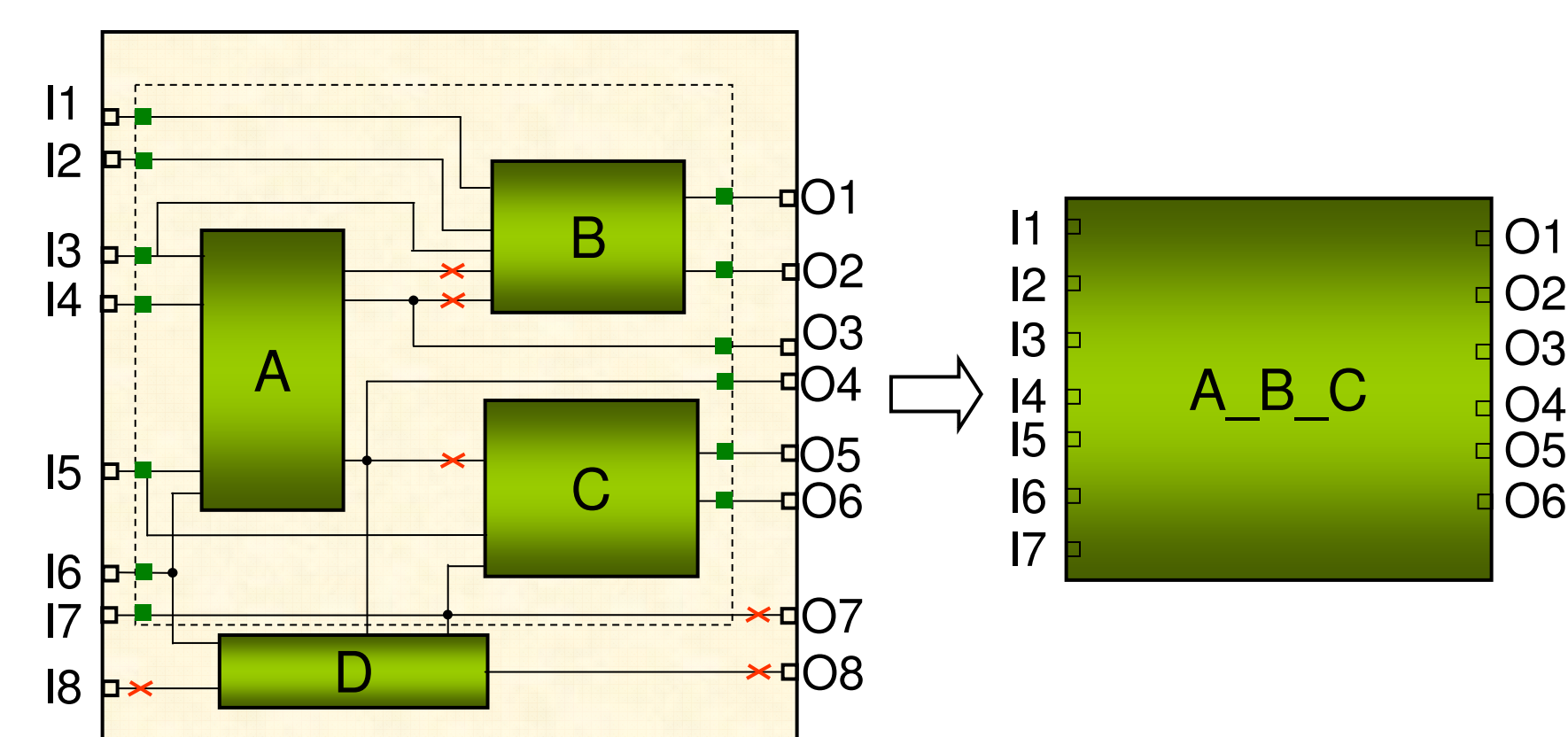


Mix of tool capability and automation used to generate the Superblock hierarchy

Connectivity Generation



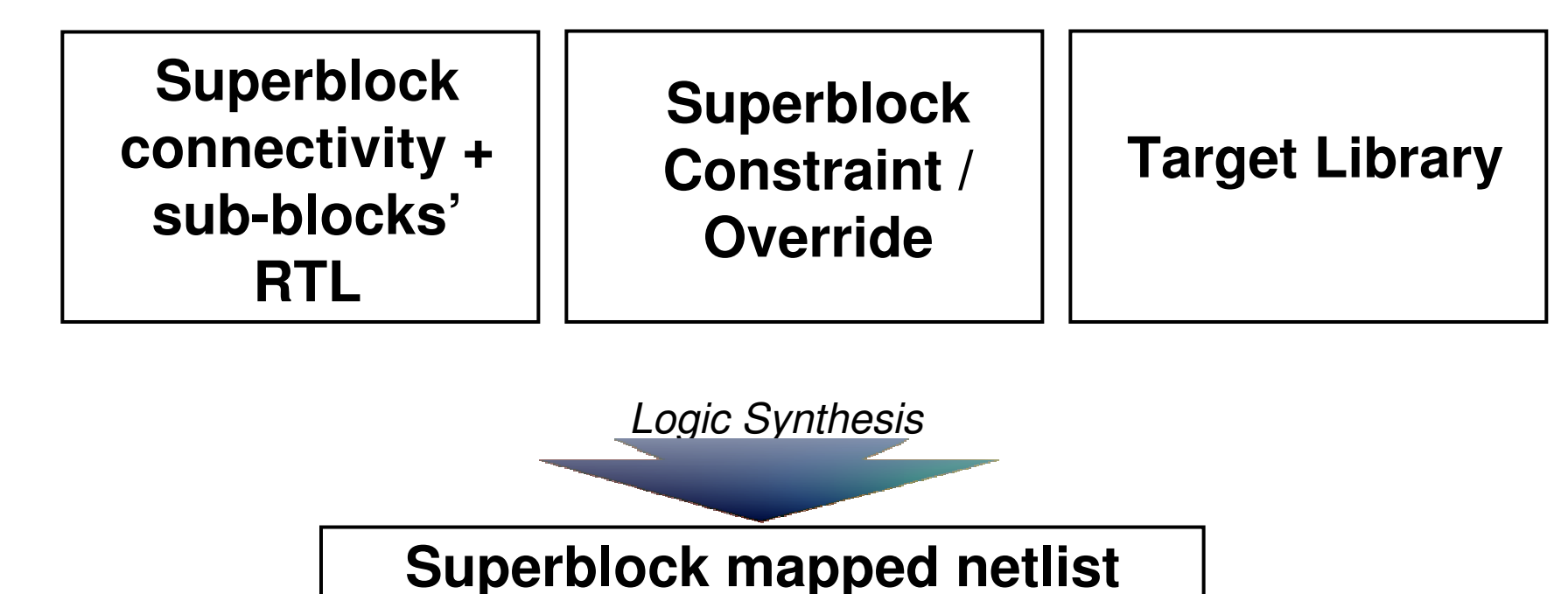
Timing Constraint Generation



Superblock Interface is subset of sub-blocks' ports
Worst timing (of the sub-blocks) is picked

Scan Reservation & Logic Synthesis

Scan Reservation implemented to reserve area



Results – Grouping 1

	SuperBlock1		
	Cumulative	Superblock	Ratio
Number of logical cells	38883	38633	99.4%
Number of flops:	4518	4516	100.0%
Number of latches:	1623	1623	100.0%
Number of Sequentials	6141	6139	100.0%
Total Z (cm)	39.77	25.71	64.6%
WNS Internal (ps)	0	9	
WNS External (ps)	0	7	

Superblock flow yields same cell count with significant Z reduction

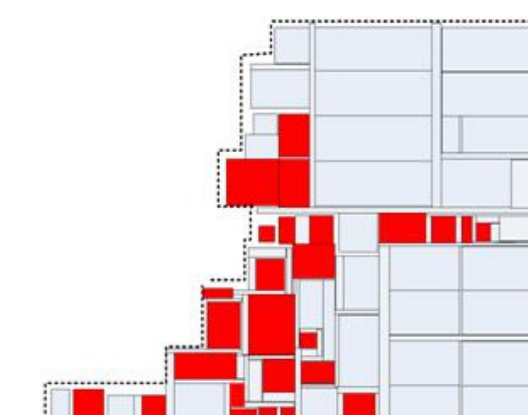


Results – Grouping 2

	SuperBlock2		
	Cumulative	Superblock	Ratio
Number of logical cells	71083	68249	96.0%
Number of flops:	9581	9581	100.0%
Number of latches:	4829	4826	99.9%
Number of Sequentials	14410	14407	100.0%
Total Z (cm)	40.56	39.77	98.1%
WNS Internal (ps)	0	14	
WNS External (ps)	0	51	

Superblock flow yields lesser cell count and Z

All the synthesizable logic in ONE block; No RTL or collateral effort



Conclusions

- Multi-core computing enables high thru-put CAD
- Superblock flow enables big block design with legacy RTL optimized for small block synthesis
- Superblock flow builds constraints automatically from constituent blocks
- Results show equal or better results for superblock flow for big blocks with no RTL effort
- Design Efficiency increase!