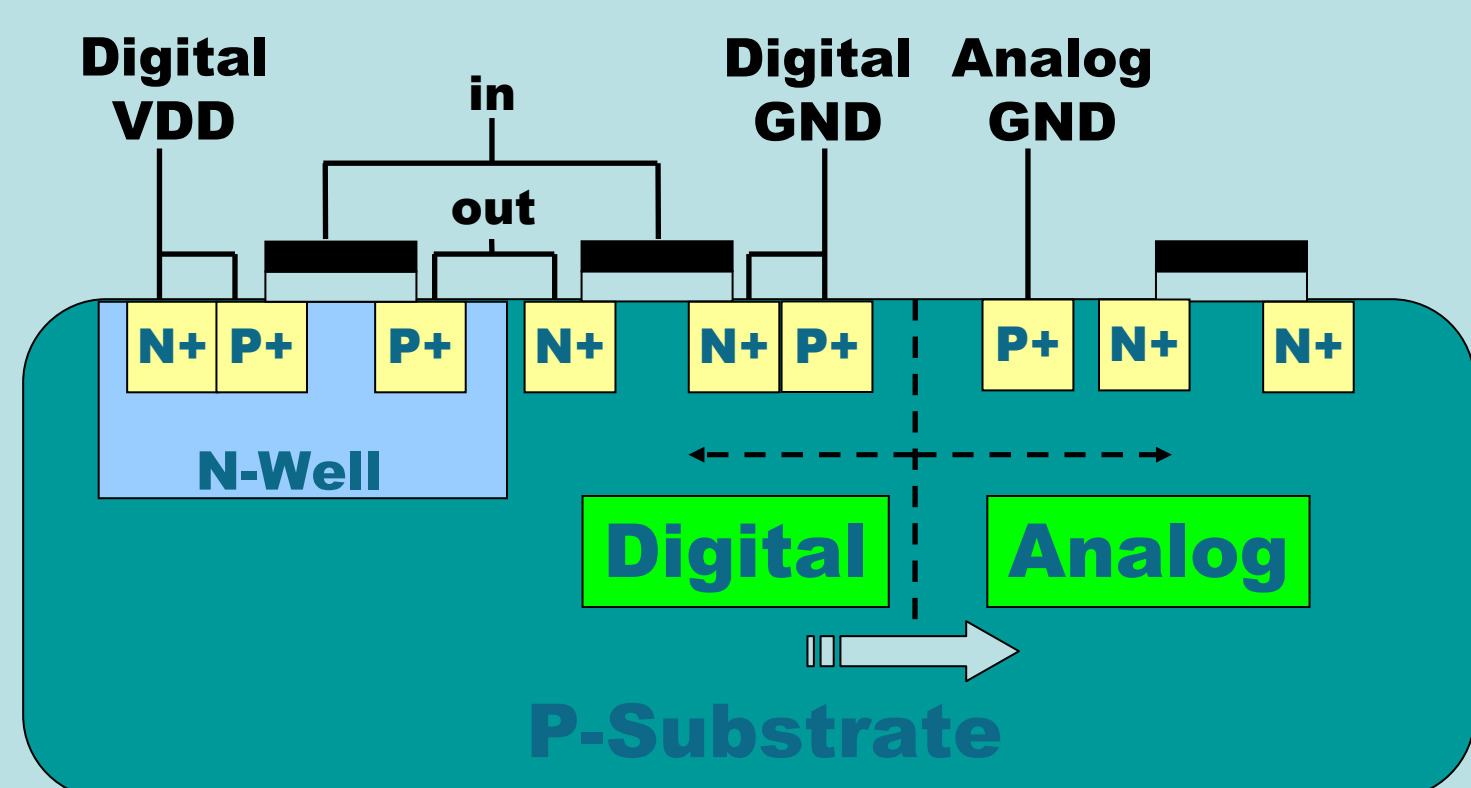


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BACKGROUND

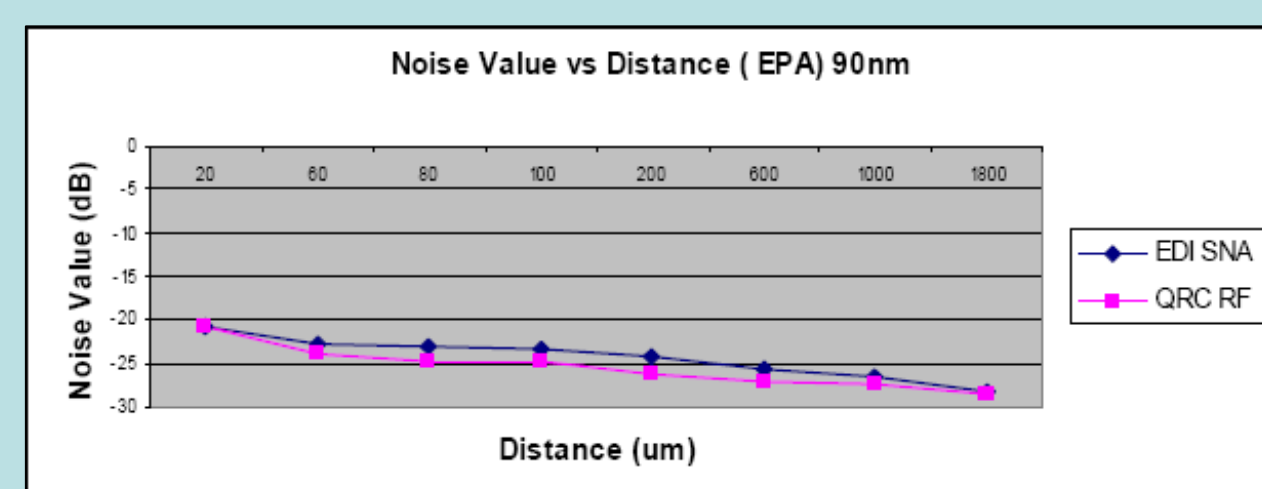
In mixed signal SoC, digital switching noise could be coupled to analog circuit through common substrate and cause signal integrity issue.



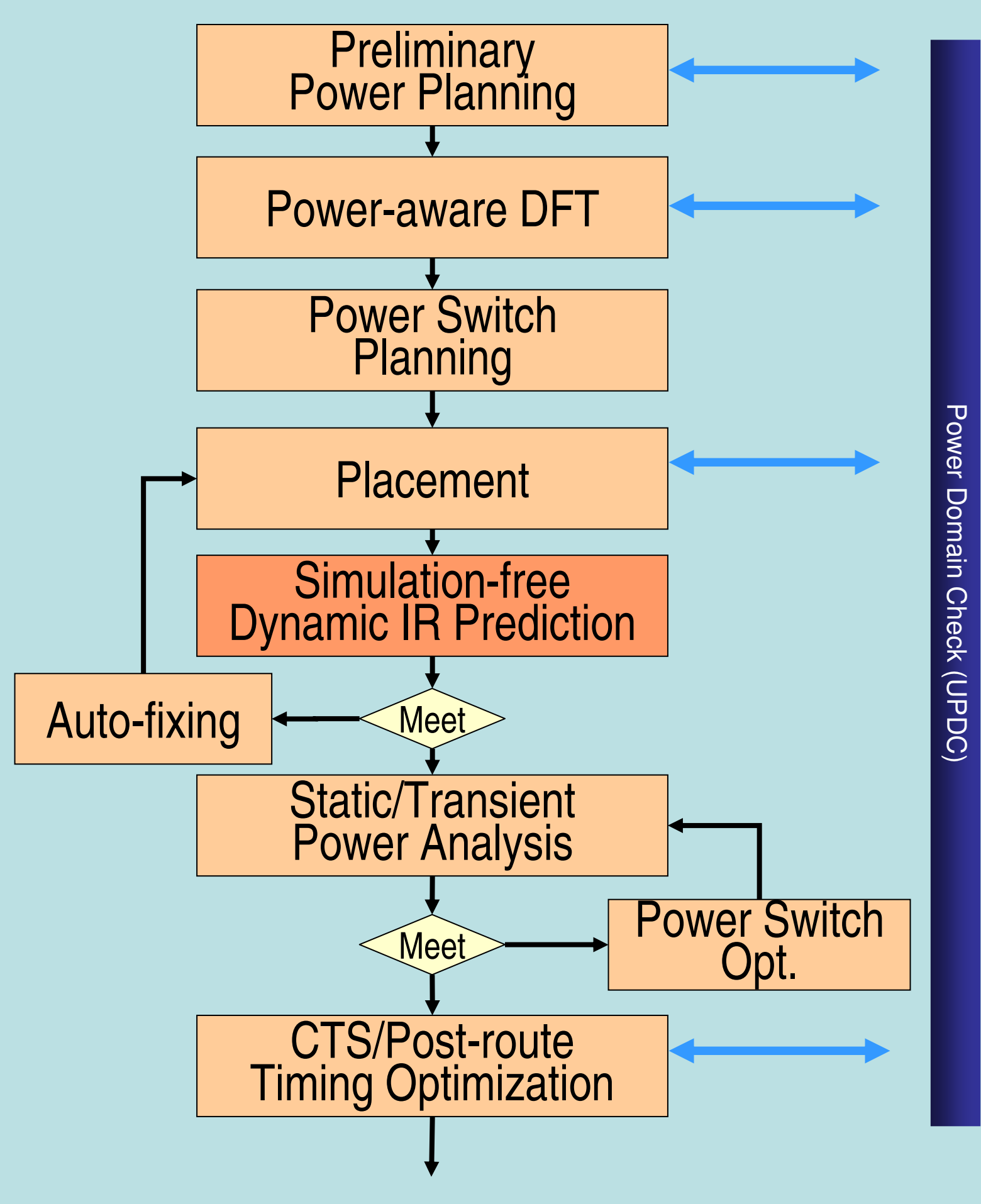
Traditional Substrate Noise Analysis

- Late in the design stage
- From the aspect of analog block
- Rough floorplan guidance from designer
- Incapable for sizable chip (capacitance)

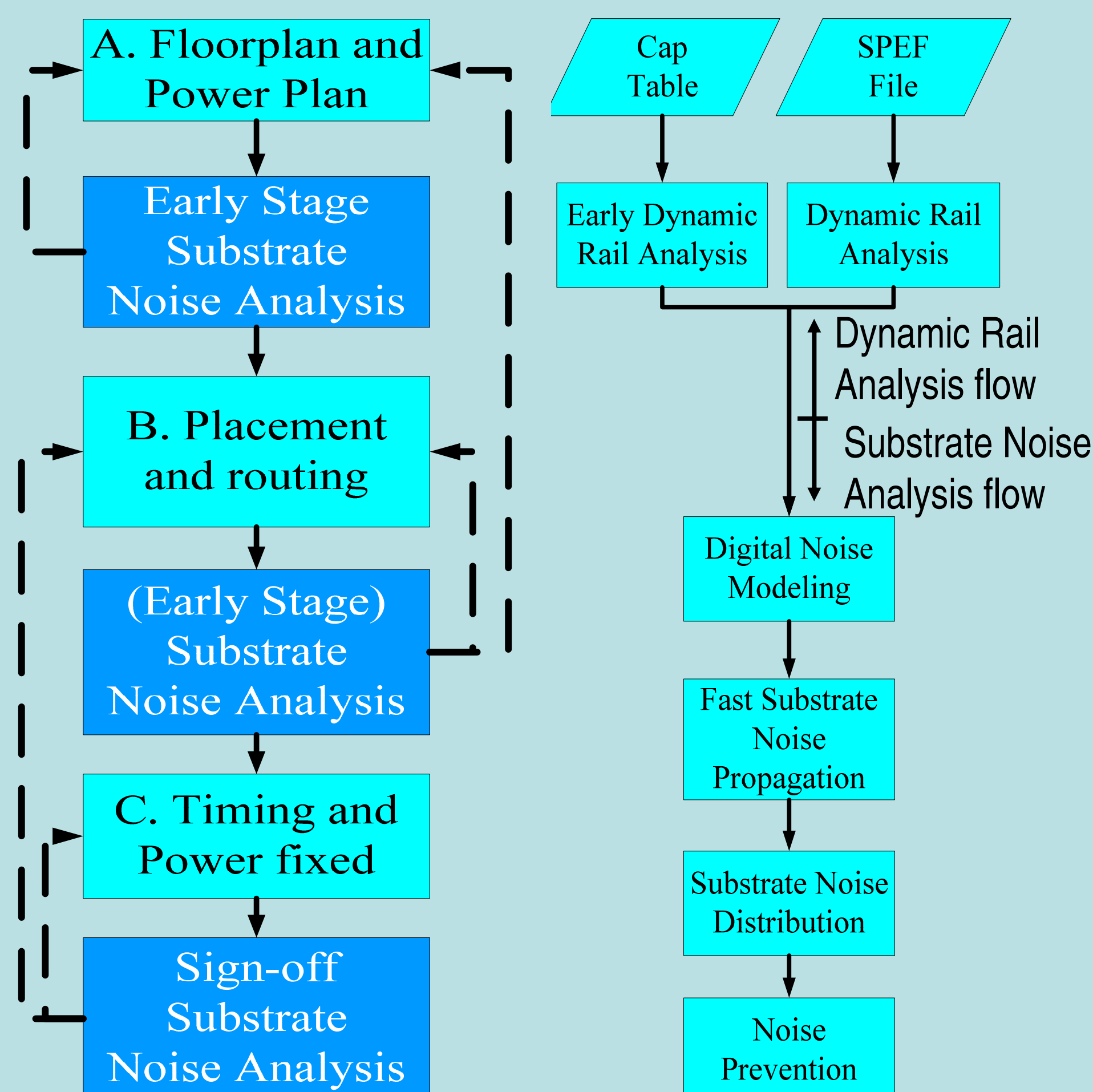
Tile Model



Dynamic IR Reduction



Substrate Noise Aware Implement Flow



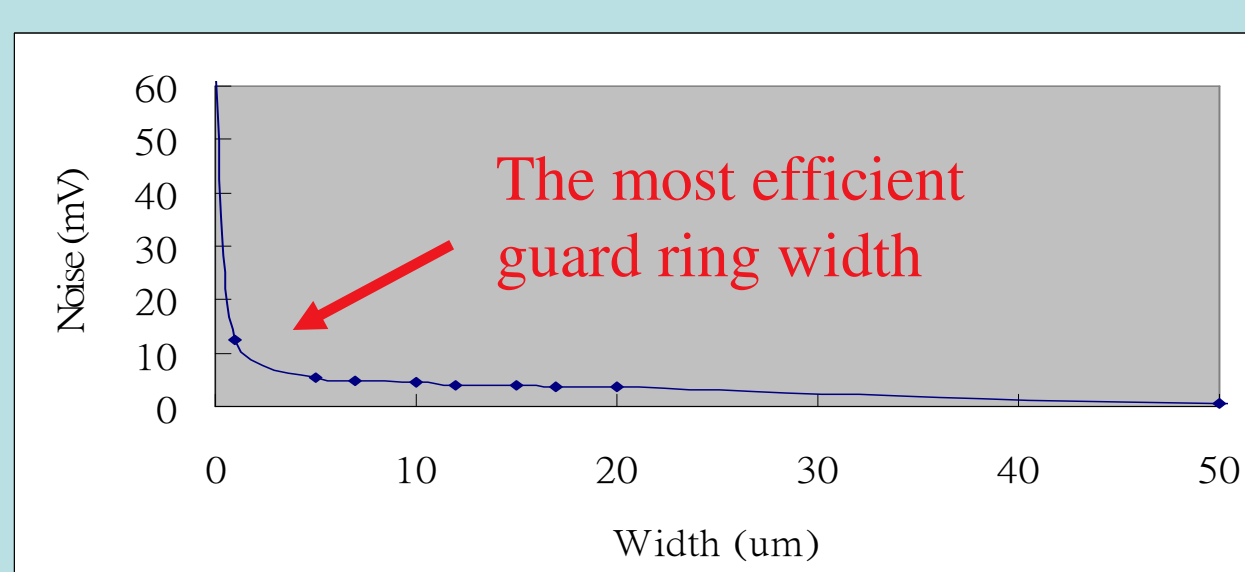
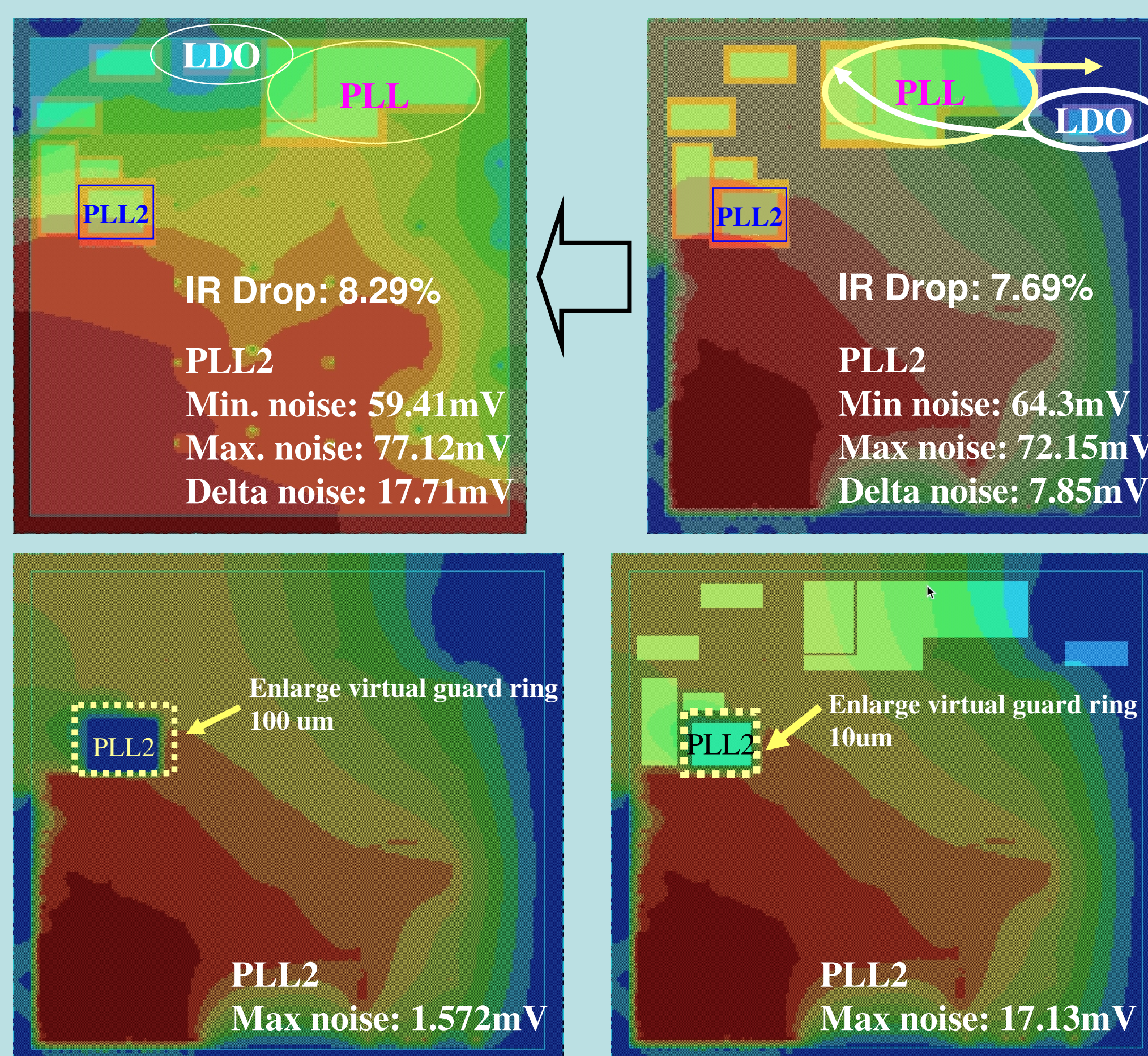
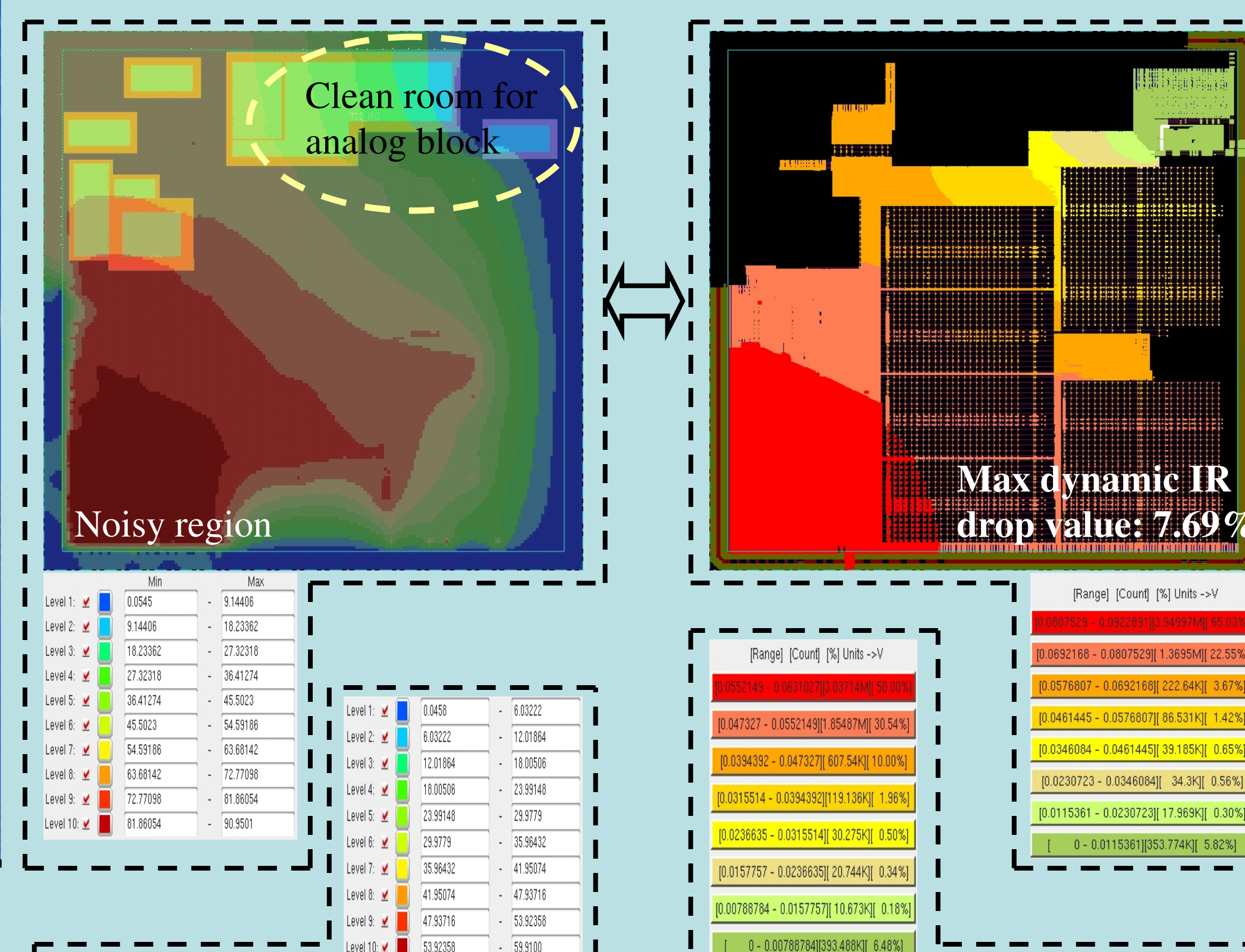
Experiment

Design Background

Process	TSMC 90nm LP
Die Size	3700um x 3700um
Instance count	100K
Power/Ground Nets	VDD/VSS
	VDDA/VSSA
	VDDD/VSSD

Run Time Compare

	EDI SNA	QRC RF
Size	100K Cells	3.6K devices
Run Time	135 minutes	120 minutes



Conclusion

- Substrate noise aware implement flow helps to give floorplan guidance in prototype stage according to substrate noise contour map.
- Because substrate noise is highly related to dynamic rail result.
- The ability and capacity to handle sizable chip is critical.
- What-if analysis helps us to get substrate noise result which has virtual guard ring and to decide effective guard ring width.
- Tool can also provide FFT based frequency analysis for the propagated noise waveforms.