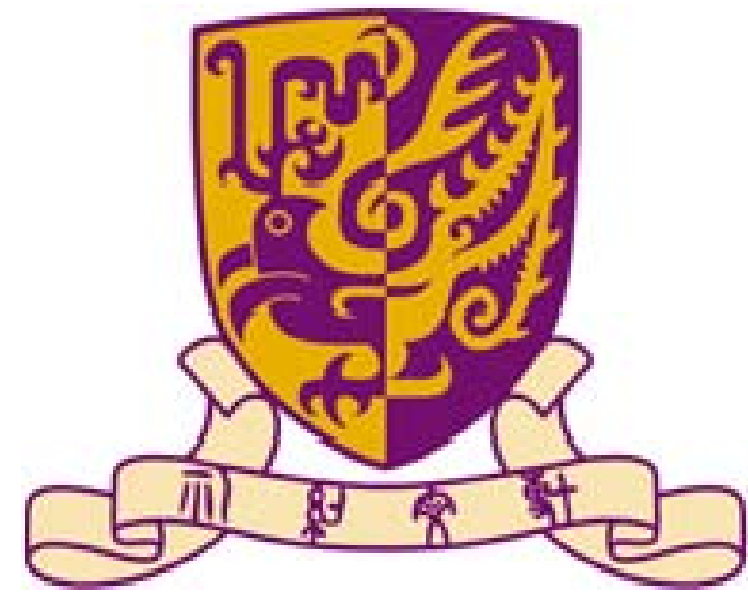


Physical Design of A Structured ASIC Based on ASIC Design Methodology



The Chinese
University of Hong Kong

Yanqing Ai¹, Steve C.L. Yuen¹, Thomas C.P. Chau², Sam M.H. Ho¹, Brian P.W. Chan¹, Oscar K.L. Lau¹, Kong-Pang Pun¹, Philip H.W. Leong³, Oliver C.S. Choy¹

¹Dept. of Electronic Engineering,
The Chinese University of Hong Kong
{yqai, clyuen, mhho, pwchan, kllau,
kppun, cschoy}@ee.cuhk.edu.hk

²Dept. of Computer Science and
Engineering,
The Chinese University of Hong Kong
cpchau@cse.cuhk.edu.hk

³School of Electrical and Information
Engineering
The University of Sydney
phwl@ee.usyd.edu.au

Structured ASIC

As a fabric filling the gap between ASICs and FPGAs, Structured ASIC (SASIC) consists of arrays of pre-fabricated yet configurable logic blocks together with hard blocks. To make the design flow of SASIC more effective and efficient, we present a novel SASIC design methodology based on a customized ASIC flow using standard tools.

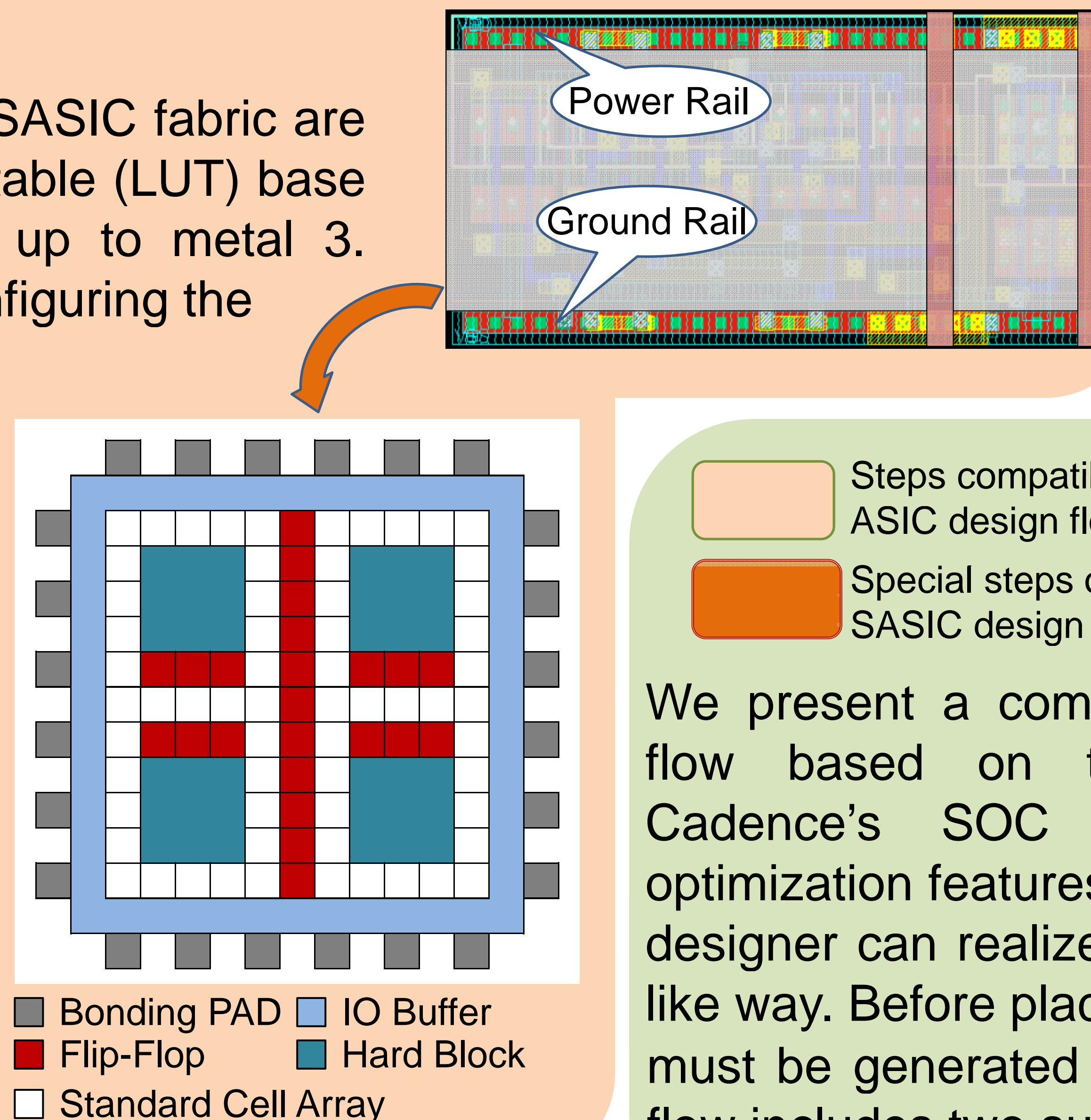
Building Cell and General SASIC Fabric

Building Cell

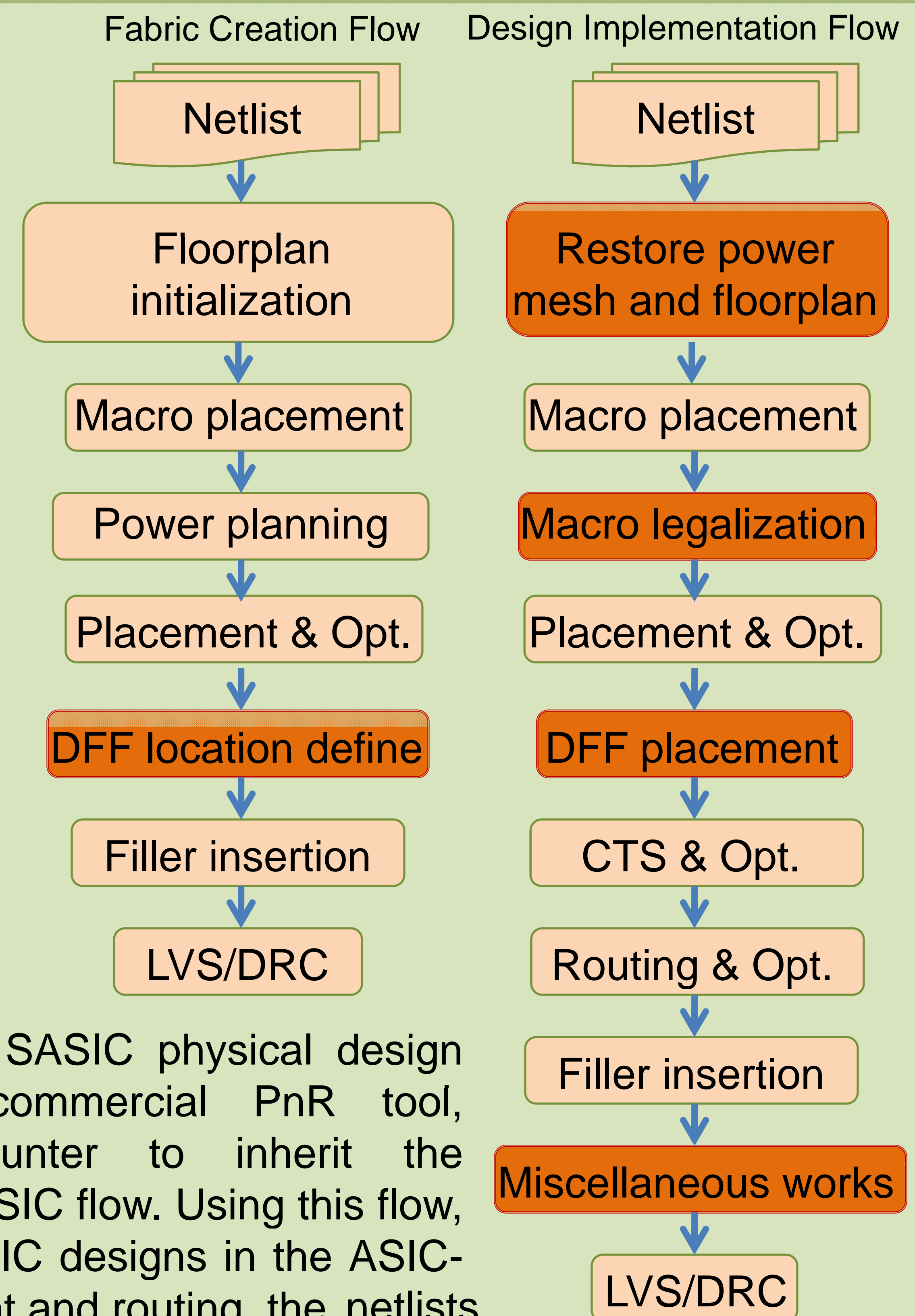
The combinatorial logic cells of our SASIC fabric are implemented with a 3-input look-up table (LUT) base cell, each of which utilizes layers up to metal 3. Because only metal 3 is used for configuring the logic function of the LUTs, all the cells have the same masks in any other layers and as such exchange of any two cells locations won't change these masks of the chip.

General SASIC Fabric

The proposed structured ASIC fabric consists of logic cells, arrays of DFFs, hard macros and power mesh.



Proposed Physical Design Flow



We present a complete SASIC physical design flow based on the commercial PnR tool, Cadence's SOC Encounter to inherit the optimization features of ASIC flow. Using this flow, designer can realize SASIC designs in the ASIC-like way. Before placement and routing, the netlists must be generated using an ASIC synthesis flow and our cell library. The flow includes two sub-flows: fabric creation and design implementation flow.

Experimental Results

All experiments are conducted on the same UMC 0.13um process. The designs implemented include four circuits: MATHCORE, To2_f, S38584 and NOVA. MATHCORE is a floating point unit, To2_f is a video frame data convertor for an LCD backlight, S38584 is the largest of the MCNC benchmarks and NOVA is an AVS H.264 decoder.

Area Comparison

Design	Faraday lib (um ²)	Our cell lib(um ²)	Top metal	Normalized area increase
MATHCORE	312136.51	1246201.92	4	4.0
To2_f	45410.11	146670.77	4	3.2
S38584	178336.06	1091169.74	4	6.1
NOVA (1)	5414381.94	12272149.30	4	2.7
NOVA (2)	2320450.50	9642402.72	5	4.2
Average	NA	NA	NA	4.0

Timing Comparison

Design	Faraday lib (ns)	Our cell lib (ns)	Clk period (ns)	Degradation respect to the clock period
MATHCORE	-1.16	-2.49	11	12.1%
To2_f	6.53	1.68	10	48.5%
S38584	6.55	3.86	11	24.5%
NOVA (1)	19.67	6.25	50	26.8%
NOVA (2)	23.07	-0.52	50	47.2%
Average	NA	NA	NA	31.8%

Mask Number Comparison

Top metal	ASIC flow	SASIC flow	Mask reduction
4	25	3	88%
5	25	5	80%

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