

For Better Results: Establish Closer Ties Between Formal Verification and Simulation Teams

Problem: Separate simulation and formal verification flows lead to verification holes

- Different Assertion Languages
- Duplicate copies of assertions
- Assertions must be translated in order to reuse them
- Constraints for formal verification not checked

New opportunity: Standard assertion language

- Common Assertion Language for simulation and formal
- Assertions freely shared
- Simulation and formal team can now collaborate
- Constraints for formal verification now checked every day in simulation

Coding Guidelines

- Code formal assertions with action blocks so they will have a readable message in simulation
- Defines for formal which map VMM messages to \$display
- Limit cross-module references to types supported by all tools

Release formal constraints and checkers to simulation environment

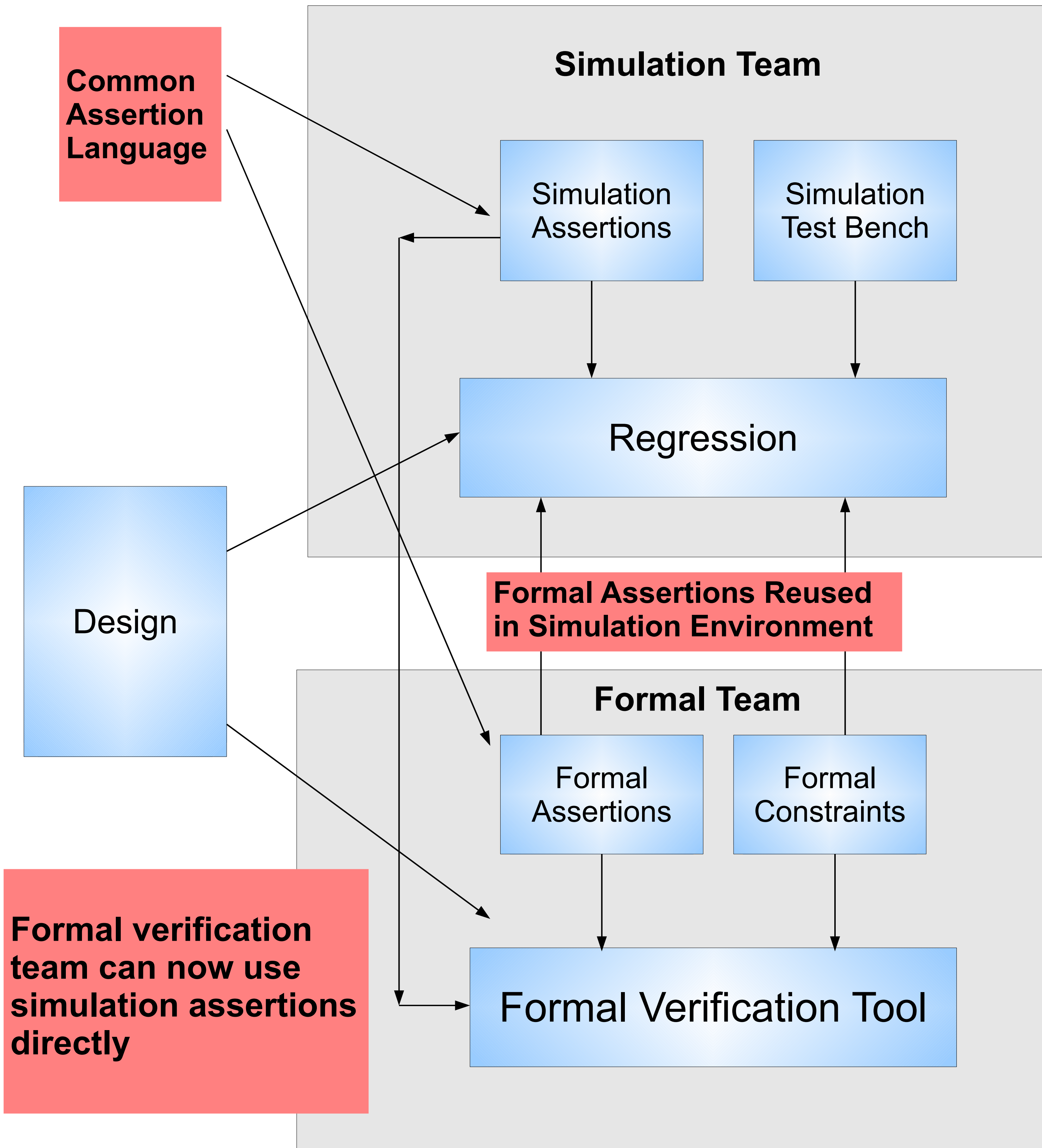
- Simulation release regression finds lots of problems with formal constraints
- Early warning for design changes that affect formal verification

Formal proof regression

- Run automatically
- Results displayed on the web

[illegible]

NEW METHODOLOGY



Results

- Better Cooperation between formal verification and simulation teams
- Release process catches problems with formal constraints
- Formal constraints catch bugs in the design
- Formal team is able to reuse simulation assertions

