

# Experiences in Addressing Critical Power Management Verification Issues in Low Power Designs

Bhanu Kapoor, Amit Kumar, John Goodenough, Prapanna Tiwari

Mimasic

CSR

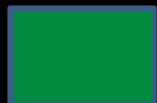
ARM

Synopsys

DAC 2010 User Track

# Power Types Targeted

			Power Being Managed		
Technique			Standby Leakage	Active Leakage	Dynamic
Power Gating	PG				
Retention with PG	RPG				
Multiple Supply Voltages	MSV				
Dynamic Voltage Scaling	DVS				
Adaptive Voltage Scaling	AVS				
Multi-Threshold CMOS	MTCMOS				
Adaptive Body-Biasing	ABB				



Primary



Secondary



Verification Impact

*mimasic*

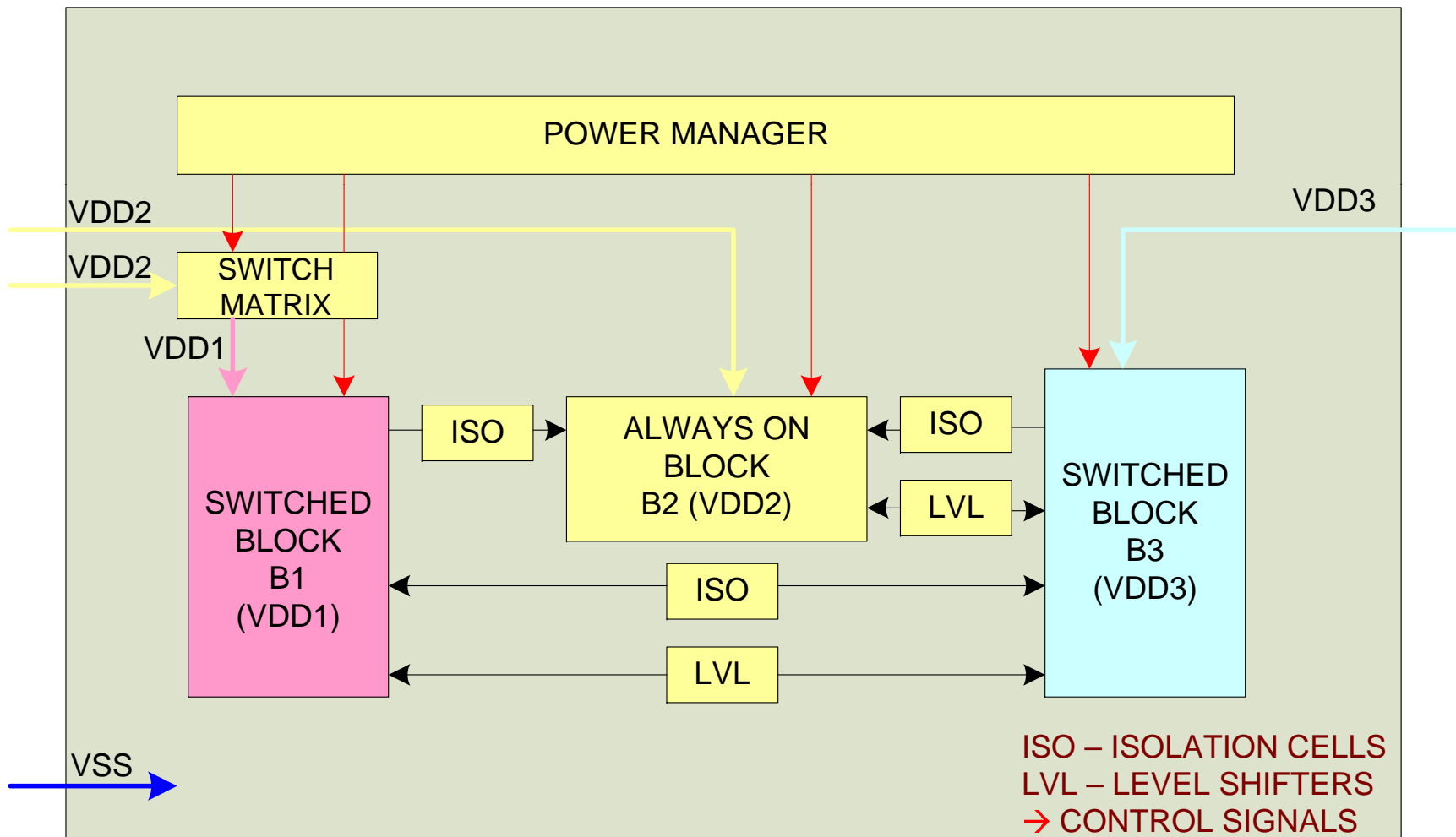
# Resolving PM Verification Issues

PM Verification Issue	Simulation	Formal	Rule-Based
Power On Reset Problems	Yes	No	No, Reset Cnvt (Y)
Power Connectivity	Yes	No	Yes
Domain Isolation	Yes	No	Yes
Power Switching	Yes	No	Yes
Level Shifting	No	No	Yes
Power Sequencing	Yes	Yes	No
State Retention	Yes	Yes	No
Power Controller	Yes	Yes	No
Always-on Buffers	No	No	Yes
Decap Insertion	No	No	Yes
Hardware/Software Intf.	Yes	Yes	No

***mimasic***



# Typical Architecture





# Static Verification

---

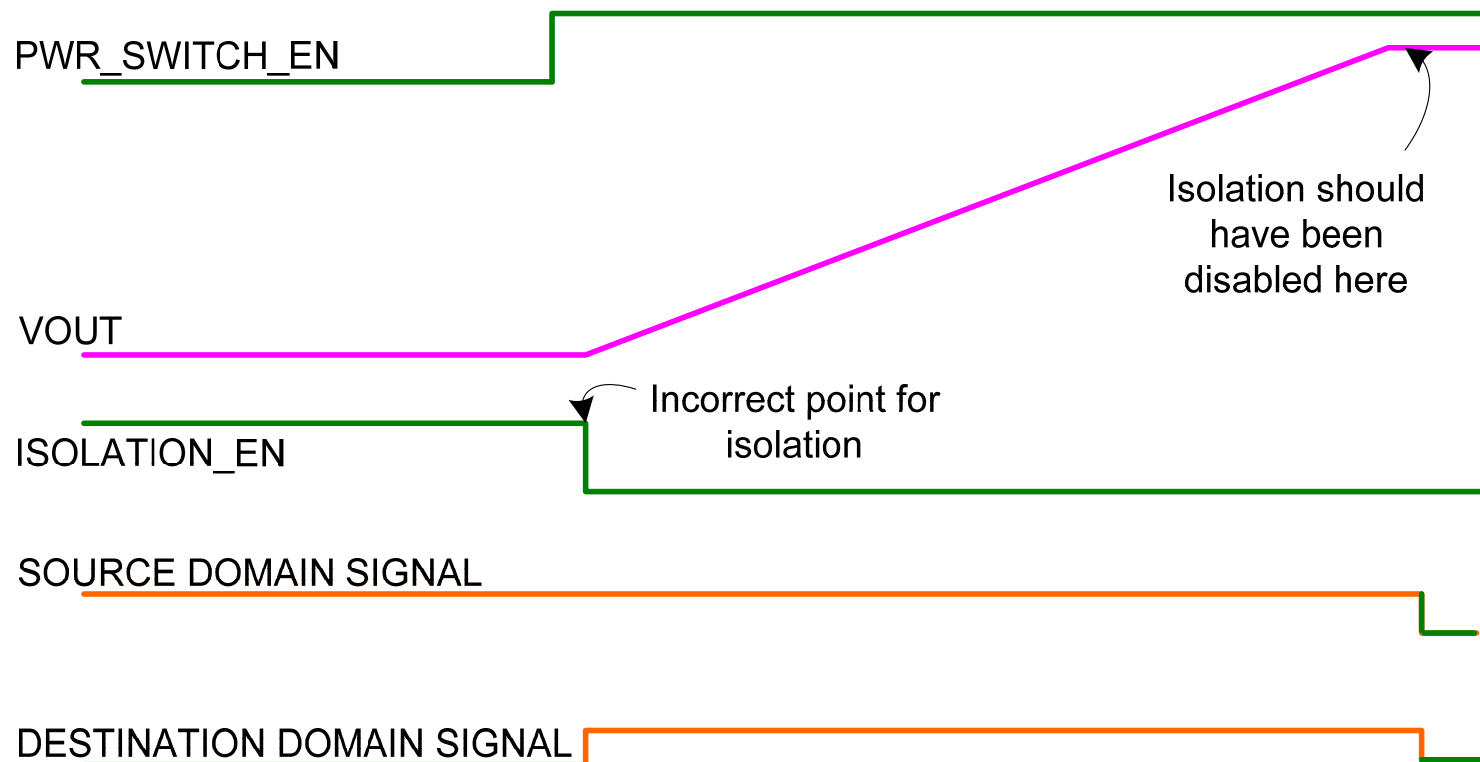
- Structural checks –
  - Level shifters
    - Correct placement (missing/inadvertently placed).
    - Connections as per voltage domains defined.
  - Isolation cells
    - Correct placement (missing/inadvertently placed).
    - Correct TYPE based on expected output.
    - Insertion of buffers in isolation paths during synthesis.
  - Always ON buffer
    - Correct placement & connections.
  - Power switch
    - Correct placement & enable signal.
  - Ensuring power integrity in a full/partially flattened netlist during synthesis.



# Dynamic Verification

## Scenario#1 – Power sequencing & Voltage ramp

Generation of isolation control signal didn't account for voltage ramp up time corrupting outputs.

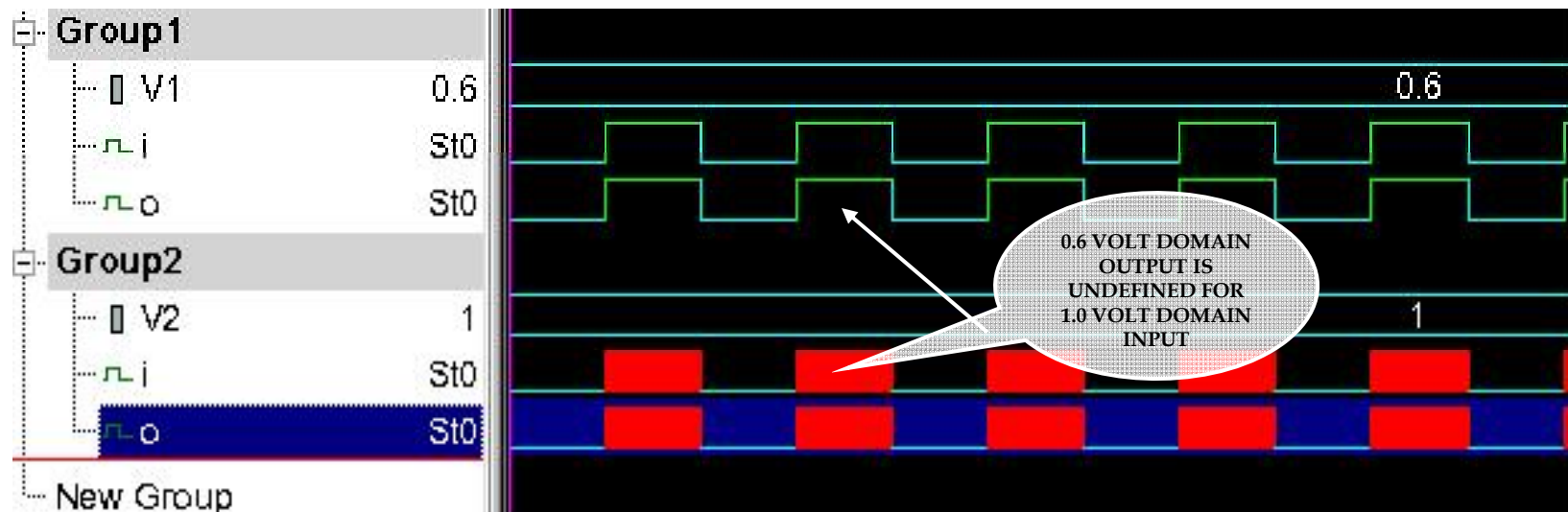




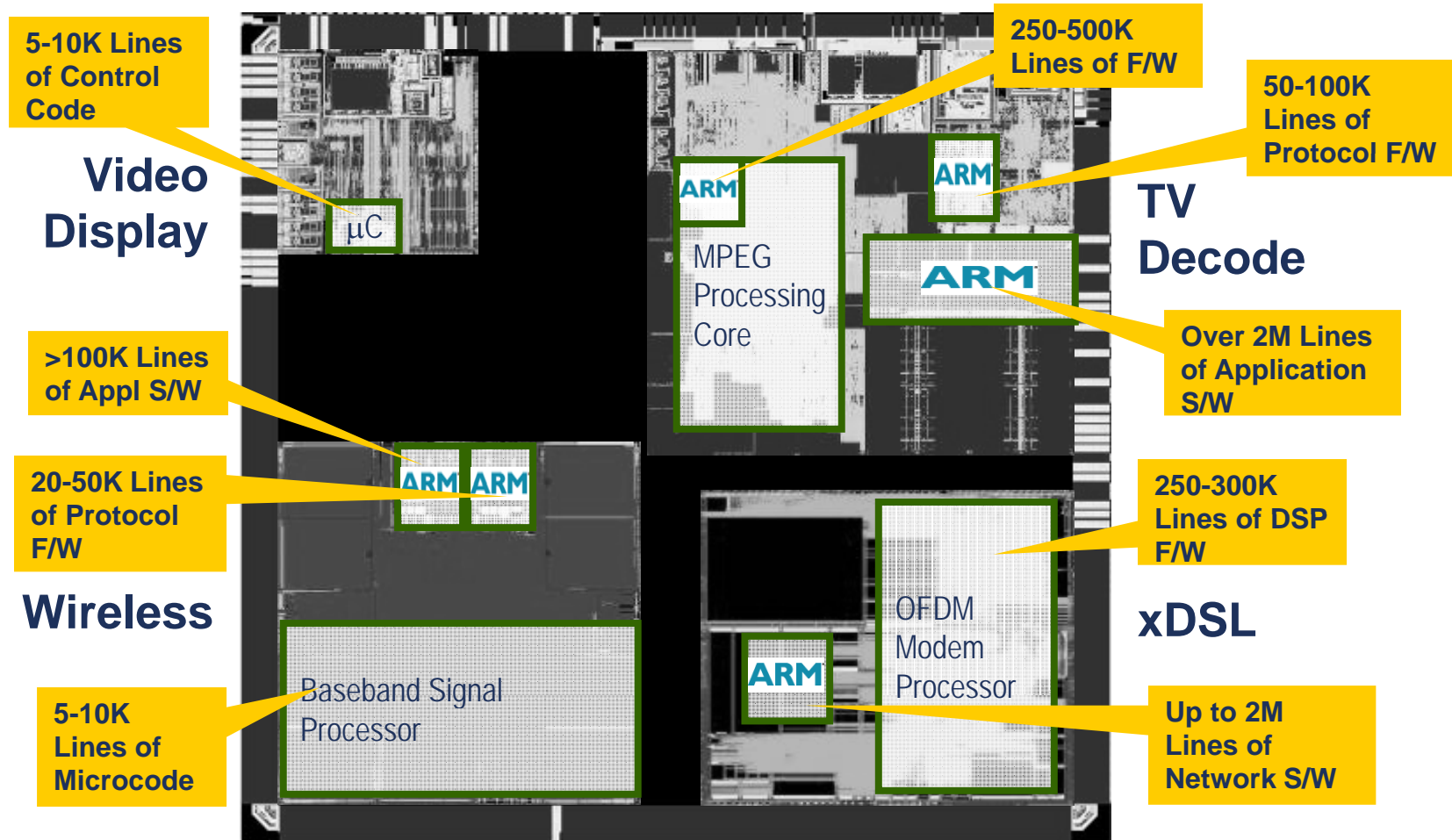
# Dynamic verification

## Scenario# – Insertion of apt cells

Incorrect or absence of level shifters corrupting signals across domains.



# What == State Space Explosion



Nearly five million lines of code to enable Media gateway



The Architecture for the Digital World®

**ARM®**

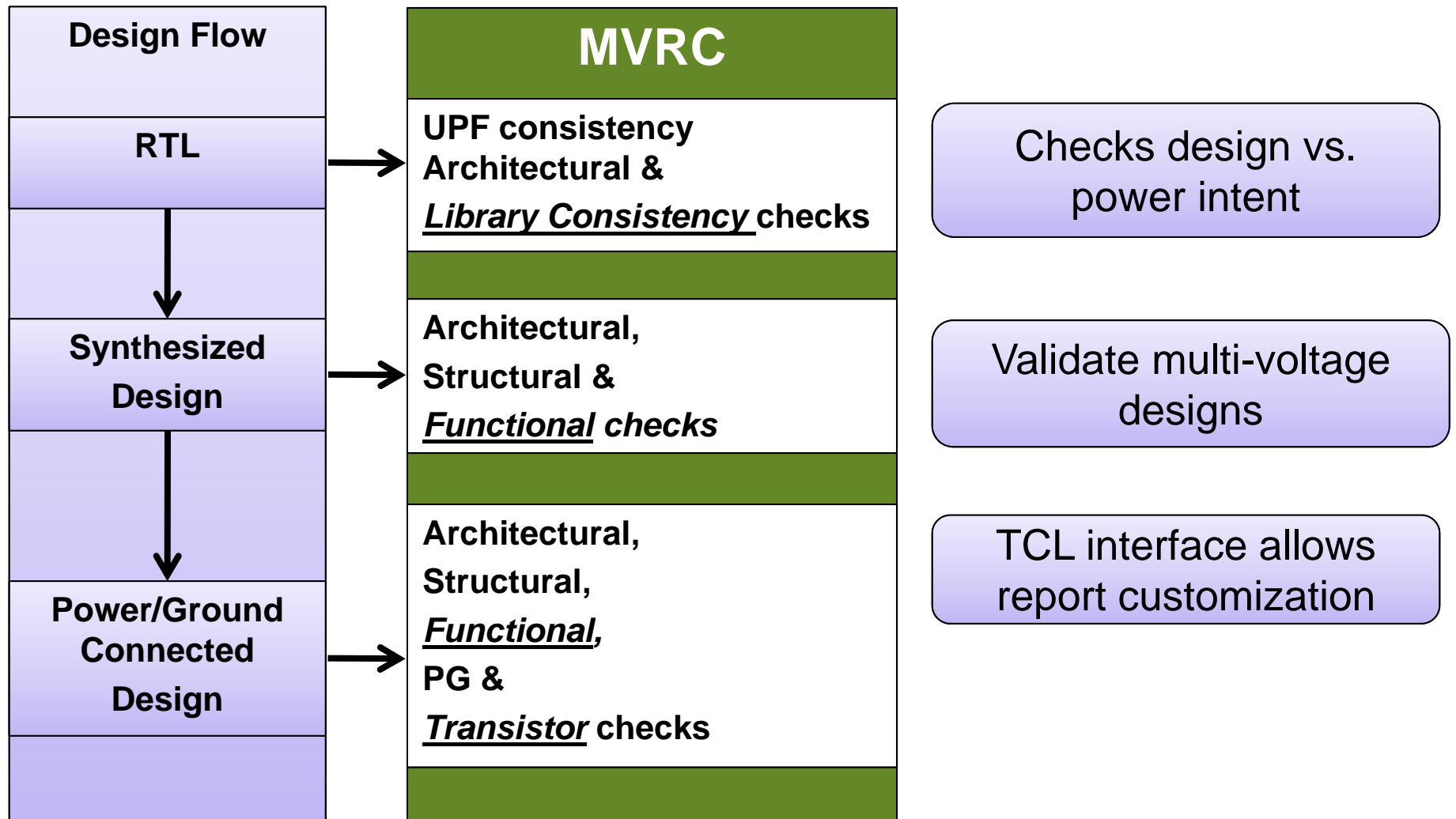


# ...Complex Design - Complex Verification

---

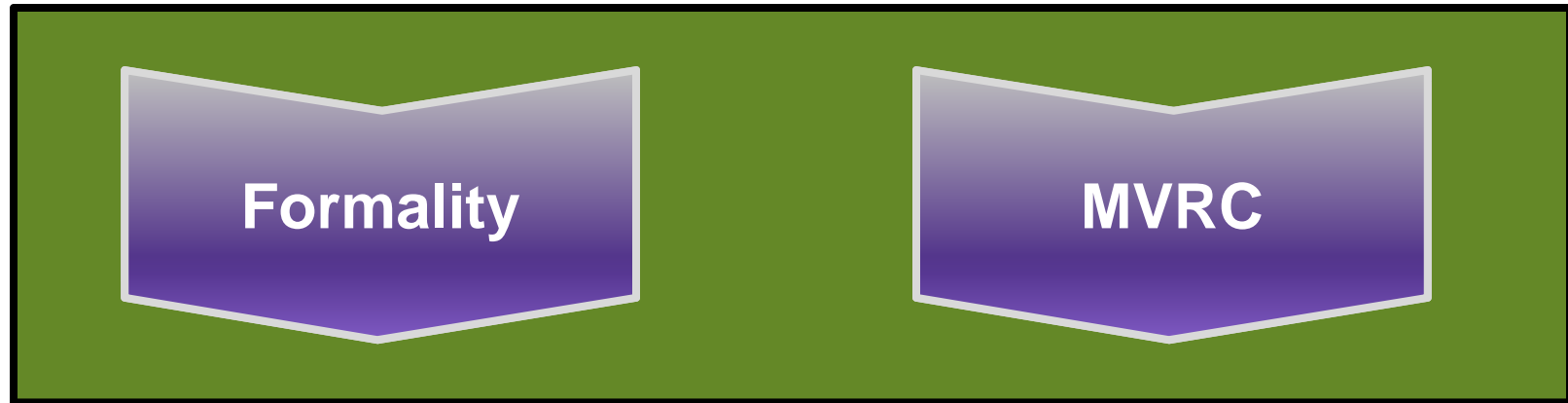
- Increasing Scope of State Space to be Verified
  - Larger SoC Subsystems
  - More complex Design Representation
  - Explosion in operating modes (Don't Forget Security too)
- .. Needs good Process Automation and Workflow Integration
  - Emphasis on measuring progress and qualifying sign off
- ... and margins are under pressure
  - Techniques must look at enterprise scaling – team and infrastructure
- Validation is really and exercise in Risk Reduction
  - Need to be very clear about what is left to do
  - ... and it *never* stops

# Static Checks Throughout The Design Flow



# Low Power Static Checks

*Companion Products*



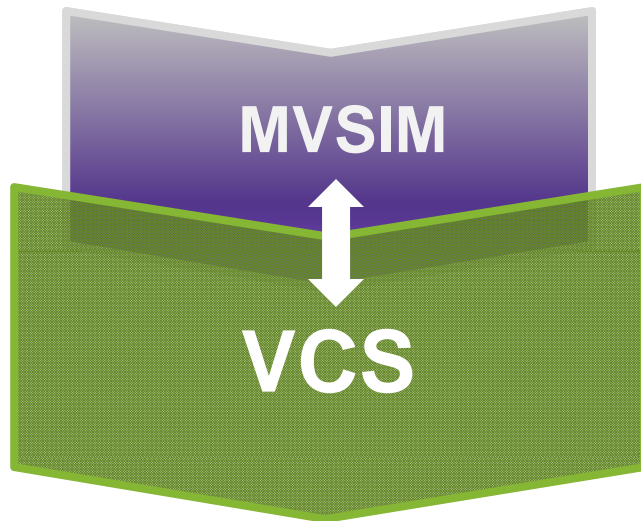
**Equivalence Checks**

**Static Checks**



**Architected for Low Power Static Checks**

# Advanced Low Power Simulation



Simulation of power transitions and sequences for power gating

Voltage-aware simulation for Low-Vdd Standby and DVS

Automated assertions and coverage

Accurate simulation of multi-voltage and hierarchical designs

Support for complex power switches and isolation policies



**Architected for Low Power Verification**



### Education

- Bugs related to low power techniques
- Documented examples from real designs
- Impact on Low power verification

### Verification

- Low power perspective into verification planning
- Power -aware assertions and coverage

### Reuse

- Power -aware base classes
- Best-practice rules and guidelines from over 30 companies

## Industry's First Low Power Verification Methodology