

A CASE-STUDY INVOLVING AN OVM-BASED ESL VERIFICATION FLOW

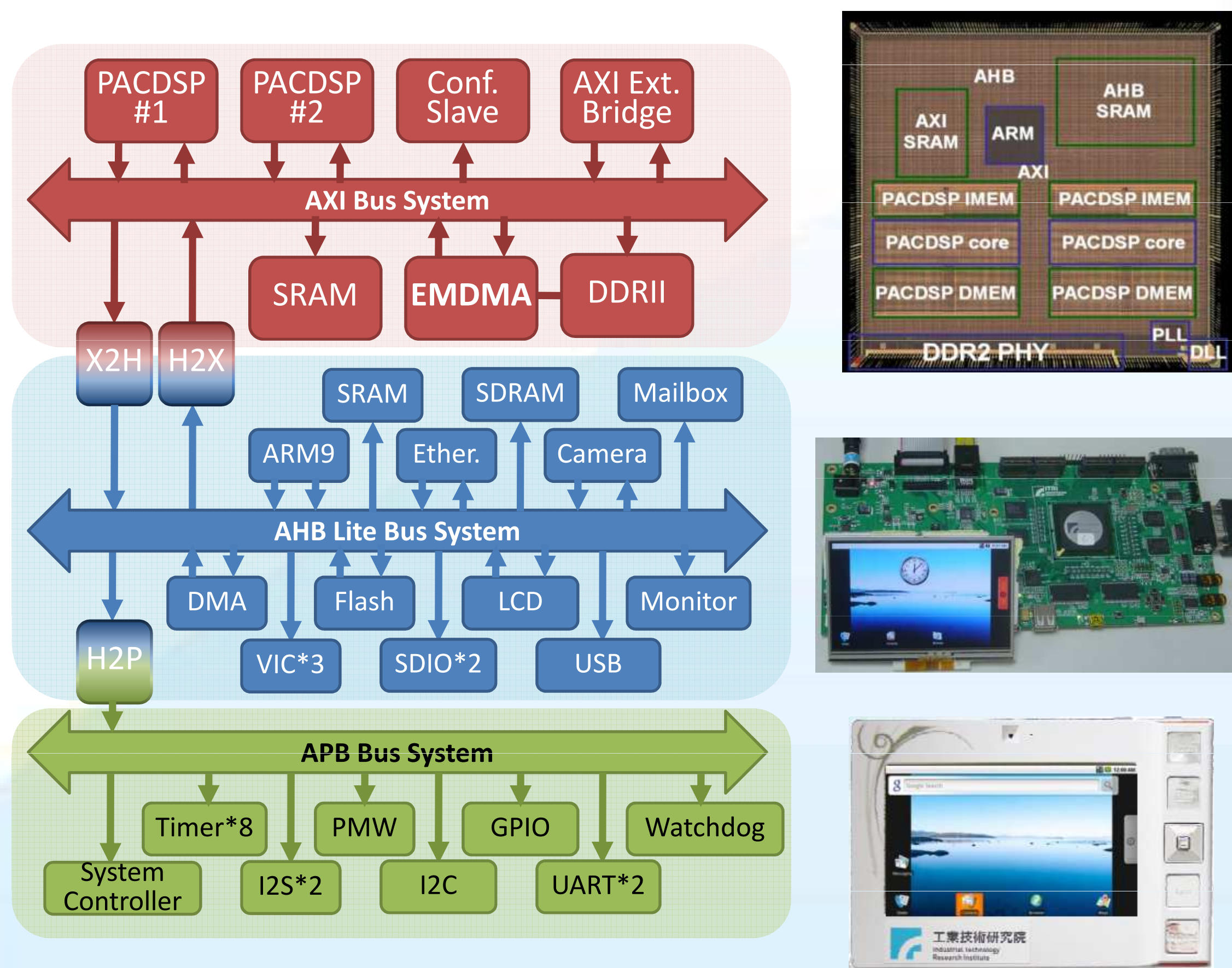


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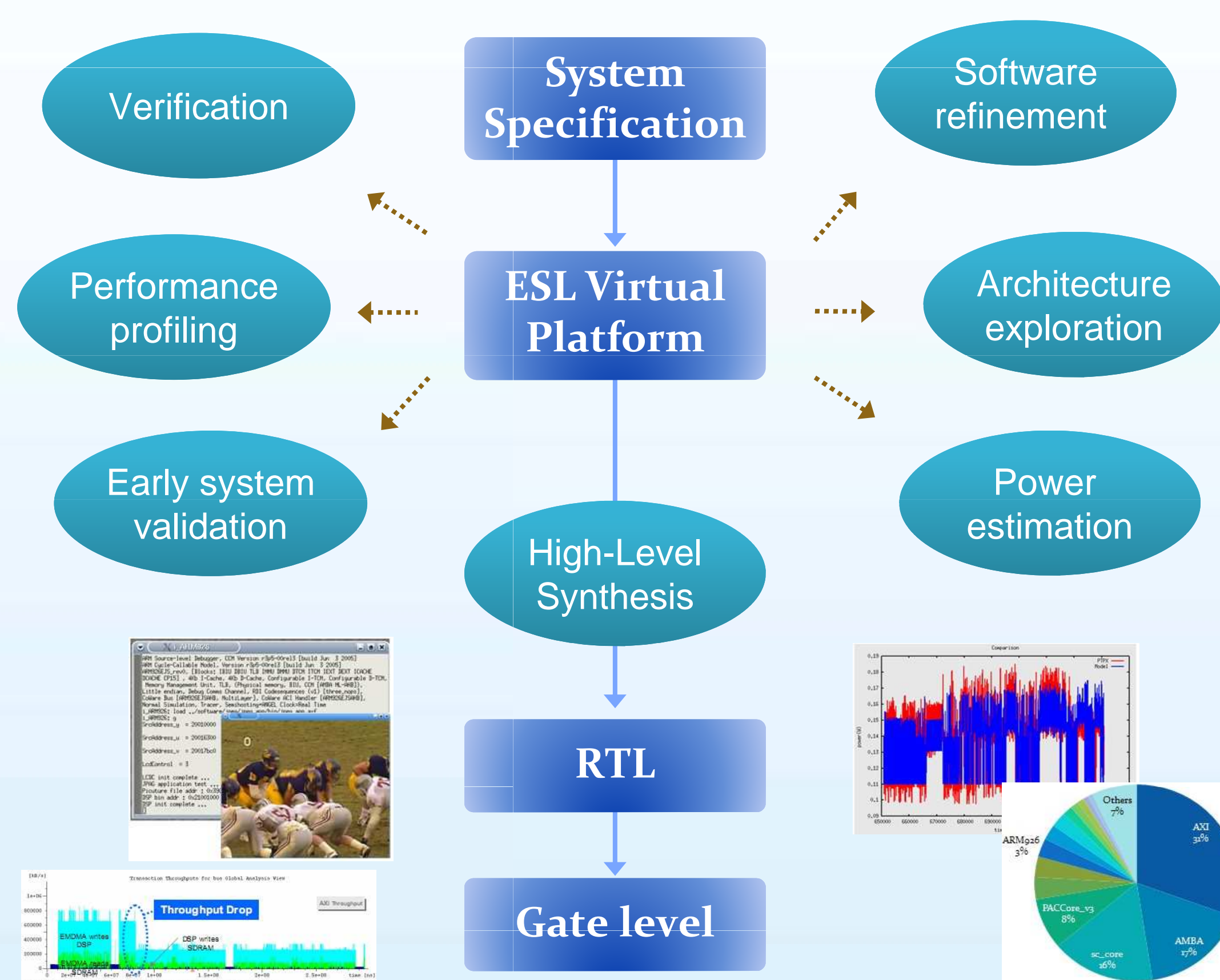


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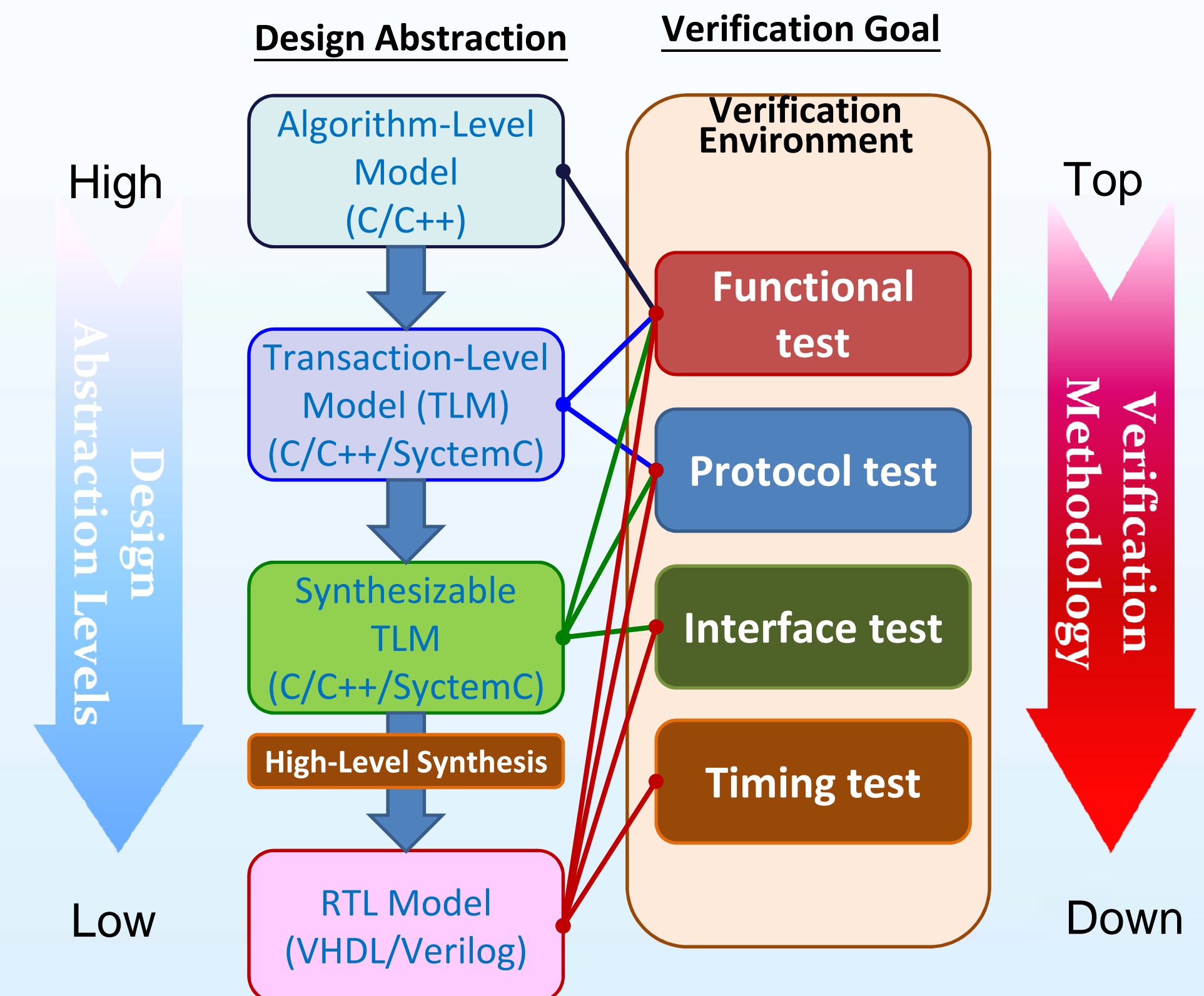
Energy-Aware PAC Duo SoC



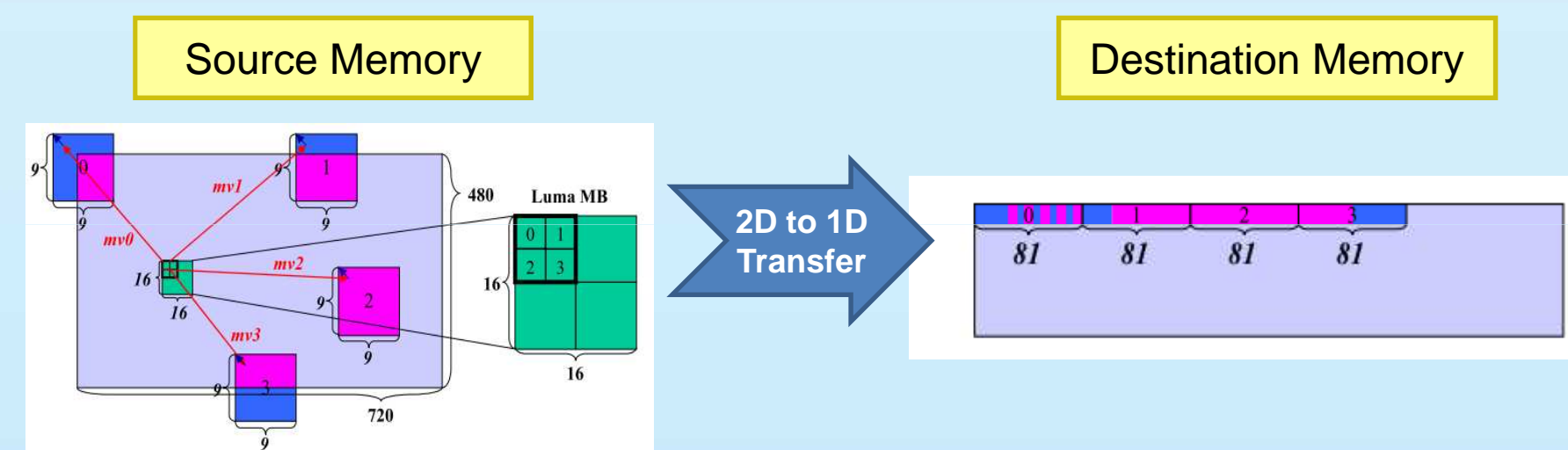
ITRI ESL Design Methodology



Motivation: How to Reuse the High Design Abstraction Level's Verification Env.

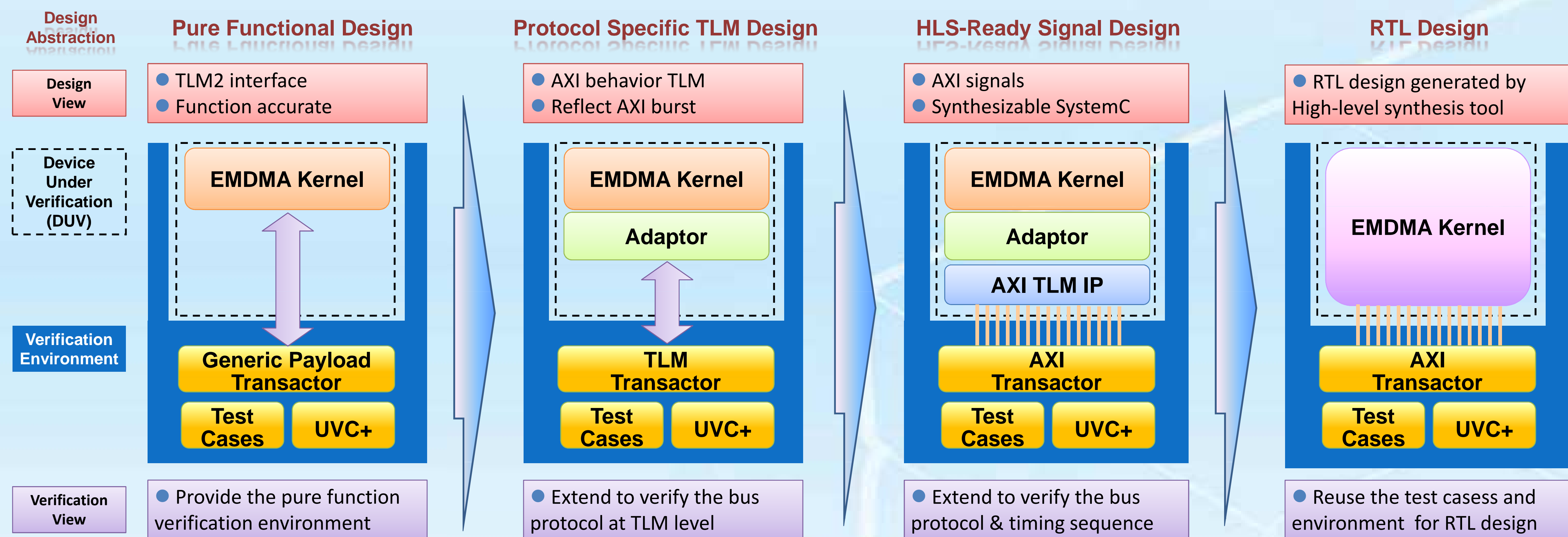


Case Study Enhanced multimedia DMA (EMDMA)



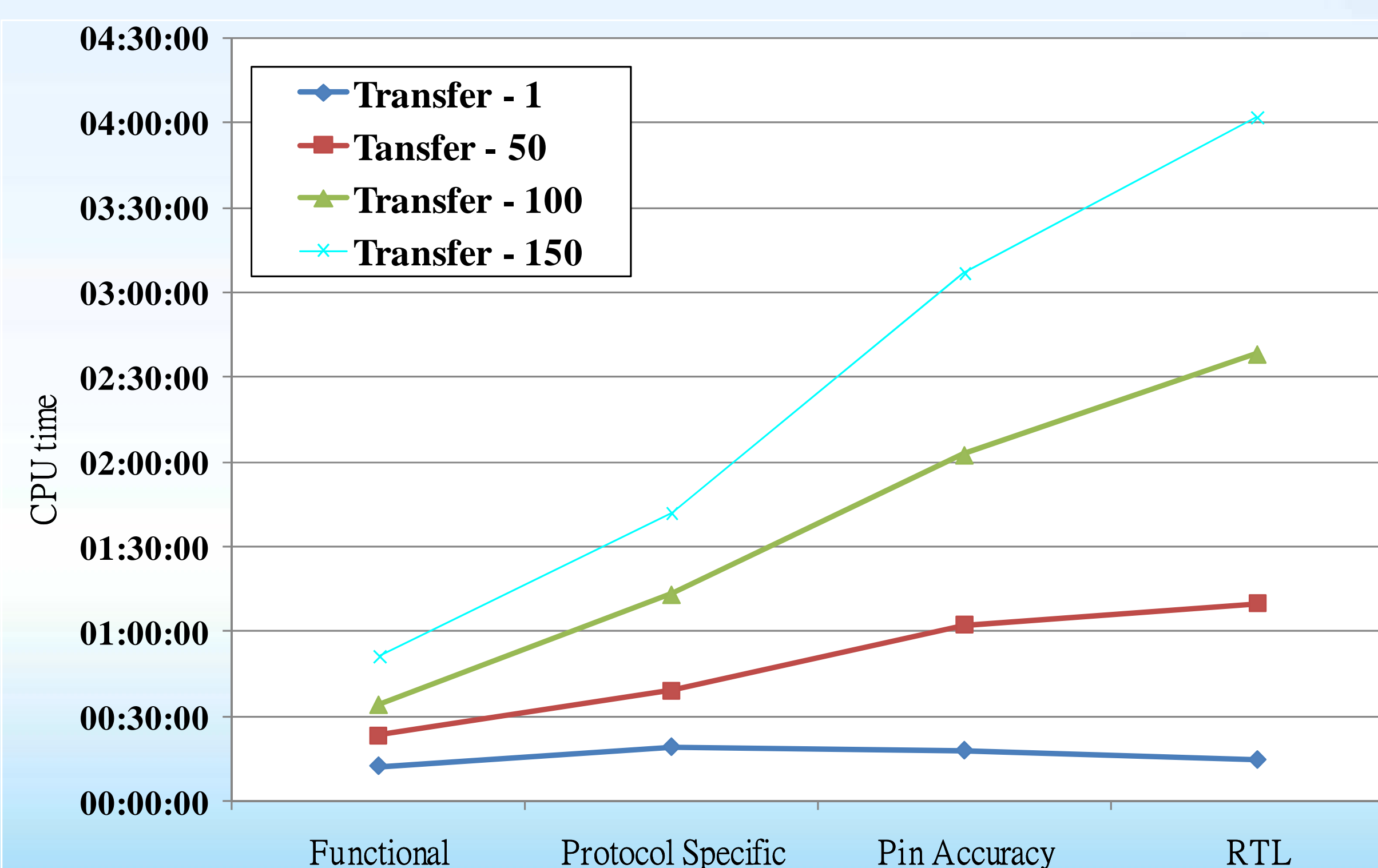
- I/O Interface : 1 AXI Slave port and 2 AXI Master ports
- Support 4 general channels, 4 multimedia channels, and 16 link-list nodes
- Support general data transaction:
 - Source gather function
 - Destination scatter function
 - Repeat function
- Support multimedia block transaction
 - Luma/Chroma (YUV420/422/444) block type
 - 1D-to-1D, 1D-to-2D, 2D-to-1D, and 2D-to-2D
 - Data padding function (out of frame)

TLM-Driven Design and Verification Flow



Experimental Results

Compared Items	Traditional RTL Verification Flow	TLM-Driven Verification Flow
Abstraction Level	RTL	RTL
Test Patterns	50 random test patterns	50 random test patterns
Total Transfer Bytes	608,771 bytes	625,128 bytes
Adopted Data Type	Byte	GP Burst
Simulation Time	8m52.4s	6m39.3s



Summary

- The design productive is about 2x fast than traditional hand-edit RTL design
- Under the same timing constrain, the QoR of EMDMA with AXI TLM IP is colse to hand-edit version
- The UVC+ (OVM based library) are useful to reuse of verification work over all abstraction levels
- Additional benefit when partition the work between abstraction levels to make work most efficient
- The productivity of TLM-driven verification flow is better than traditional verification flow, even this was the first time
- Some challenges still open: the design throughput, the verification IP for protocol specific TLM, untine TLM verification supporting