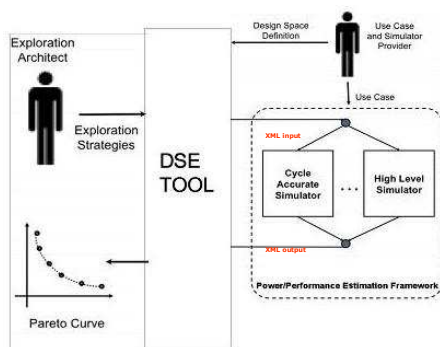


In present era of Multi-Processor System-on-Chip (MPSoC) embedded devices, to run multiple applications optimally (in terms of execution time and power consumption) is an enormous challenge. Embedded designers usually tackle this challenge by dividing it in two parts : at design-time, Design Space Explorations (DSE) are performed to derive Pareto set of optimum operating points for each application, and at run-time, embedded device is monitored continuously to operate at one of the points in the derived Pareto set. With growing complexity of embedded devices and with time-to-market pressures, at design-time, it is not trivial to derive the operating point Pareto set.

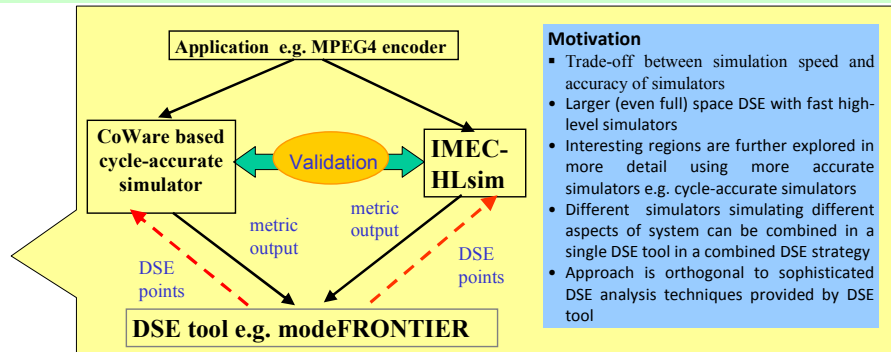
We have developed techniques to tackle this issue of DSE. At design-time, we use DSE with multiple simulators running at multiple abstraction levels to converge quickly to Pareto set of operating points. Our key contribution is the idea of using multiple simulators under one DSE tool in a single comprehensive DSE strategy. We have developed necessary ingredients to achieve such an integration. Note that use of multiple abstraction levels is orthogonal to sophisticated analysis techniques provided by current DSE tools. Also our techniques are orthogonal to a model refinement approach (across different abstraction levels) that is taken in many simulation environments. We applied our methodology on an embedded device having eight processor cores running an MPEG4 encoder. With our DSE methodology, we could derive accurate Pareto set much quickly (as compared to full-space explorations on a cycle-accurate simulator).

Typical DSE strategy with DSE tool

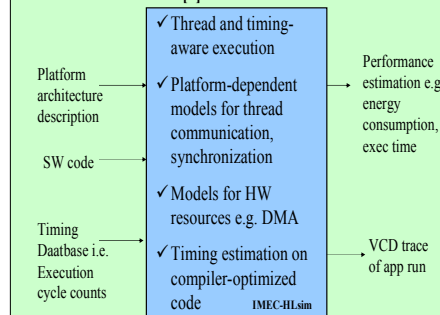


Ingredients needed for such DSE recipe:

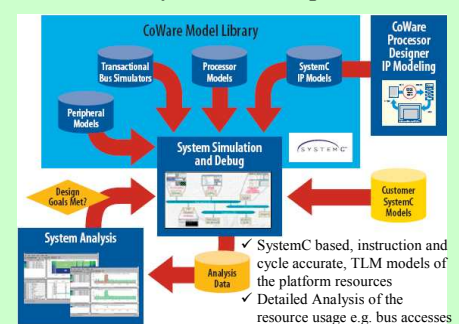
- DSE tool supporting a robust DSE strategy, supporting multiple simulators
- Standardized XML interfaces between DSE tool and simulators
- Same application code should be used across simulators
- Validation, if possible, across different simulators



IMEC-HLsim simulator [2] :

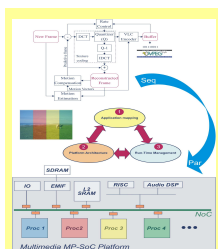


CoWare based cycle-accurate platform :

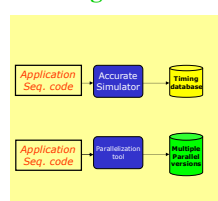


Applying our approach : DSE of multiple parallel versions of MPEG4 encoder on an eight-core MPSoC platform

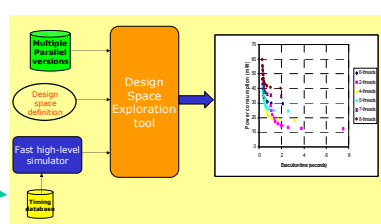
Target platform for MPEG4 encoder



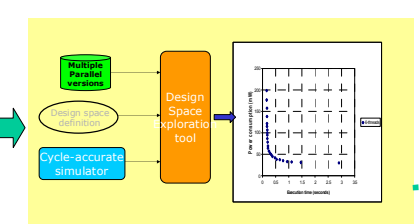
Prepare parallelizations and timing information



DSE of 2 to 8-threaded application running on a 8-core platform with processor clock frequencies 20-200 MHz, run with a high-level simulator



DSE of 6-threaded application running on a 8-core platform with processor clock frequencies 20-500 MHz, run with a cycle-accurate simulator



References:

- 1) Prabhat Avasare, et al, "High-Level Performance Estimation Using Simulators At Multiple Abstraction Levels", DATE'09 Friday Workshop on Design of Embedded Parallel Platforms
- 2) Rogier Baert, E. Brockmeyer, S. Wuytack, T. Ashby, Exploring parallelisations of applications for mpsoC platforms using MPA, Proceedings of DATE'09, pg 1148-1153.