

Correlation and Predictability within a Complex Hierarchical Design

General Hierarchical Design Challenges:

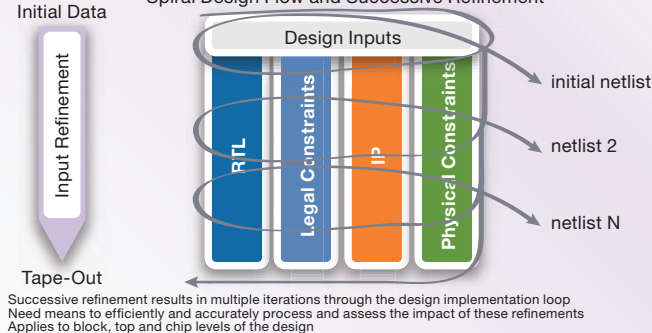
- Islands of expertise - Typically have separate groups with front and back end expertise; maybe at different sites, even different companies.
- Parallel development of top and block levels and design flow complexity makes for multiple hand-off points between islands of expertise.
- Careful attention must be applied to ensure tight correlation between front and back end, else:
 - may encounter surprises in physical design,
 - time to results is unnecessarily extended,
 - design convergence is jeopardized.

Case Study Specific Challenges and Details:

- 1.3M instances at top level
- 2 hierarchical blocks of ~500k each
- 65nm libraries
- Multi-voltage design
- 412 clocks
- Numerous memories
- Existing timing constraints cannot be met, seeking best performance
- Front/back-end correlation / predictability is critical
- Baseline top level run time from RTL to placed gates of 86 hours

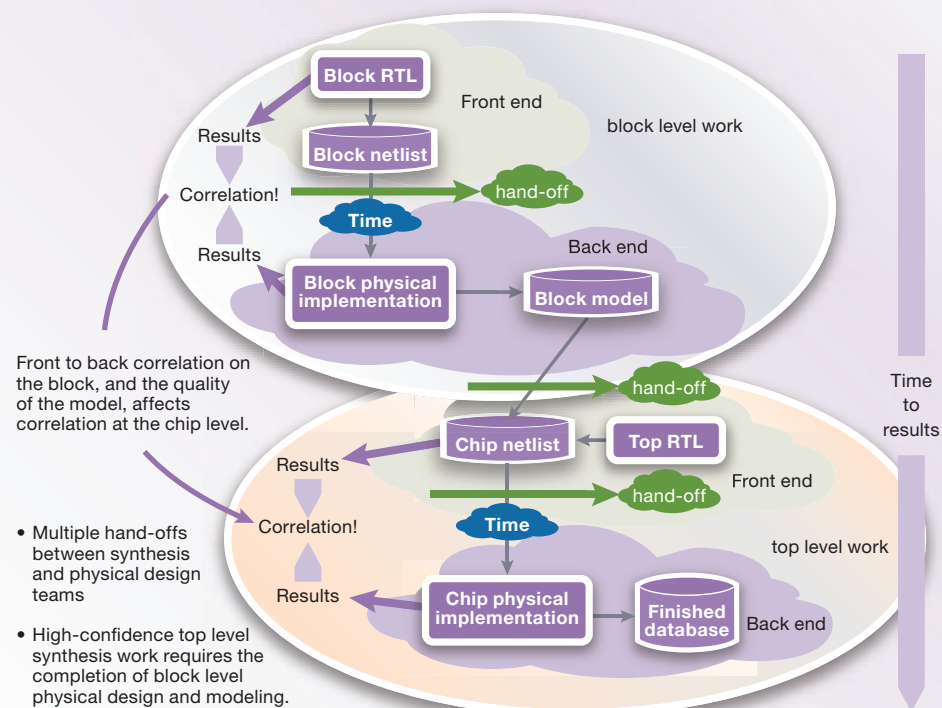
Spiral Flow Diagram

Spiral Design Flow and Successive Refinement



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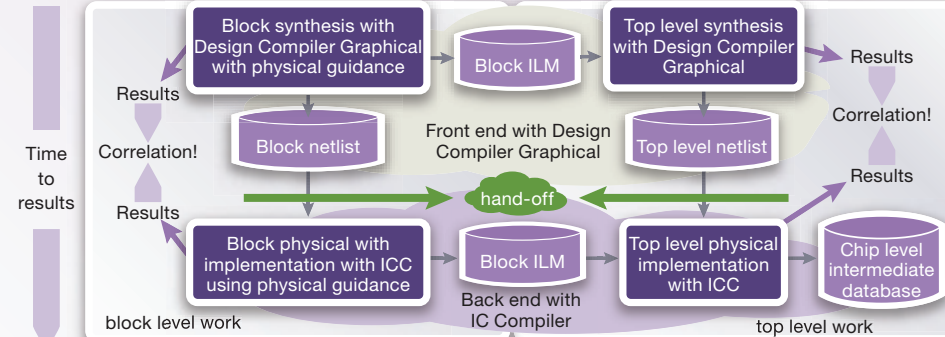
Traditional Generic Hierarchical Design Data Flow



Front to back correlation on the block, and the quality of the model, affects correlation at the chip level.

- Multiple hand-offs between synthesis and physical design teams
- High-confidence top level synthesis work requires the completion of block level physical design and modeling.

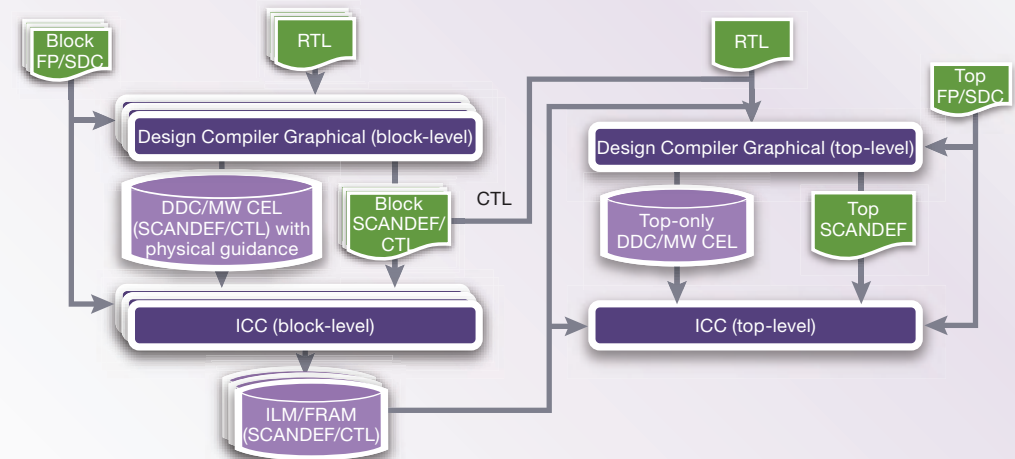
Design Compiler Graphical, IC Compiler Hierarchical Flow with Physical Guidance at the Block Level



Used for early and mid-term refinement in the spiral cycle

- Due to tight correlation at the block level using physical guidance, the block model from Design Compiler® Graphical can be used for high confidence top level synthesis.
- Excellent chip-level correlation and confidence based on highly accurate block model
- Early to mid-design cycle top level synthesis with high-confidence block models is not paced by block level physical implementation. Associated hand-offs eliminated.
- Time to results in evaluating mid-term refinement significantly reduced
- Early and mid-design cycle block and top level physical implementation can be parallelized with higher confidence leading to reduction in overall time to results.

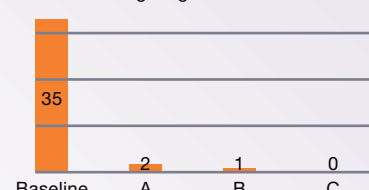
Design Compiler Graphical, IC Compiler Hierarchical Flow with Physical Guidance at the Block and Top Level



Used for later-term and final refinement in the spiral cycle

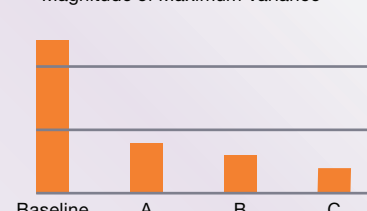
- Optimal correlation achieved by employing Physical Guidance at the block and top levels

Number of Path Groups Exceeding Targeted Tolerance



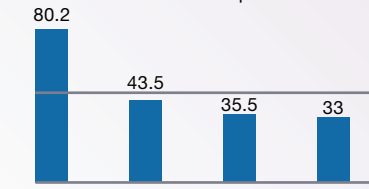
Correlation

Magnitude of Maximum Variance

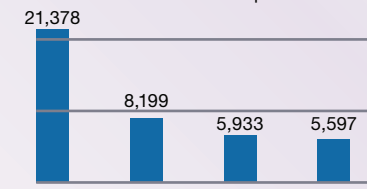


Quality of Results

Sum of all Path Groups WNS



Sum of all Path Groups TNS



Legend:

- A - Physical Guidance employed at top level. ICC ILMs used
- B - Physical Guidance employed at top and block levels. ICC ILMs used.
- C - Physical Guidance employed at top and block levels. Tool-specific ILMs used

Results

- All 412 path groups within the targeted tolerance!
- 90MHz Maximum improvement in frequency (118MHz to 208MHz)!
- 49% improvement in frequency on critical path groups (154MHz to 230MHz)!
- TNS reduced by 73%
- Top level run time reduced by 37%
- Significant reduction in Time to Results

Hierarchical Design Best Practices

- Forward annotation of front-end virtual placement information to guide physical design
- Refine timing budgets as block-level information is refined and spiral flow proceeds
- Ensure common constraints between front and back end
 - Parasitic estimation details,
 - Timing derating
 - DEF cell instantiation
 - Common handling of blockages between front and back end