

POST LAYOUT VERIFICATION OF AMS DESIGNS AT 28NM



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Abstract

The design of analog mixed signal (AMS) circuits in the sub 45nm technologies becomes more complicated due to layout dependent effects e.g. stress engineering. To ensure first-time right silicon ([1][2]) thorough postlayout verification is required. This becomes easily prohibitive for larger AMS designs due to required simulation effort. A mixed configuration simulation strategy in a subdivided AMS postlayout verification flow is proposed, carefully balancing simulation speed and accuracy. Results from a real design implemented at 28nm are showing that post layout verification can be speed up substantially improving the turn around time of the AMS design flow.

AMS Design Challenges at 28nm

Stress engineering such as embedded SiGe [3], dual stress liners [4] [5] and stress memorization techniques [3] have been introduced to improve the performance of devices. These effect depend highly on the layout and need to be taken into account during layout creation and verification [6]

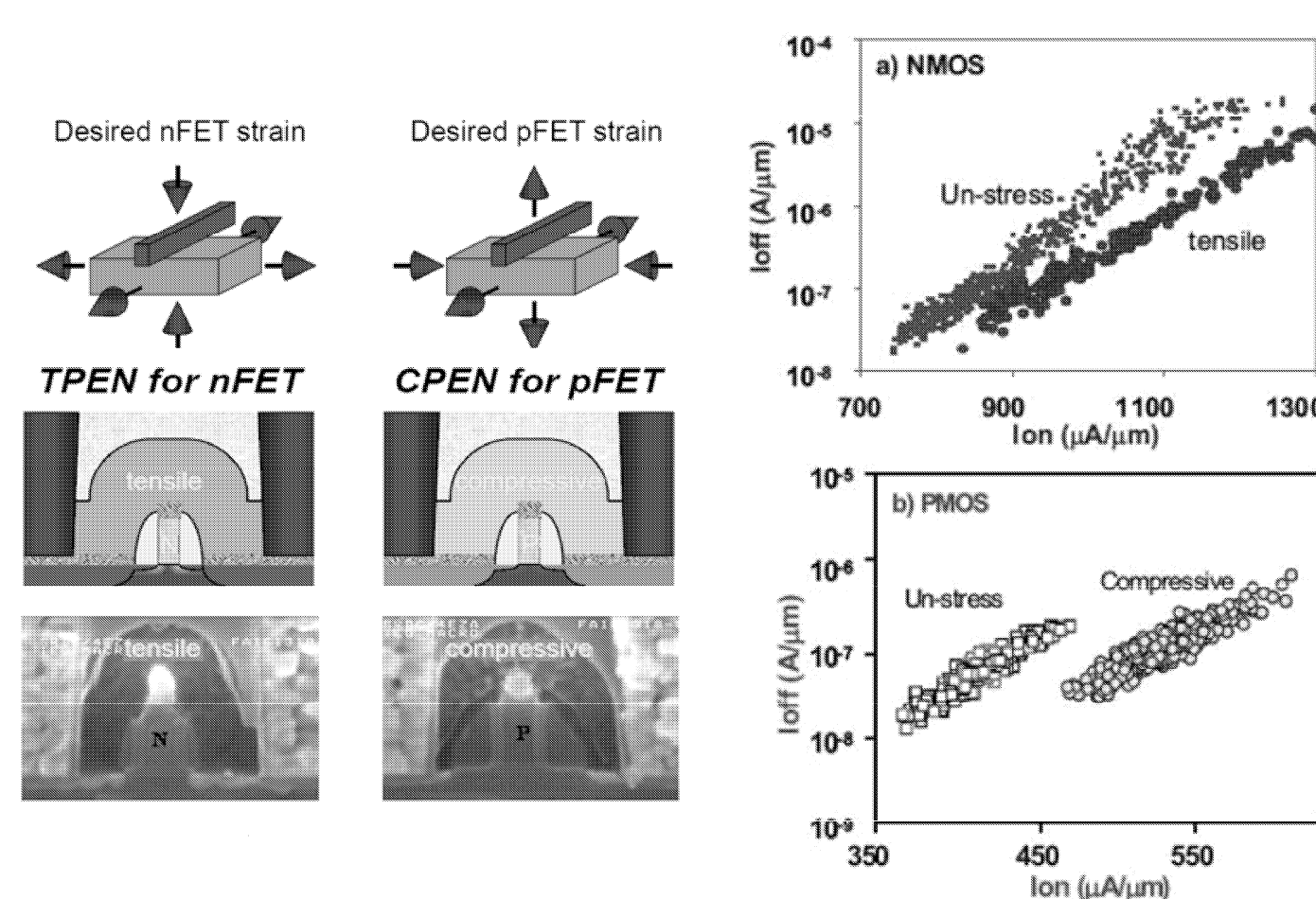


FIGURE 1: Performance Improvement due to Dual Stress Liners

Variations in I_{on} current of up to 11% and 20% for NMOS and PMOS respectively in addition to several 10th of mV threshold voltage shift depending on layout conditions have been reported [3] [7].

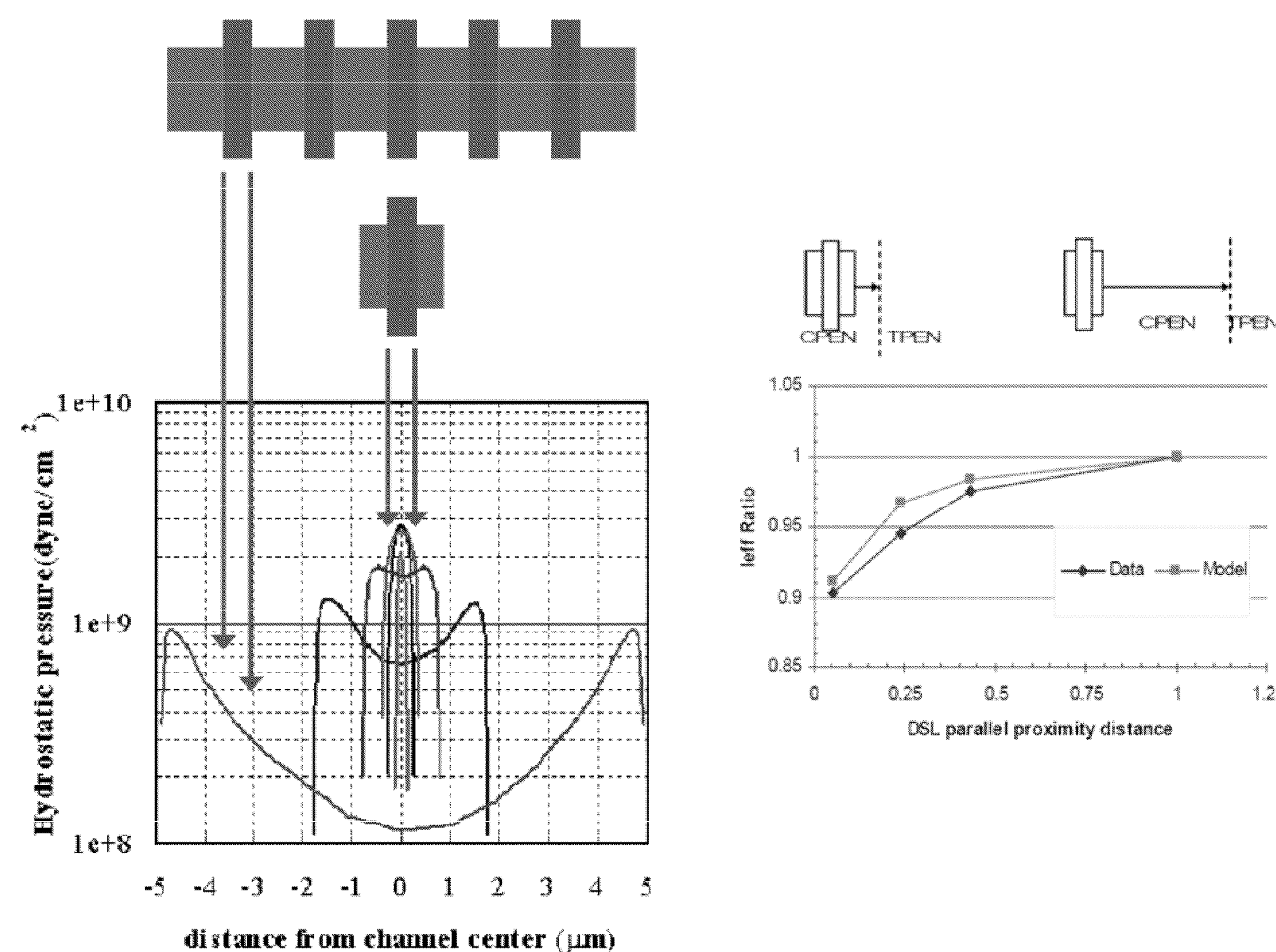


FIGURE 2: Mechanical Stress depending on dimension of active area and position of gate finger [7]

Design Verification Flow using EVS

The flow follows the commonly used flow comprising of the step schematic driven layout (SDL) and verification. However, the post layout verification is split into the steps *verification using simple extracted view* containing D devices only and *verification using extracted view* comprising of D devices and RC parasitics.

During *schematic verification* the design under test will be simulated using schematic and potentially Verilog-A views.

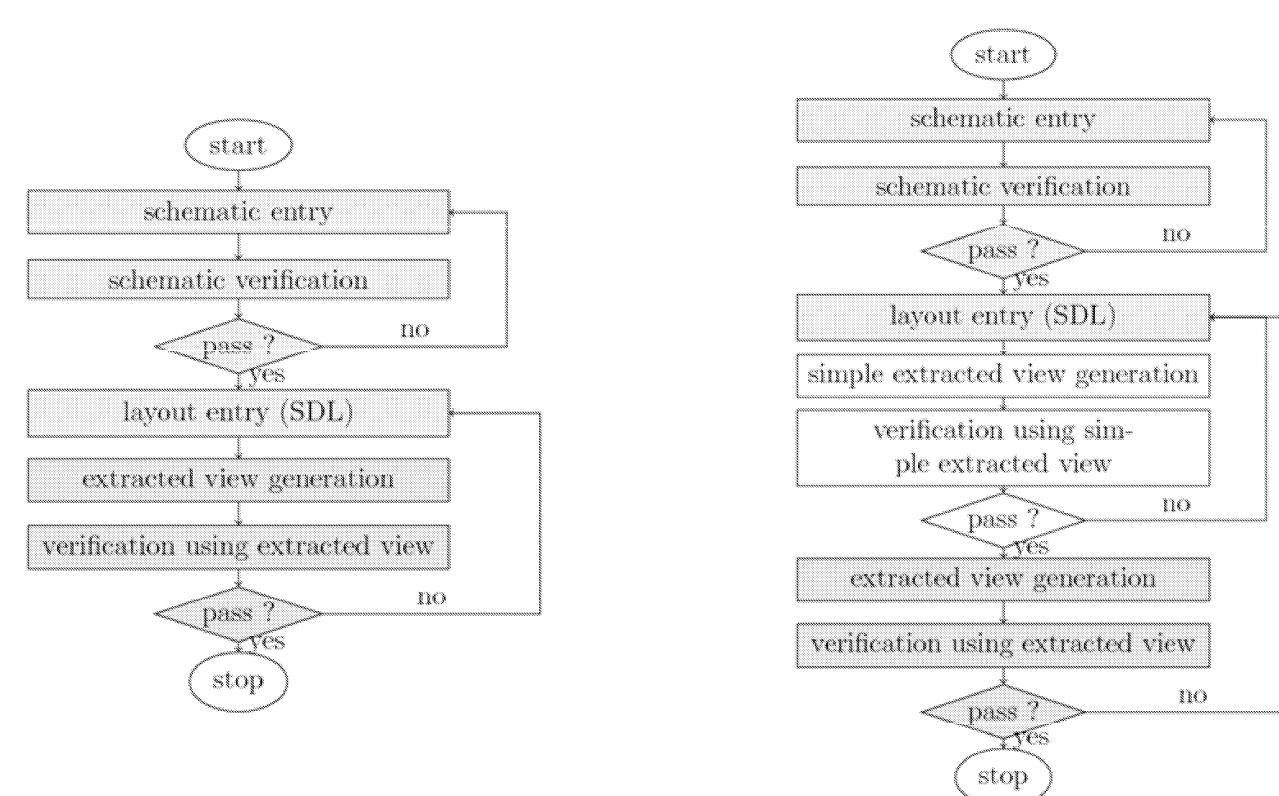


FIGURE 3: Comparison of traditional SDL flow with Post Layout Verification and extended Post Layout Verification

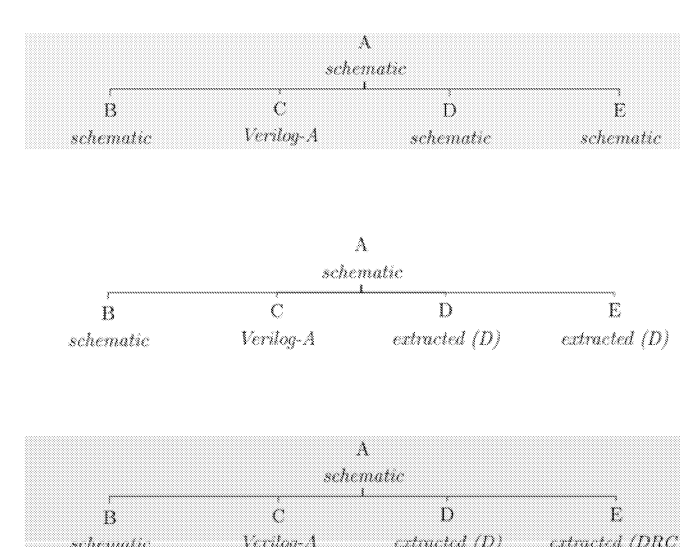


FIGURE 4: Combination of different views during the various verification steps.

Design Example VCO

The new SDLverification flow has been used verifying a VCO part of a PLL designed in 28nm.

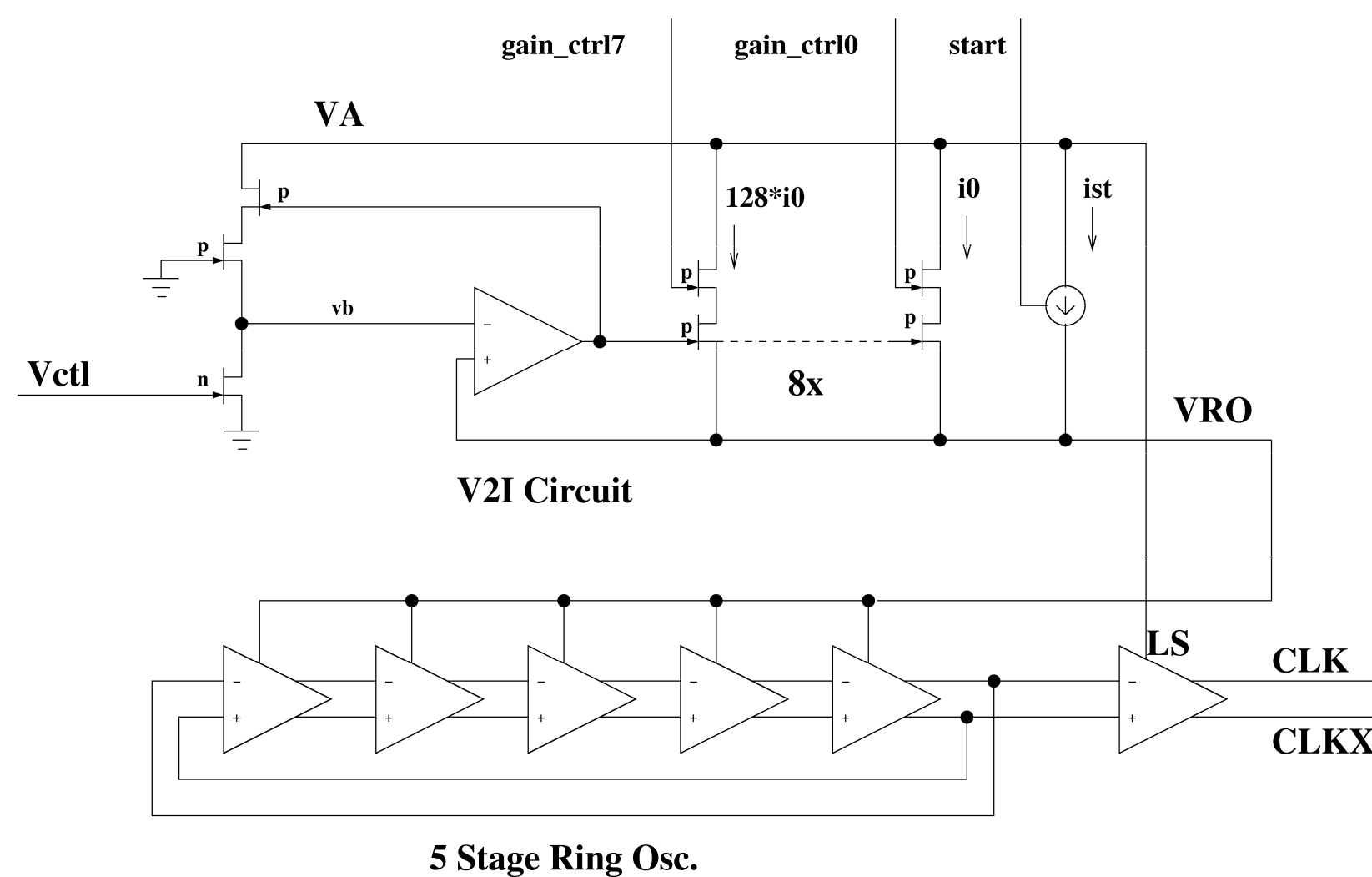


FIGURE 5: VCO block diagramm

The blocks **v2i** and **i2i** are supplying current to **ro** and are working in a quasi DC mode such that parasitics can be ignored. The current provided

by **v2i** and **i2i** depends strongly on the performance of the MOS transistors and hence on stress effects. In contrast to this, the frequency of the **ro** block depends on parasitics RC's and on the transistors.

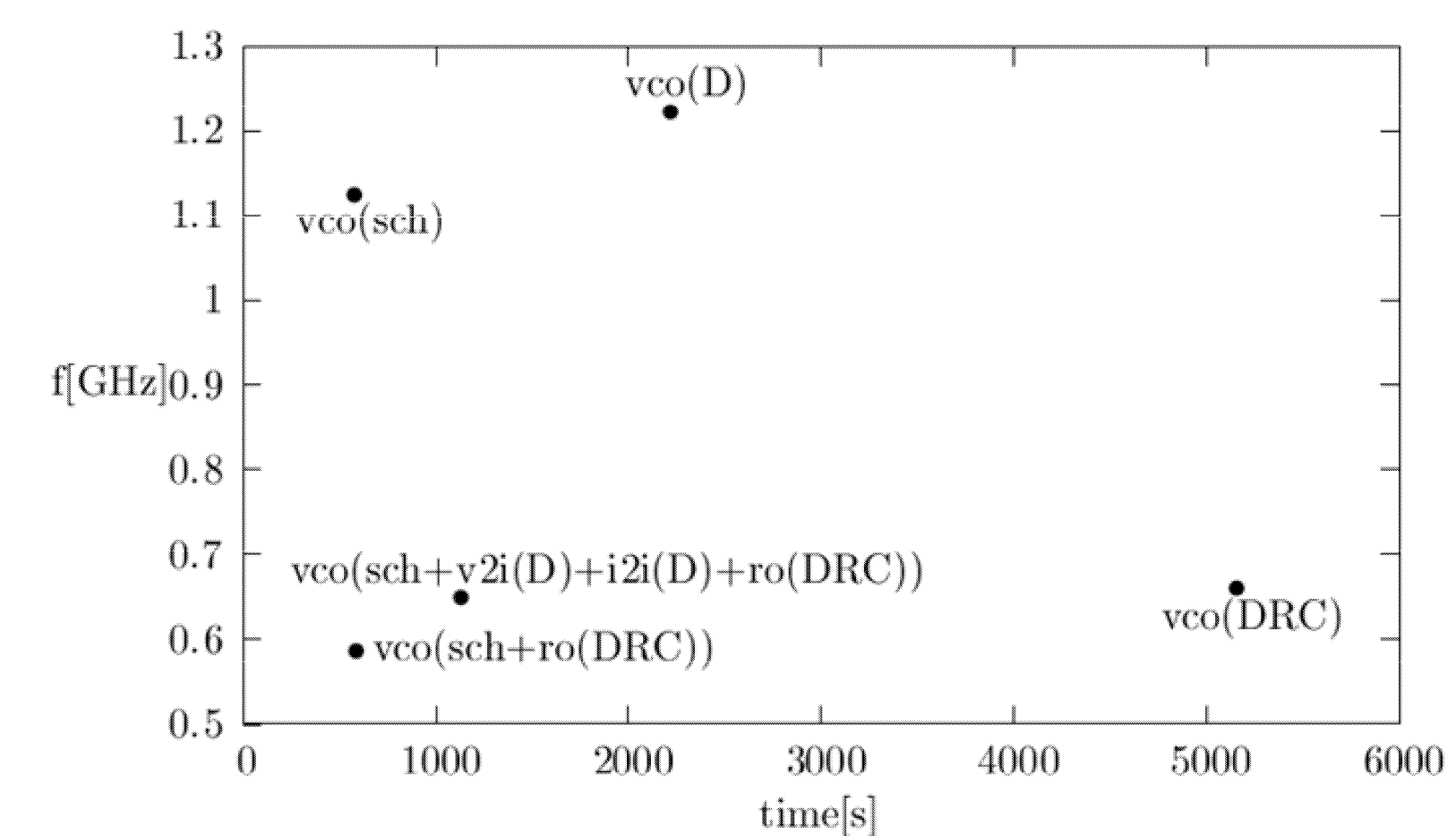


FIGURE 6: Runtime of simulation for one combination of $[Vctl, gain_{ctrl} < 7 : 0 >]$ versus simulated frequency for various extracted view combinations.

Main results from the comparison are:

- $f(CLK) = 1.12GHz$ for **vco(sch)**, 584s simulation time
- $f(CLK) = 1.22GHz$ for **vco(D)**, 2224s simulation time
- $f(CLK) = 0.66GHz$ for **vco(DRC)**, 5156s simulation time
- $f(CLK) = 0.65GHz$ for **vco(sch+v2i(D)+i2i(D)+ro(DRC))**, 1135s simulation time
- Only 22% of simulation time were needed to obtain $f(CLK)$ with an error less than 2%

Limitations

In this analysis we have neglected potential correlations between blocks due to layout effects and parasitics, which can impact the accuracy. Also top level block routing has not been taken into account, here hierarchical extraction could allow to incorporate those parasitics as well.

Conclusion

Despite the introduction of an additional verification step to assess the layout dependent impact of stress on design performance the overall turn around time has been reduced by about 30%. The use of extracted views together with simple extracted views during final post layout verification is reducing the complexity of the simulation compared to a verification using flat extracted netlists.

References

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