

Improving post-layout simulation flow accuracy and productivity

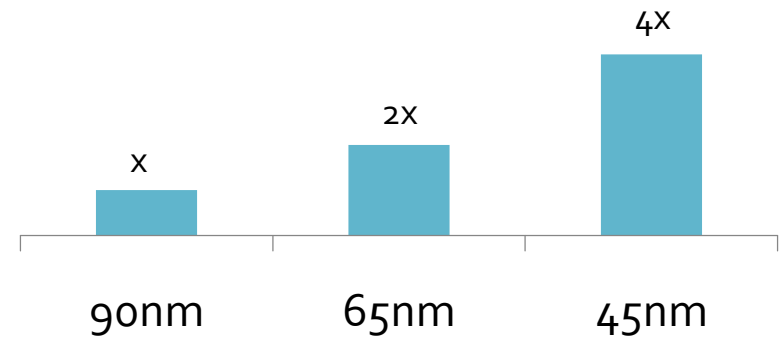
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What is changing?

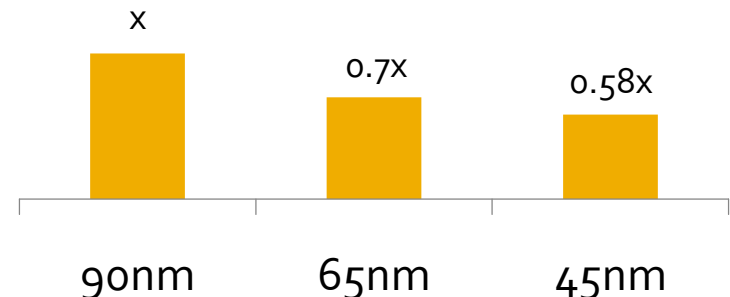
- Process
 - Design size is shrinking
 - Contact Resistance
 - Close interaction between device layers
- Impacts
 - Resistor device parasitics
 - MOS device parasitics
 - Handling substrate/well contacts
 - MOS device parameters

Post layout Simulation flow needs to handle these challenges

Contact Resistance

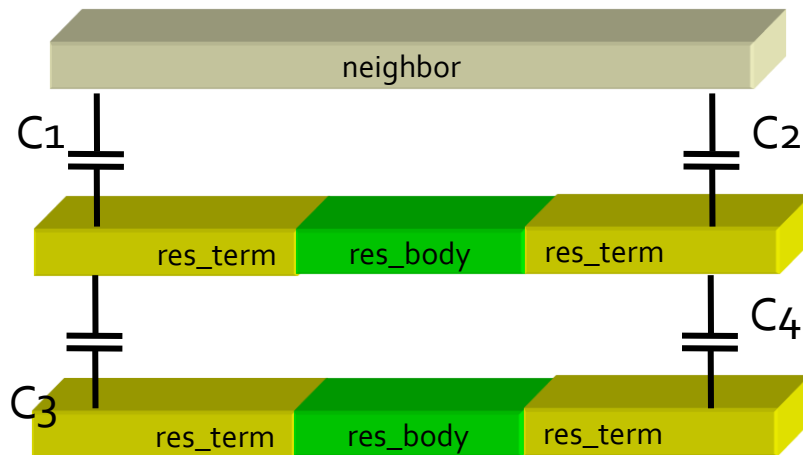


Gate Contact Spacing



*source: Synopsys

Effect of Resistor



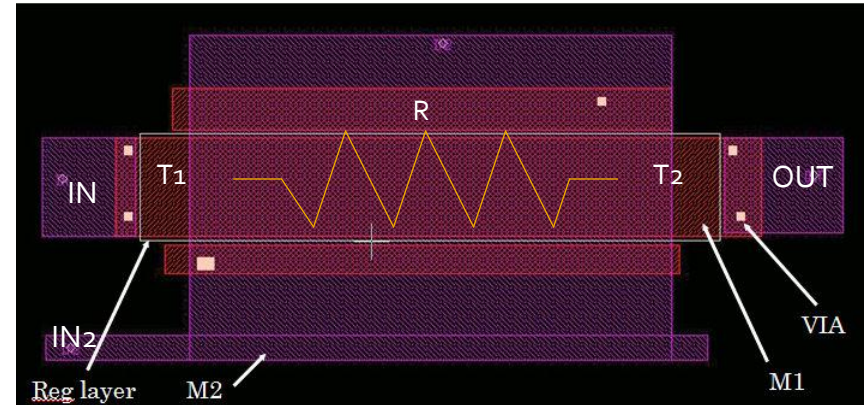
- Resistor banks common in Analog design
- Resistor body capacitance
 - Context specific - Function of neighboring conductors and other resistors in the resistor bank
 - May not be modeled accurately in spice models
- Extraction tools
 - Extract capacitance but ground the capacitance
 - Do not extract resistor body to resistor body capacitance

Challenges in Resistor Device Parasitics

- Resistor body does not connect to any net
 - No net property
- The capacitance associated with resistor body cannot be associated to one terminal
 - Needs to distributed correctly
- Handling capacitance between resistor bodies in resistor banks
 - Not is spice models
- Handling capacitance of resistor body to ground
 - If not present in spice models

Handling Designed Resistor terminals

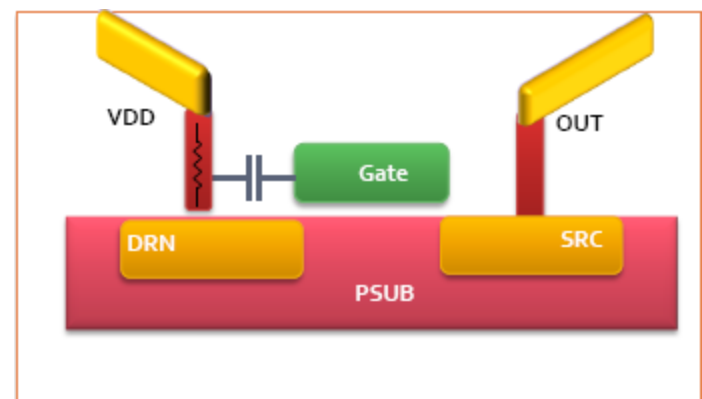
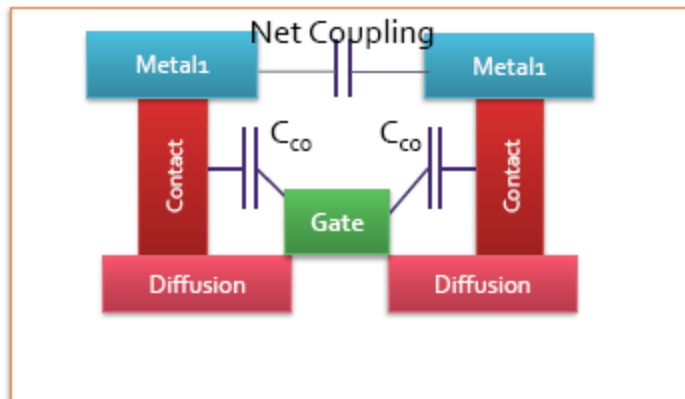
- Treat Resistor body as a special net
- Ensure resistor body does not short two terminals
- Split resistor body and connect one to each terminal



	Without Resistor Parasitics	With resistor Parasitics
Total Cap IN	0.5ff	2.9ff
Total Cap OUT	0.57ff	2.9ff
Total Cap of IN2	7.1ff	7.1ff
Coupling IN2-IN	0.12ff	2.08ff
Coupling IN2 - OUT	0.081ff	2.03ff

Contact Capacitance and Resistance

- Gate-contact capacitance has a pronounced impact on device performance
- SPICE model does not include gate to contact capacitance
- Extraction tools either grounds or retains all coupling caps, including gate to contact coupling
- Power net extraction and simulation is expensive!
- Device parasitics are layout dependent
 - SPICE model introduces approximation
 - SPICE model may not include contact, gate and diffusion resistance
- Contact resistance and gate-contact coupling are key contributors to device performance



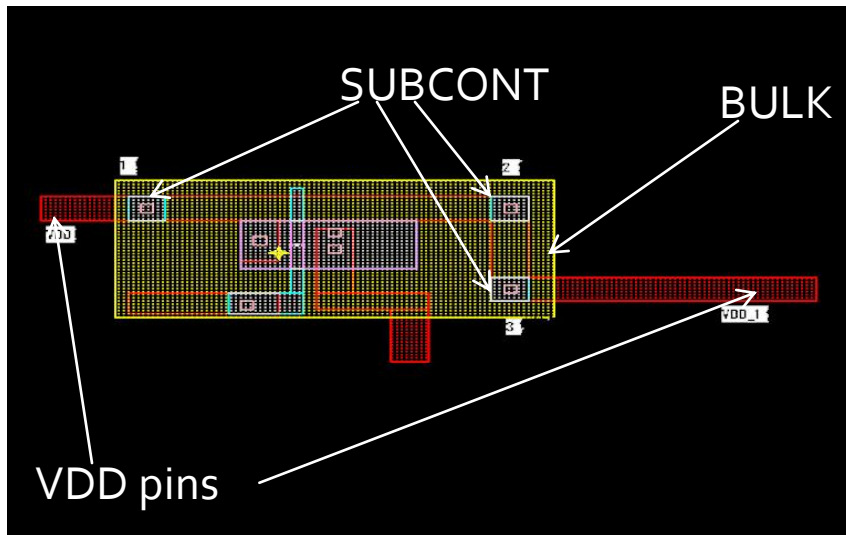
Results of Selective Device Parasitics



	Digital Cell (Buffer Chain)	
	Simulation Runtime (Secs)	Delay (ps)
With complete power net parasitics	145	168
With only power net contact parasitics	18	166
Gain/error	8X	~1.2%

Accelerates Simulation, Maintains Accuracy

Multiple SUBCONT on Bulk layer



Ideal bulk layer connections leads to shorting of Power network parasitics

- Preserve point to point metal resistance
- Prevent shorting due to ideal substrate
- Ensure isolated wells have correct IR drop

Past and Proposed approach

PAST APPROACH

- Substrate extraction
 - Increases Netlist size
 - Bottle-neck for simulation tools
- Extraction without Bulk layers
 - Devices bulks will have ideal voltage
- Use high resistance value for substrate contact to limit current through substrate
 - Fine for small blocks
 - As the number of parallel contacts increases the effective resistance decreases

PROPOSED APPROACH

- Select one substrate contact per well
 - Each isolated well will have unique substrate contact
- Ensures no increase in netlist size
- Comprehends voltage for each set of devices in a well

Resistance without well	Resistance with ideal well	Resistance with current solution
4.0816 ohms	0.002 ohm	4.0816 ohms

Challenges with MOS Device Properties

DEVICE EXTRACTION & LVS

- Device terminals are assigned by PV tools
- Device terminals assignment is not based on schematic connectivity
- Leads to different terminal assignments between schematic and layout
- Most PV tools treat DRN/SRN are swappable in LVS step to complete LVS check

DEVICE PROPERTY EXTRACTION

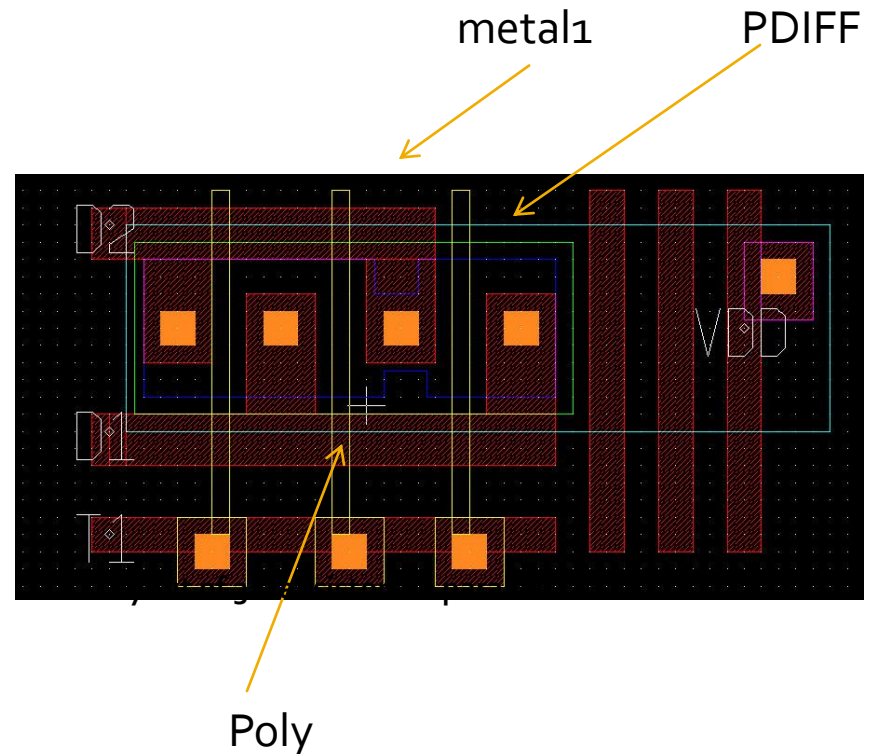
- Property names may not have relationship to terminal names
 - String match cannot be used as technique
 - Hard coded heuristics would require customer specific code enhancements
- Property extraction may be encrypted
 - One cannot parse rule file to determine terminal/property name association
- All device properties are not associated with terminals
 - Like SA, SB, WPE & PSE properties etc

An example

SCHEMATIC NETLIST

- SUBCKT check_float VDD
T1 D1 D2
- M1 D1 T1 D2 VDD P
L=0.08u W=0.64u
- M2 D1 T1 D2 VDD P
L=0.08u W=0.64u
- M3 D1 T1 D2 VDD P
L=0.08u W=0.64u
- .ENDS

LAYOUT



Results with ability to control property swapping

WRONG DEVICE PARAMETERS

- MM2 M2:D M2:G M2:S
VDD p AD=0.1536p
AS=0.1256p L=0.08u
PD=1.12u PS=1.4u
W=0.64u **pd2=1.4e-06**
ps2=1.12e-06

CORRECT DEVICE PARAMETERS

- MM2 M2:D M2:G M2:S
VDD p AD=0.1536p
AS=0.1256p L=0.08u
PD=1.12u PS=1.4u
W=0.64u **pd2=1.12e-06**
ps2=1.4e-06

**Associating correct property value to a terminal is key
to accurate post layout simulation**

Summary

- An efficient Post Layout Simulation flow has been presented that handles
 - Resistor device parasitics
 - MOS diffusion contact parasitics extraction
 - Substrate tap extraction
 - MOS property extraction with cross reference
- Multiple examples have been presented to illustrate the benefits