

A novel **configuration and communication interface infrastructure** for custom design prototype system is proposed. Based on a **set of basic design guidelines** that are typically easy to be met, the custom design prototype system could be adopted for more advanced verification methodologies, such as **co-simulation**, **co-emulation**, **scalable RTL-level signal probing** and **full RTL visibility debugging**. Implementation and integration of the proposed solution to several industrial custom design prototype systems have shown this could be done with small design and integration effort while achieving greater verification methodological flexibility and efficiency. One major verification methodological advantage of this approach is the capability of moving the usage of custom design prototype system forward in the design flow from towards the end to **early stage of the design verification cycle** to greatly increase verification efficiency.

Industrial chip design verification challeng

Simulators are too slow for system validation.

Emulators are too expensive for broad deployment.

← - - - - - **Prototype** systems do not have good visibility. late stage

Design cycle early stage

Block level RTL design

Integration validation

system validation

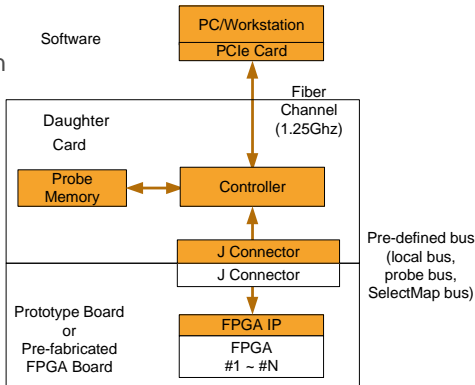
software/firmware development

Prototype System Controllability and Visibility Enhancement Infrastructure Architecture

Local bus
For co-emulation
/ co-simulation

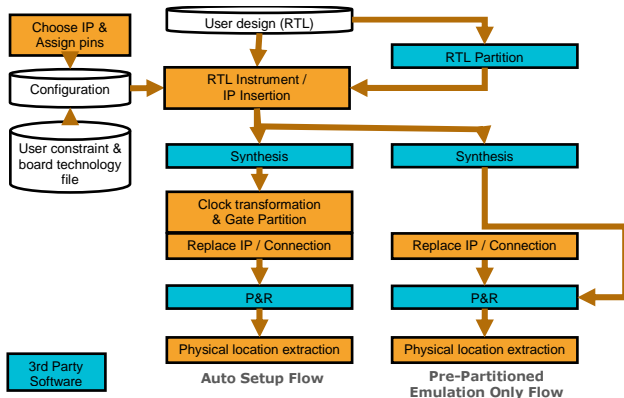
Probe bus
For built-in
probes

SelectMap bus
For dumping
FPGA internal
states

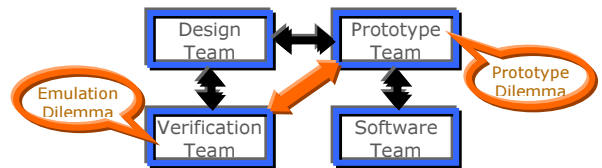


	Emulation	Co-Simulation	Co-Emulation
TB Simulation Capability	None	Major simulators	C-API; SCE-MI 1.1 and 2.0 DPI; Synthesizable transactor
Extra Auto Setup Functions	None	TB ext ref/force/release; Generate wrapper	RTL instrument; Clock synch; Generate wrapper
Extra Runtime Functions by using SelectMap Bus	FPGA download; memory init and read-back	FPGA download; memory init and read-back	FPGA download; memory init and read-back
Debug	Probe	Full Visibility	Full Visibility, Probe
Speedup	Near real time	5x to 10x	1000x

Prototype System Design Instrumentation Implementation flow



Enhanced Prototype System Based Verification Methodology



Enables verification team to use prototype board
- Enhanced visibility and controllability
- Verification for Design module/IP: 2M-10M gate
- Verification for design revision



Prototype system Infrastructure Hardware Implementation

