

Jens Harnisch,  
Albrecht Mayer  
Robert Schwencker

Infineon Technologies AG  
Munich, Germany

Kesavan Prasanna,  
Sasidharan Prasanth

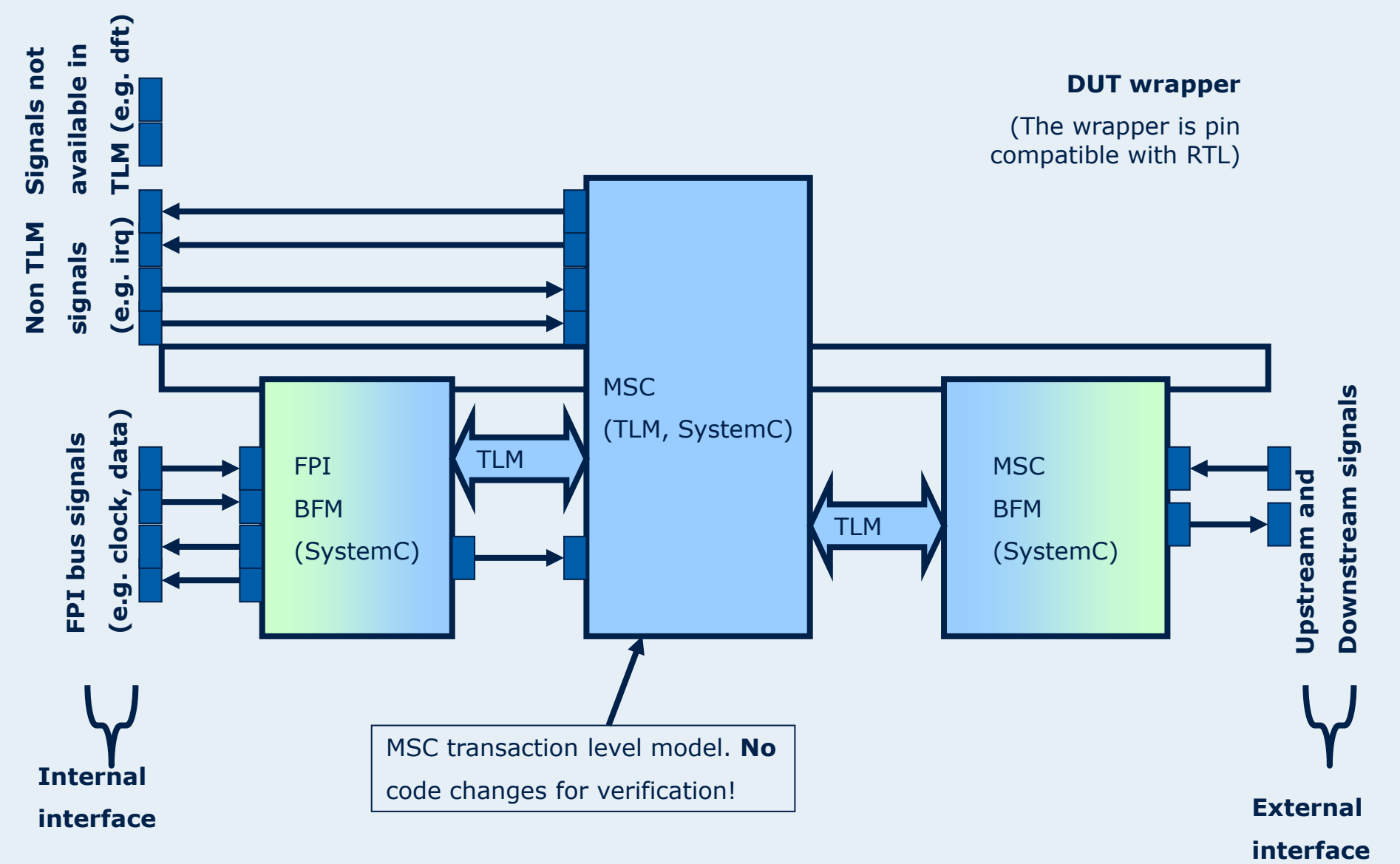
Infineon Technologies India  
Bangalore, India

Diamantino Goncalves

Infineon Technologies U.K. Ltd.,  
Bristol, U.K.

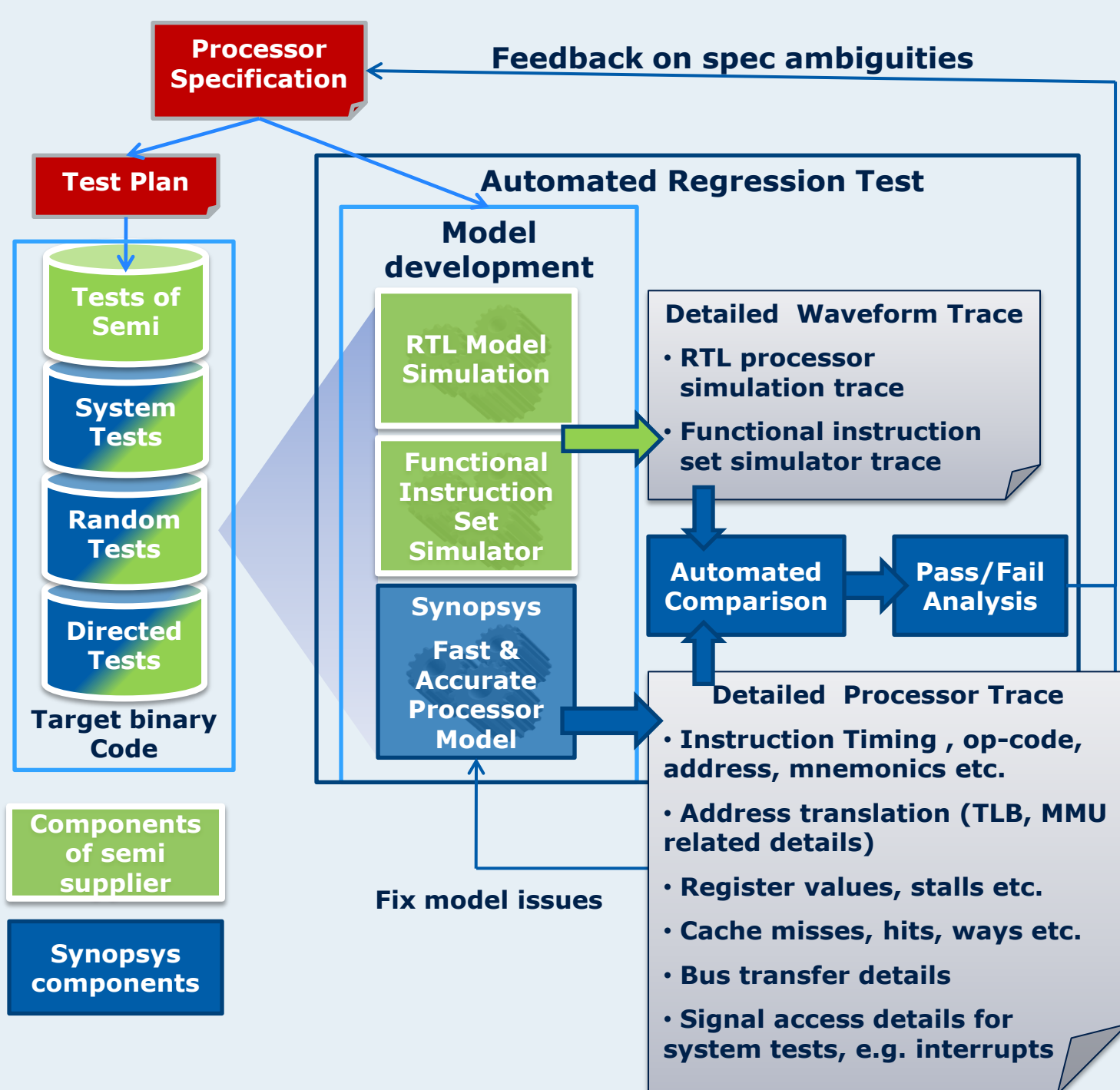
- Objectives:
  - Virtual prototype of microcontroller with near 100% functionality
  - Timing accuracy higher than 90%
  - Simulation performance >1 MIPS
- Challenges:
  - Matching RTL with TLM abstraction level in verification
- Approach:
  - Automated verification flow with reuse of RTL tests and additional directed tests
- Results:
  - Timing accuracy for the applied system test cases higher than 90%,
  - VP running at more than 1 MIPS even for complex scenarios, and for several scenarios much faster
- Learning's:
  - White box RTL tests should be avoided, because they can usually not be reused for virtual prototypes
  - The VP needs to be refined based upon complex customer use cases, automatic regression tests are absolutely mandatory
  - Standard waveform comparison available in digital simulators is too inflexible due to different clock models (toggling signal vs. simple time value). In-house tooling was used. Small differences between TLM and RTL cannot be avoided. TLM does not provide a natural synchronization point like the clock edge.

## Automated Peripheral Model Verification



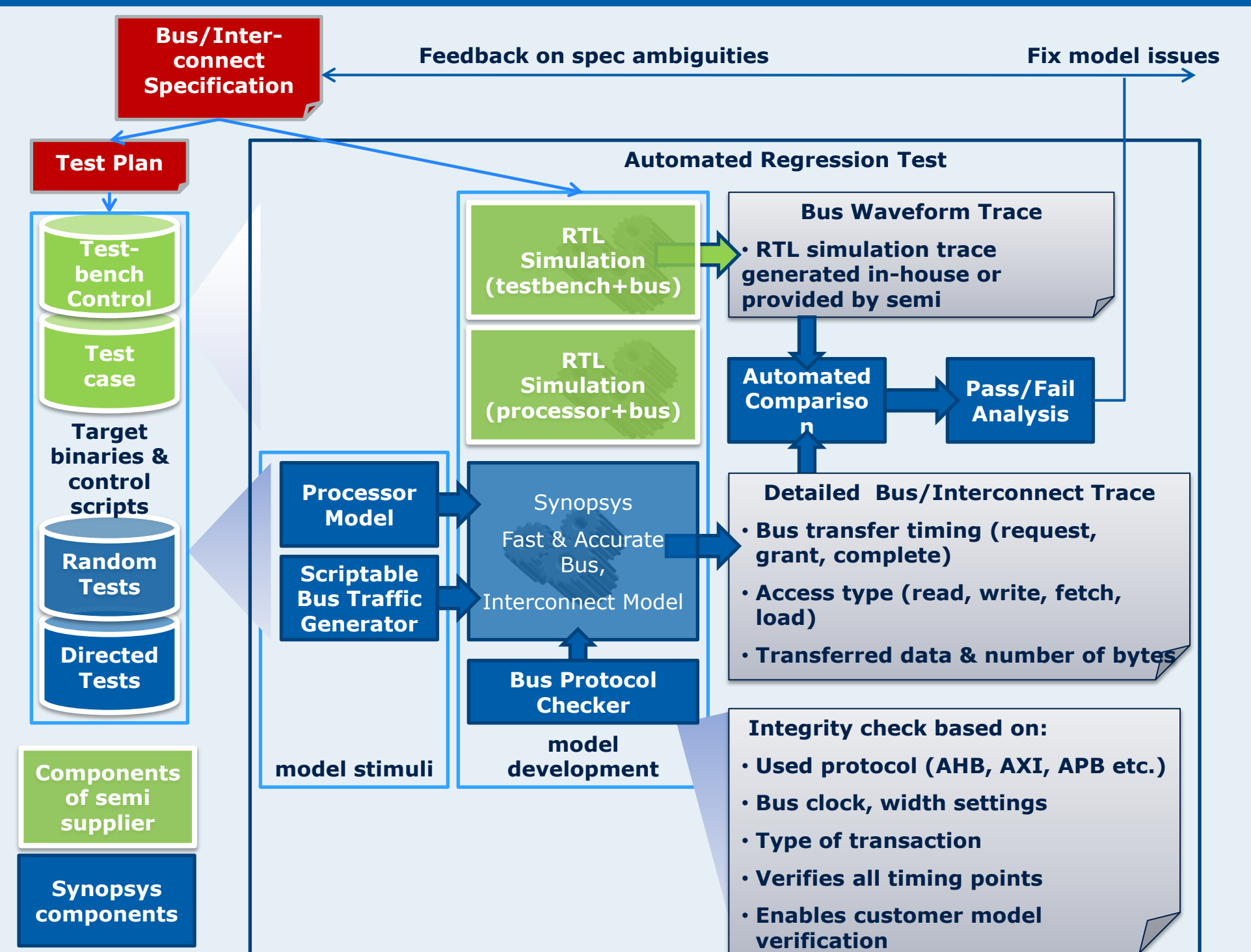
- Bus functional models (BFMs) translate the transaction-level interfaces between TLM and RTL. Embedding TLM inside RTL translates from a high abstraction level to a lower transaction level. Thus for the BFM this partly means inventing details that are not available within TLM.
- Signal-level communication (e.g. clock) is translated in case of incompatible types. E.g. the clock on RTL side is provided as toggling clock whereas within TLM it is provided a clock-period value in order to speed up simulation.

## Automated Virtual Processor Model (VPM) Verification



- Virtual Processor Models (VPM) are verified with regards to functional and timing behavior.
- Maximum possible re-use of semi's components such as test cases, test vectors, reference waveforms, simulators and RTL simulations.
- Verbose VPM trace with detailed timing annotation of instructions, register loads cache events and interleaved bus transfers allow automated comparison to RTL.

## Automated Verification of Buses and Interconnects



- Timing of TLM bus and interconnect models are verified against the semi's reference simulator.
- Scriptable traffic generators are used for automated random & directed tests
- Verbose timing annotated bus trace allows automated comparison to RTL.
- An integrated protocol checker validates all timing points and can be re-used for user models.