

ESD verification challenges in deep sub-micron design SOC's

- Introduction to ESD failure mechanisms
- ESD verification flow for complex System On Chip designs:
 - Human Body Model/Machine Model ESD verification
 - Charge Device Model ESD verification
 - ESD verification in SOC implementation flow
- Floorplan optimization driven by ESD requirements
- Complex SOC 45nm design case study
- Summary and Conclusions

Introduction to ESD failure mechanisms

- Human Body Model:
 - The HBM testing model represents the discharge from the fingertip of a standing individual delivered to the device. It is modeled by a 100 pF capacitor discharged through a switching component and a 1.5KOhm series resistor into the component.

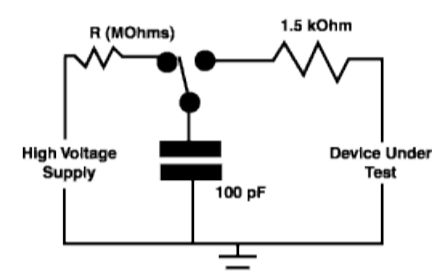


Figure 1: Typical Human Body Model Circuit

See: ESD Association standard *ESD STM5.1: Electrostatic Discharge Sensitivity Testing -- Human Body Model*.

- Machine Model:
 - A discharge similar to the HBM event which can occur from a charged conductive object, such as a metallic tool or fixture. This ESD model consists of a 200 pF capacitor discharged directly into a component with no series resistor. Figure 2 describes a typical DUT bench:

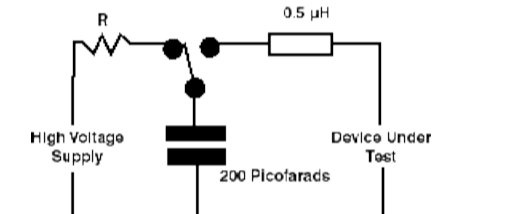


Figure 2: Typical Machine Model Circuit

See: ESD Association standard *ESD STM5.2: Electrostatic Discharge Sensitivity Testing -- Machine Model*

Introduction to ESD failure mechanisms

- Charge Device Discharge Model:

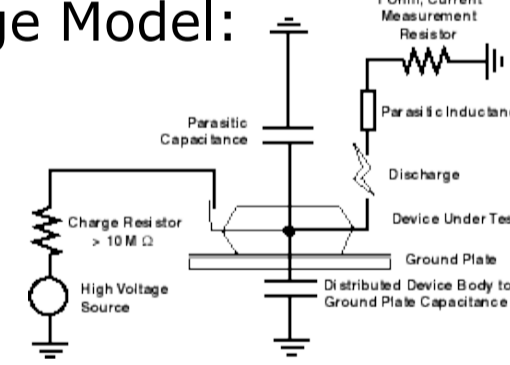
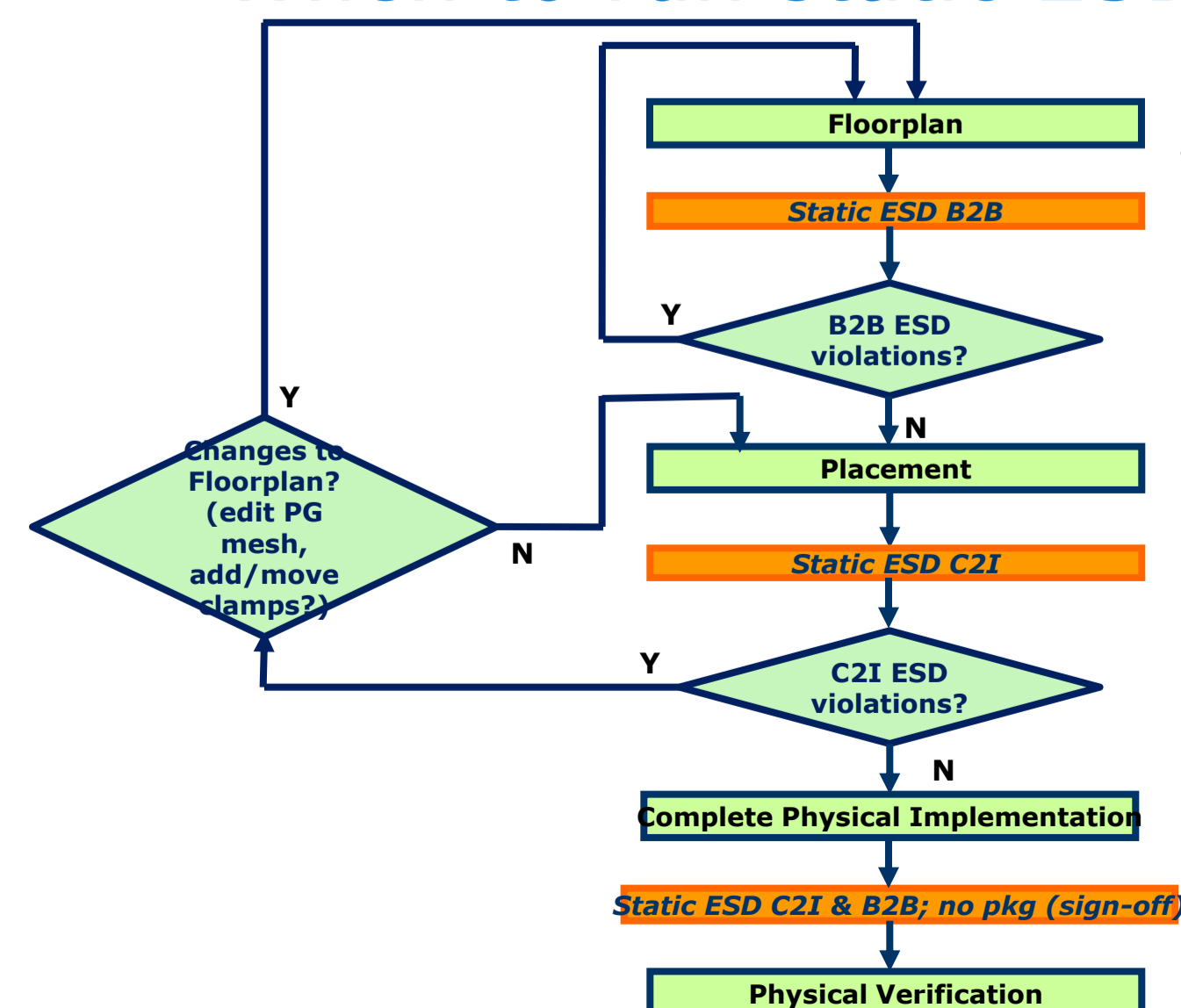


Figure 3: Charge Device Discharge Model Circuit

See: ESD Association standard *ESD STM5.3.1: Electrostatic Discharge Sensitivity Testing - Charged Device Model*

- The complexity of ESD protection implementation for modern System on Chip devices is driven by the increased number of independent power rails on the die and the complexity of digital and analog IP's which are integrated on the same die and require electrical isolation.

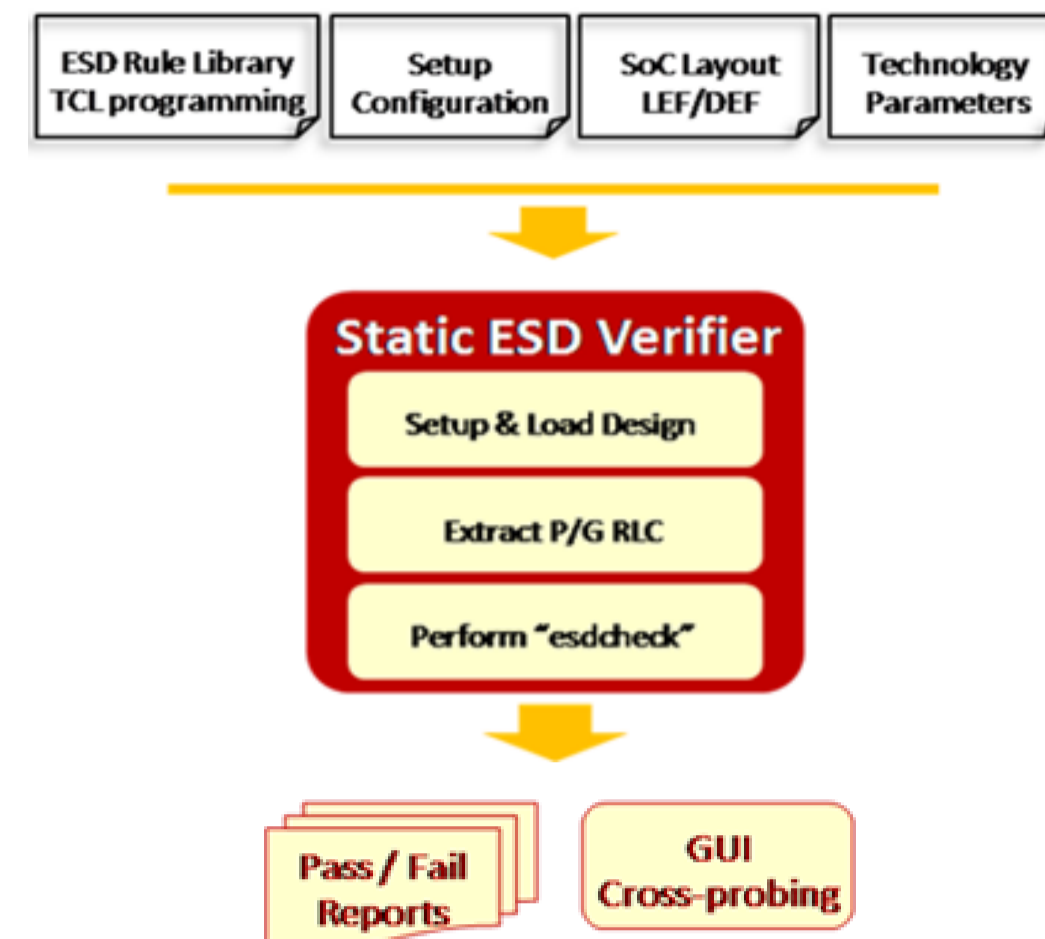
When to run static ESD analysis?



- In the floorplan stage we perform:
 - Block/region partition
 - PG mesh implementation
 - Bump placement and assignment
 - Clamps placement and connection
 - IO placement

- ESD verifications:
 - B2B: Bump 2 Bump (HBM/MM ESD check)
 - C2I : Clamp to instance (CDM ESD check)
 - Final sign off is performed without and with the package

ESD verification flow for complex System On Chip designs



- Provide Clamp file to get the clamp information
- Provide ESD Rule File to get the ESD analysis information
- LEF/DEF flow for the physical database
- Process technology file
- Package model if the analysis is performed with package

Static ESD Verifier Flow

HBM/MM Static ESD Verifier

- HBM/MM ESD events form discharge path between die/package pins and on-die protection devices
- Clamps connected in this path provides low-impedance bypass paths.
- HBM Static ESD verifier computes the effective resistance from bump-to-clamp-to-bump as shown in figure 1. Both individual path resistance as well as effective parallel path resistance is calculated.
- The input data requirement is shown in figure 2. Design related data (LEF/DEF) is required to setup design and perform PG grid resistance extraction.

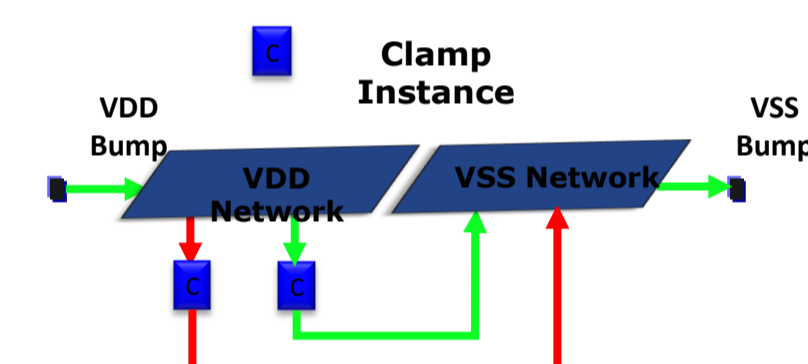


Figure 1 – HBM/MM ESD Check

- Design Related data
 - Technology Parameters
 - LEF/DEF Files
 - Power Domains
- ESD Rule Information
 - Rule Name, Type
- Thresholds (PARALLEL_R, LOOP_R)
- ESD Clamp Information
 - Node and Layer information

Figure 2 – Input Requirements

HBM/MM Static ESD Verifier

- Clamp and ESD analysis thresholds information is input to the flow
- Based on identified clamps and associated domains, connected bump-to-clamp-to-bump pairs are created as shown in figure 3.
- Resistance for each pair computed and compared against user thresholds

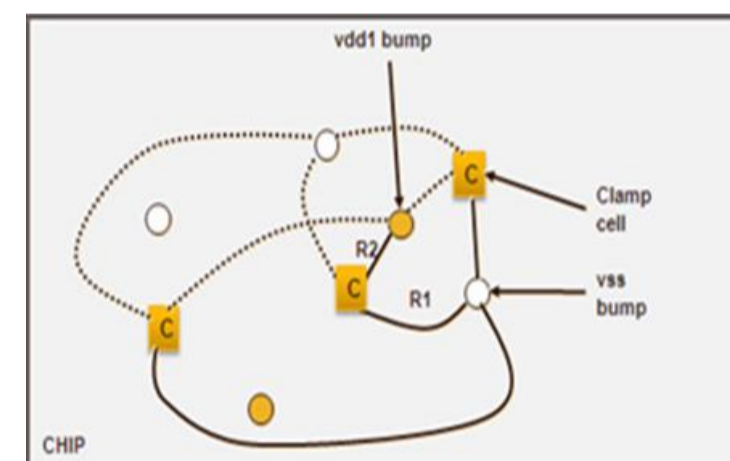
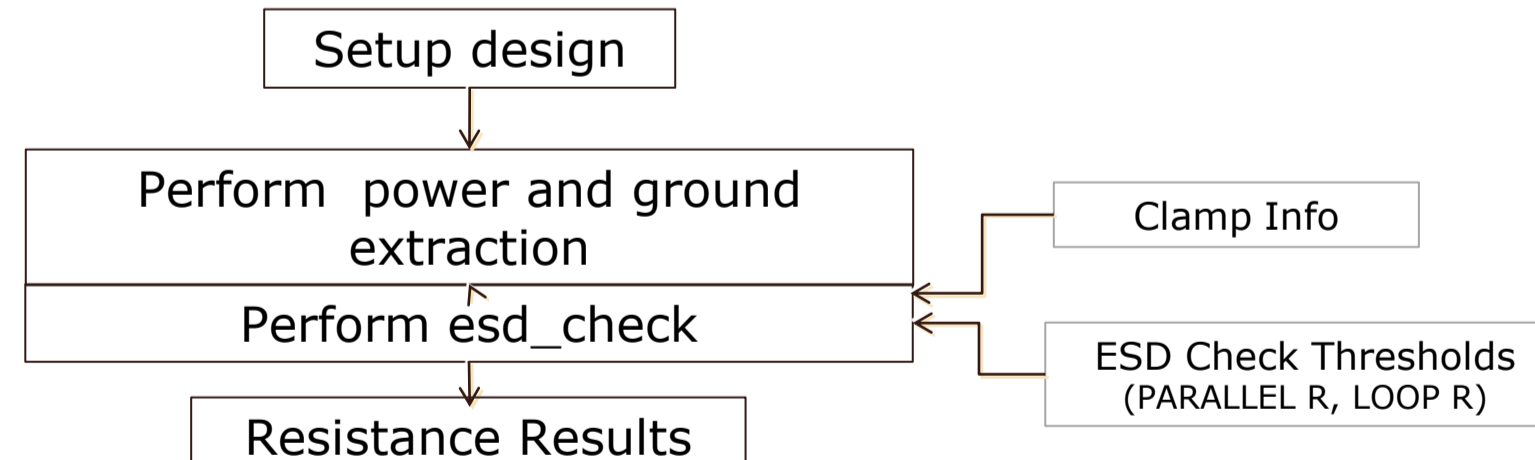


Figure 3 – HBM/MM ESD Flow



CDM Static ESD Verifier

- CDM ESD events form discharge path between on-die devices (accumulated static charge) and on-die protection devices.
- Clamps provides low impedance path to protect other devices from discharge event.
- CDM Static ESD verifier computes the effective resistance from logic instance/macro to clamp devices as shown in figure 4. Multiple clamp connections are also considered.
- The input data requirement is shown in figure 5. Design related data (LEF/DEF) is required to setup design and perform PG grid resistance extraction. The resistance is computed for input instances in instance list.

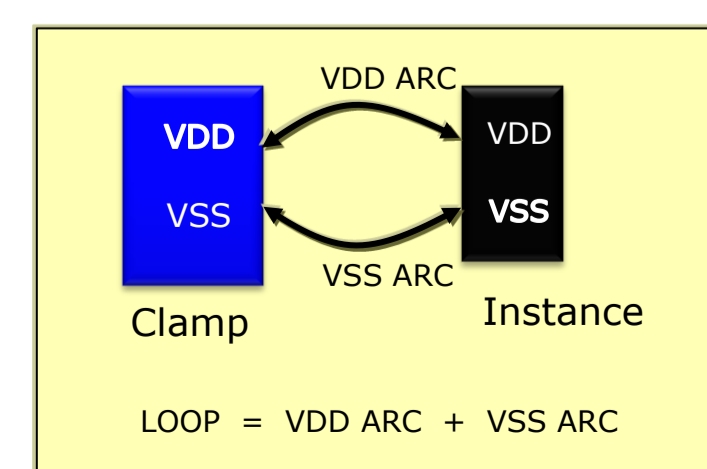


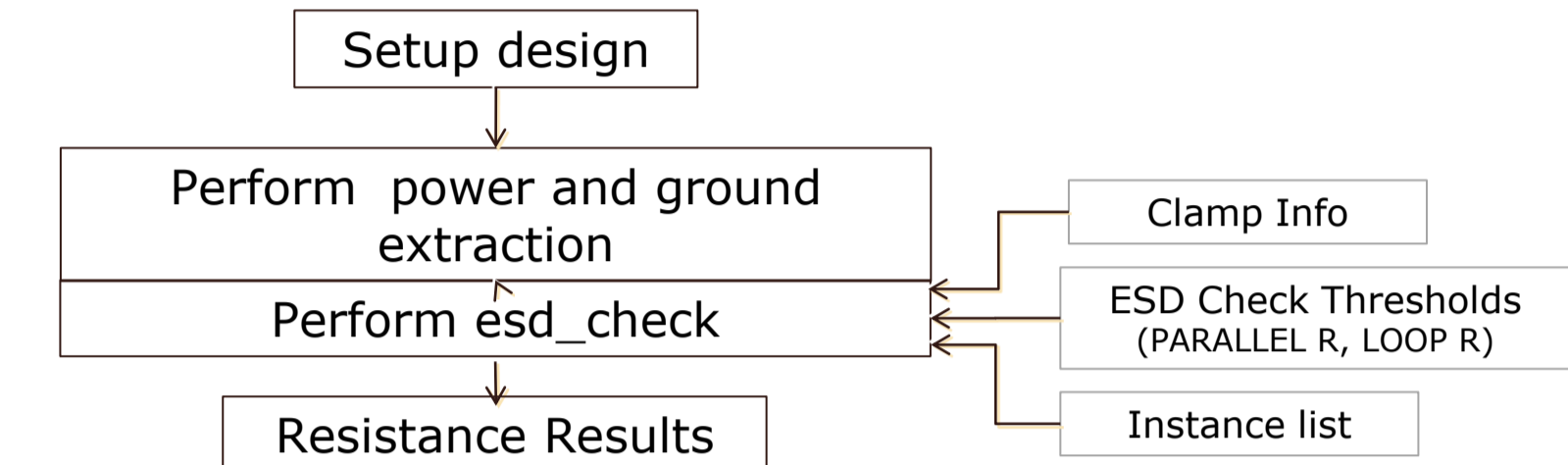
Figure 4 – CDM ESD Check

- Design Related data
 - Technology Parameters
 - LEF/DEF Files, Power Domains
- ESD Rule Information
 - Rule Name, Type
- Thresholds (ARC_R, LOOP_R)
 - Instance list.
- ESD Clamp Information
 - Node and Layer information

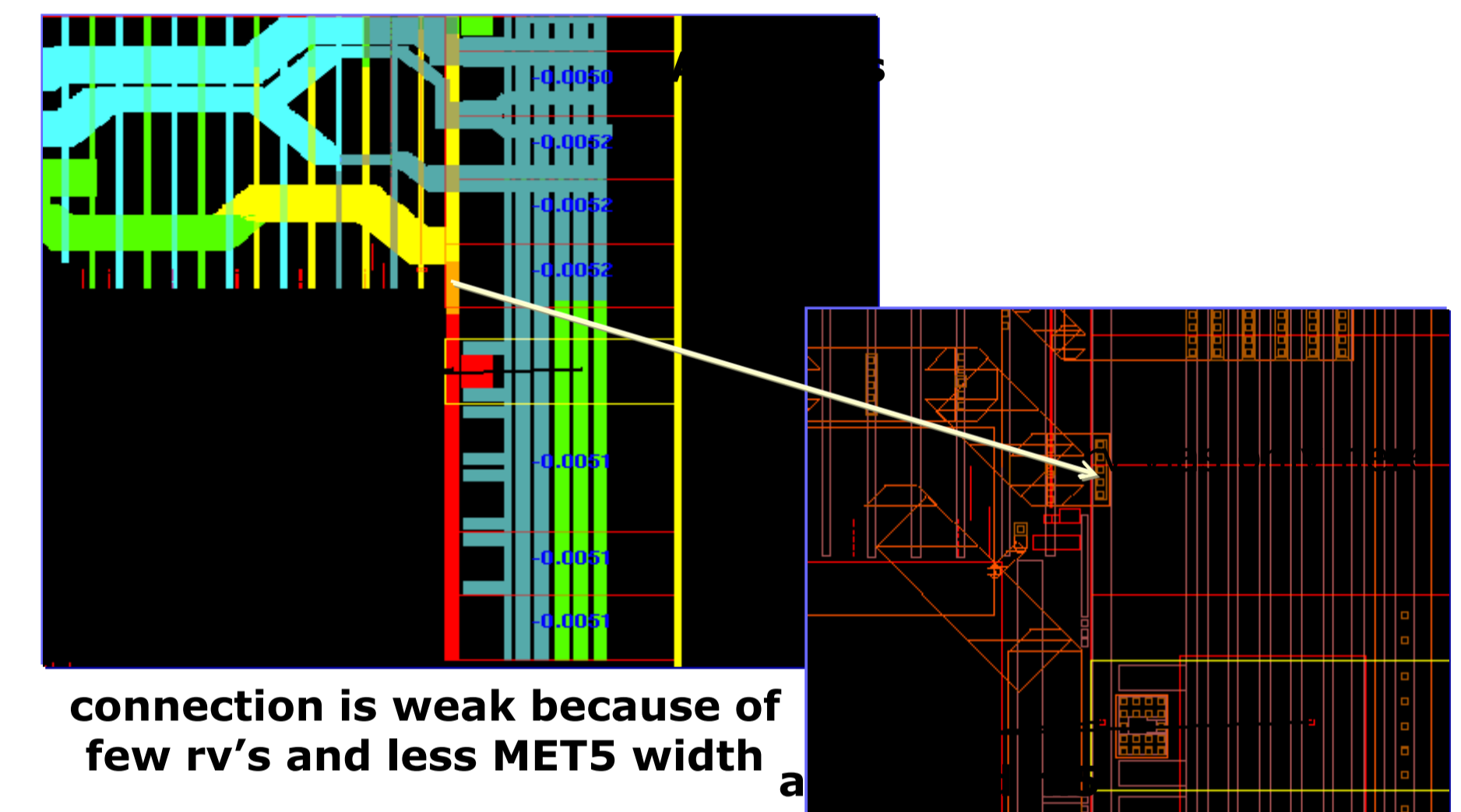
Figure 5 – Input Requirements

CDM Static ESD Verifier

- Clamp and ESD analysis thresholds information is provided through clamp and rule file (example shown below)
- Based on identified clamps and associated domains, all clamps connected to logic instance/macro are considered and electrically shorted clamp is reported
- Both ARC (either VDD or VSS paths from logic instance to clamp) as well as LOOP (VDD + VSS path resistance) are compared and reported.
- Multiple IP's are verified during C2I verification:
 - Standard cells, Memories, Pad IO's, Analog blocks,
 - Cells inside the Analog blocks protected by top level clamps



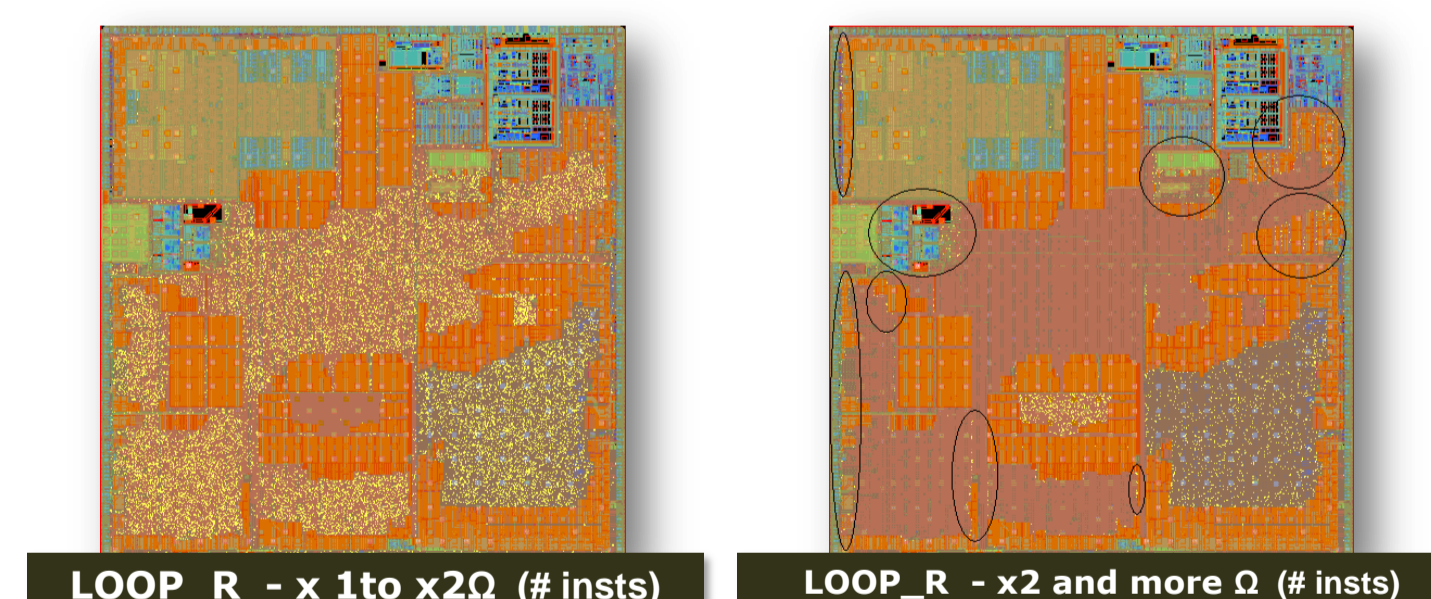
Debug ESD Failures: Resistance Debug



connection is weak because of few rv's and less MET5 width

Standard Cell ESD Checks Results

Loop R Distribution



B2B ESD Results



CDM ESD VERIFICATION

Design Info: (Flip chip 65 nm Design)	
Size	3.9m x 4.2m (540K instances)
Power Pads	40+
Power Domain	7 (4 Power and 3 Ground)

CDM ESD Results: (64GB machine, 4 threads)

Memory	1170MB
Runtime	2 mins 5 secs
Total # loops checked	153
Loop Summary	Pass: 152 Fail: 1
ARC Summary	Pass: 152 Fail: 0

