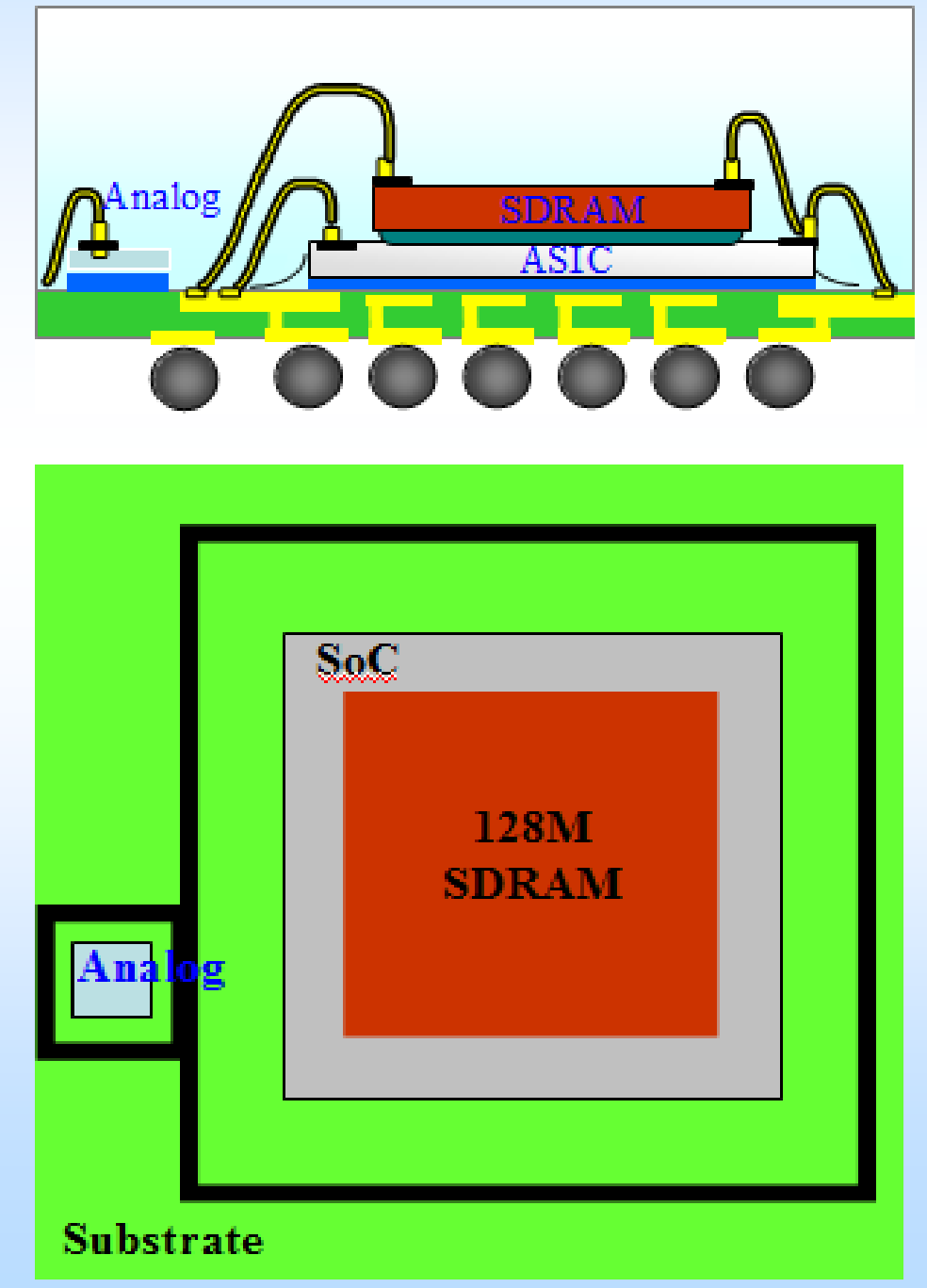
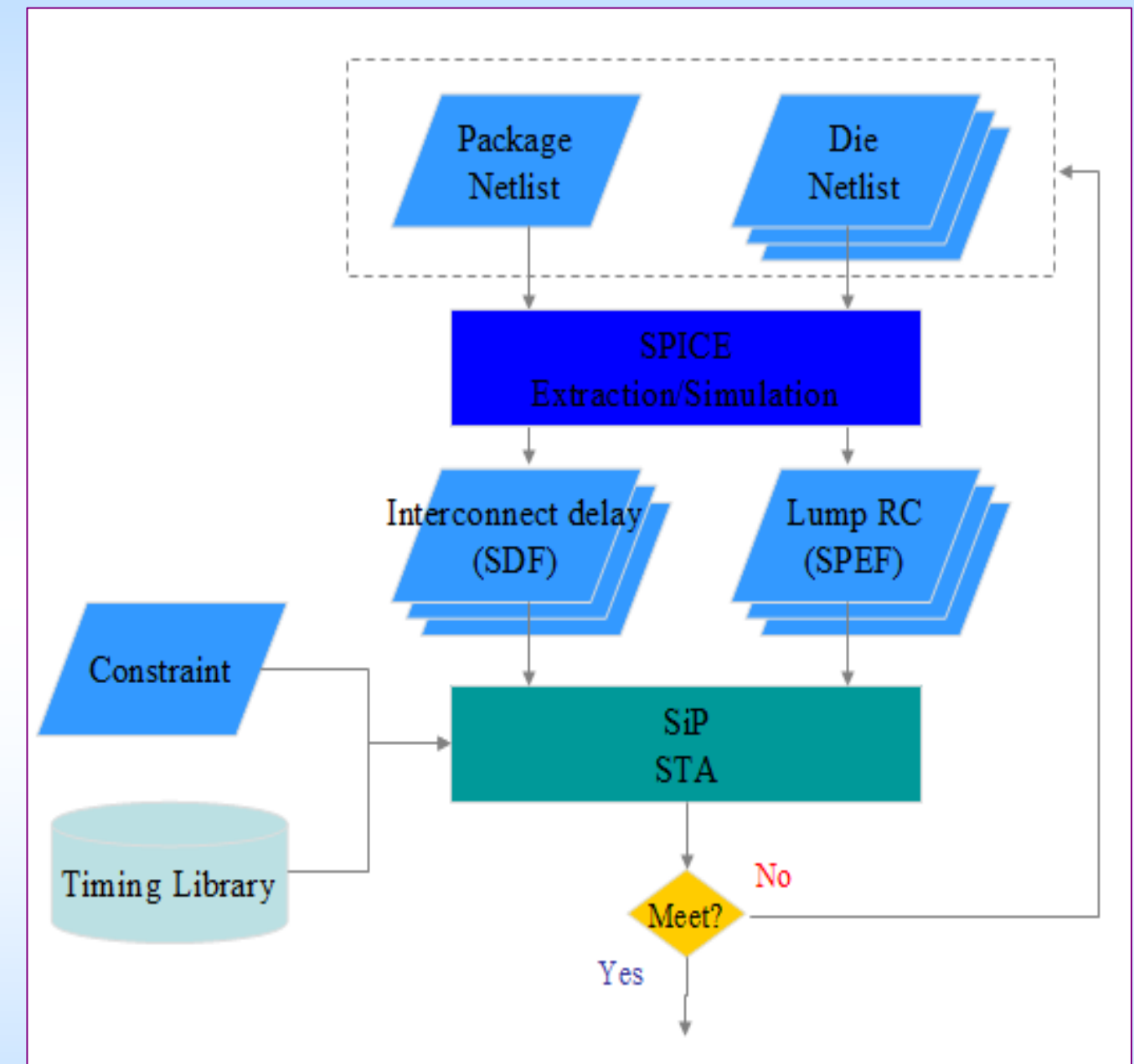


Background

Heterogeneous integration for analog and RF
Analog/RF may not be ported to advanced technologies from cost/ performance consideration.



Traditional SiP Timing Flow
Lack of accurate cross-die timing in chip implementation



SiP-level STA is applied late in design stage
Ability and capacity to handle SiP level STA is critical. Timing cannot correlate to spice simulation with lump RC (SPEF). It almost have no chance to fix timing issues after STA.

Experiment & Observation

Timing library characterization
In real case, the capacitance of package could be out of table index.
Abstraction model for package interconnect
SPEF cannot represent package behavior.

	Spice Value		Look-up value with lump RC	
	Input trans. = 1ns	Input trans. = 0.1ns	Input trans. = 1ns	Input trans. = 0.1ns
Case 1				
Cell Rise delay	4.199E-09	4.127E-09	4.60E-09	4.53E-09
Cell Fall Delay	4.125E-09	4.080E-09	4.73E-09	4.68E-09
Cell Delay	4.162E-09	4.104E-09	4.66E-09	4.61E-09
Case 2				
Cell Rise delay	4.191E-09	4.119E-09	4.56E-09	4.50E-09
Cell Fall Delay	4.054E-09	4.002E-09	4.68E-09	4.64E-09
Cell Delay	4.123E-09	4.060E-09	4.62E-09	4.57E-09

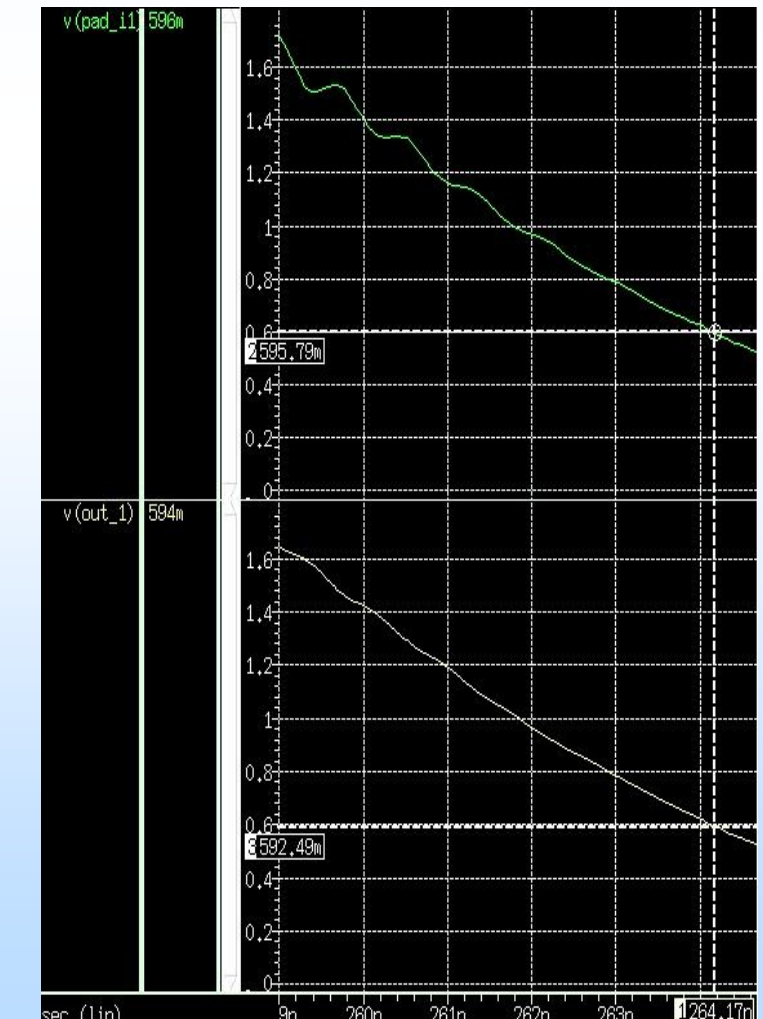
Independence of output transition
The output transition is almost the same whether the input transition is good or not.

	Input transition = 1ns (.sec)	Input transition = 0.1ns (.sec)
Case 1	1.9692E-09	1.9605E-09
Case 2	2.0147E-09	2.0196E-09
Case 3	2.0200E-09	2.0282E-09

Lump RC
Inductor contribute significantly to package timing. SPEF can only evaluate the timing caused by R and C.

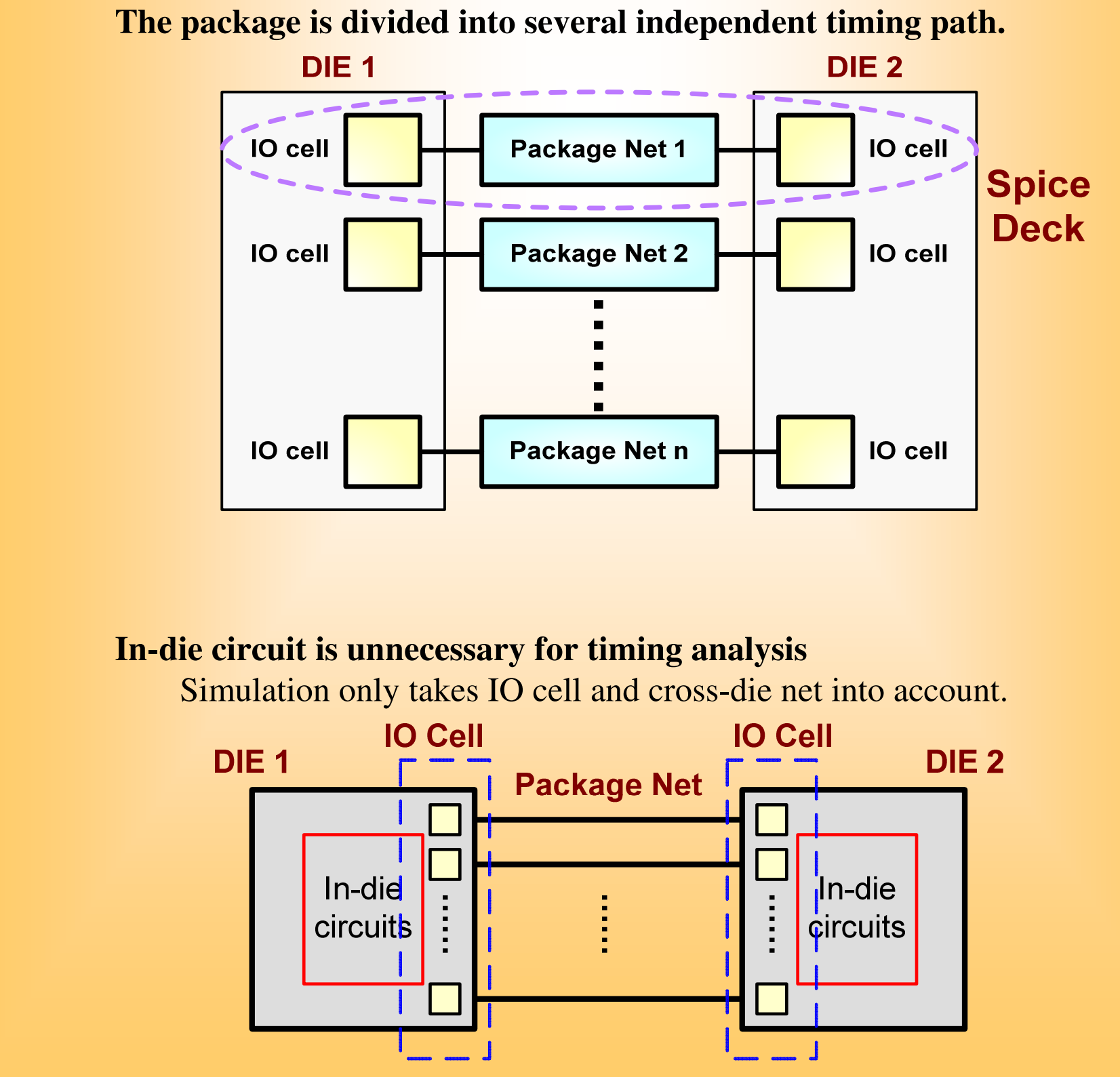
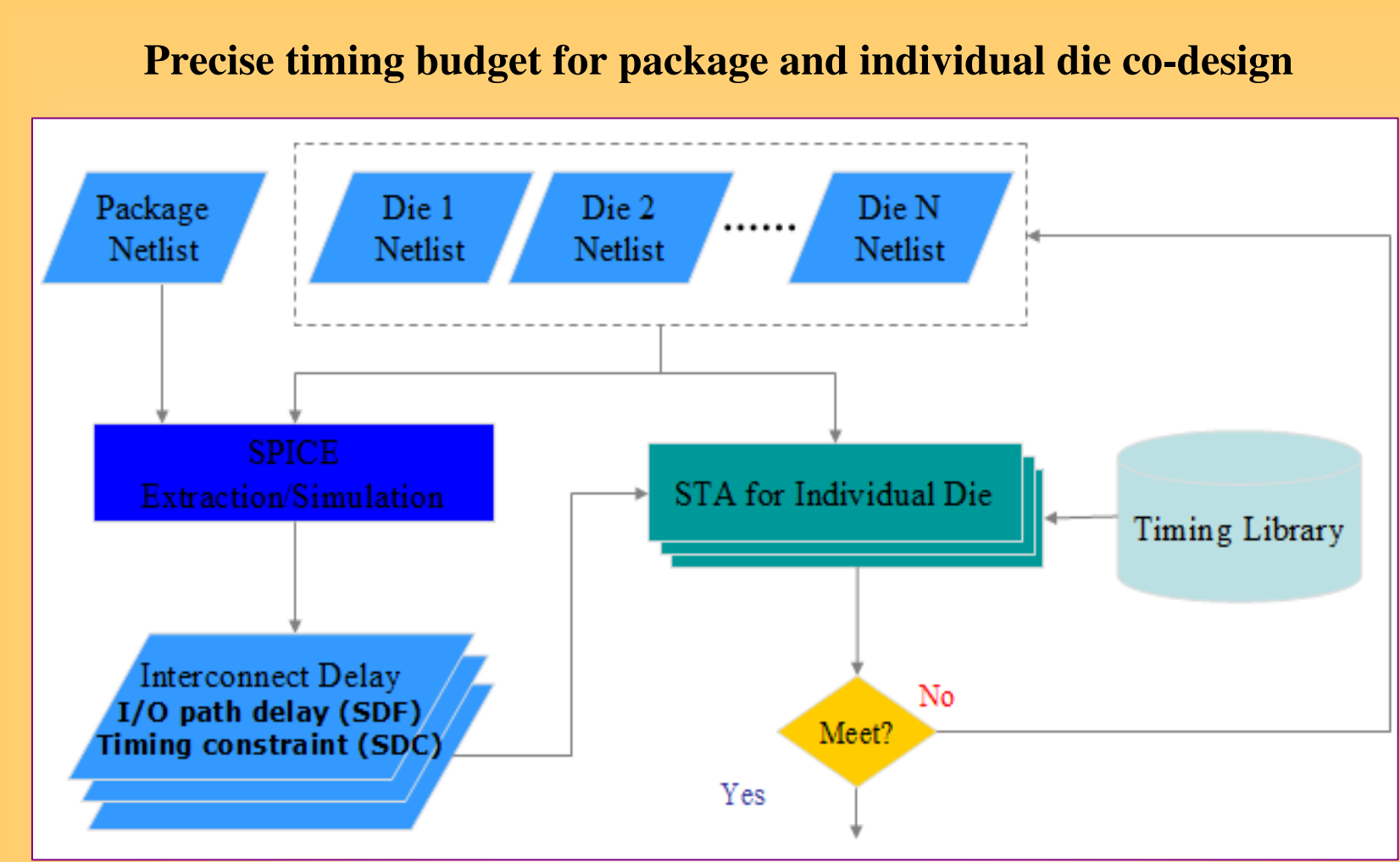
	Package delay with L	Package delay without L
Case 1	3.715E-11	1.123E-12
Case 2	3.810E-11	1.122E-12
Case 3	3.761E-11	1.187E-12
Case 4	3.847E-11	1.186E-12

This signal acceleration is caused by inductors.

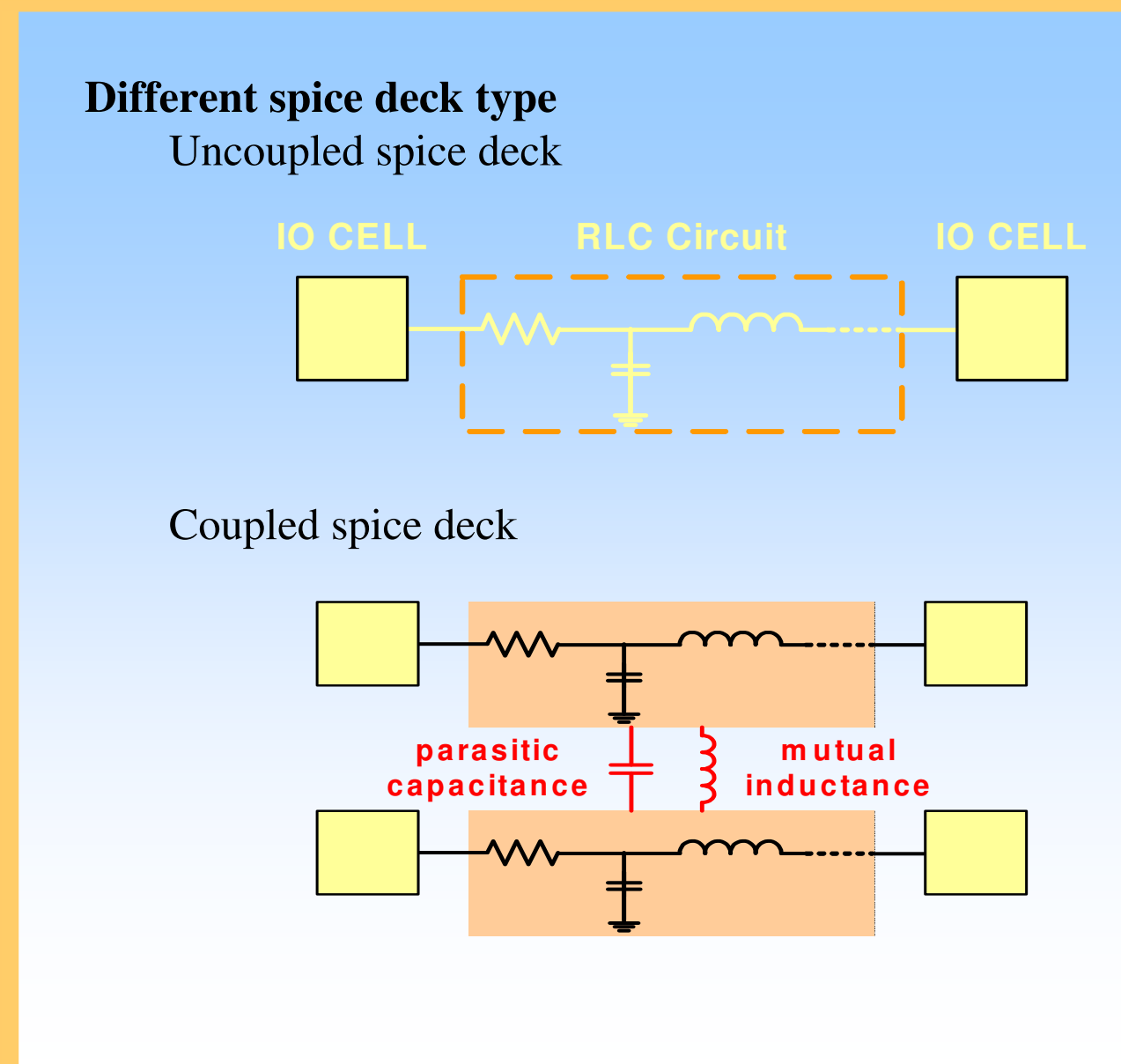


	Package delay
case_1	-1.548E-11
case_2	-1.771E-11
case_3	-1.451E-11
case_4	-1.494E-11

Timing Budgeting Flow



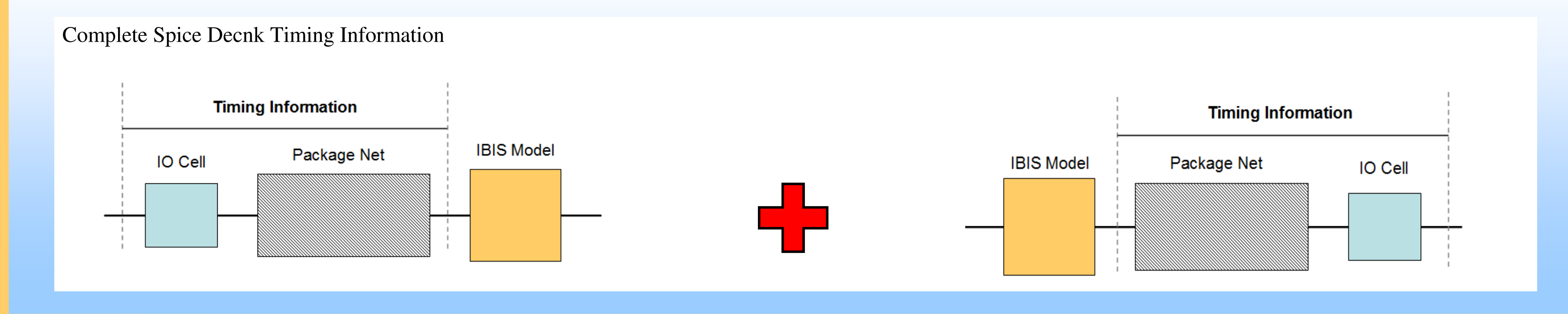
Result & Conclusion



Replace receiver IO cell with IBIS model
IBIS model seems to be more precise than equivalent model.

Delay Time of Driver's IO Cell			
	With IO cell	With equivalent model	With IBIS model
Case 1	4.162E-09	4.079E-09	4.082E-09
Case 2	4.123E-09	4.071E-09	4.070E-09
Case 3	4.111E-09	4.087E-09	4.111E-09
Case 4	4.165E-09	4.085E-09	4.165E-09

Lack of timing information
IBIS only contains IV information, but no timing information. Two stage simulation is necessary in heterogeneous simulation.



A precise timing budgeting flow is proposed for heterogeneous multi-die system co-design.
No guess, no package type restriction
The cross-die timing (delay and constraint) can be derived automatically with the ability to partition package netlist into individual spice deck.