

SCV Transaction Recording and Its Application to TLM-2.0 AT Style Performance Modeling

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Outline

- Background
- SystemC Verification (SCV) Standard
- Example – AXI
- Experiment – PCI Express Switch
- Potential SCV Transaction Recording Use Models
- Summary

Background

- Performance Modeling is widely used for system architecture/micro-architecture exploration
- SystemC and TLM-2.0 are displacing proprietary frameworks in the interest of interoperability and reuse
- Accurate project of system throughput/latency is a necessity
 - Approximately-timed coding style used
 - Payload and phase extension mechanism used
- Challenges
 - Debug correctness of arbitration algorithm, ordering, pipelining
 - Correlate TLM models with hand-coded RTL implementations

SystemC Verification Standard (SCV)

- Enables transaction-based verification using SystemC in a top-down design flow
- SCV includes
 - Data introspection
 - Constrained and weighted randomization
 - Transaction recording
- Transaction recording/visualization is essential to TLM-2.0 AT model debugging
 - Various proprietary frameworks (APIs, viewers, etc.) exist

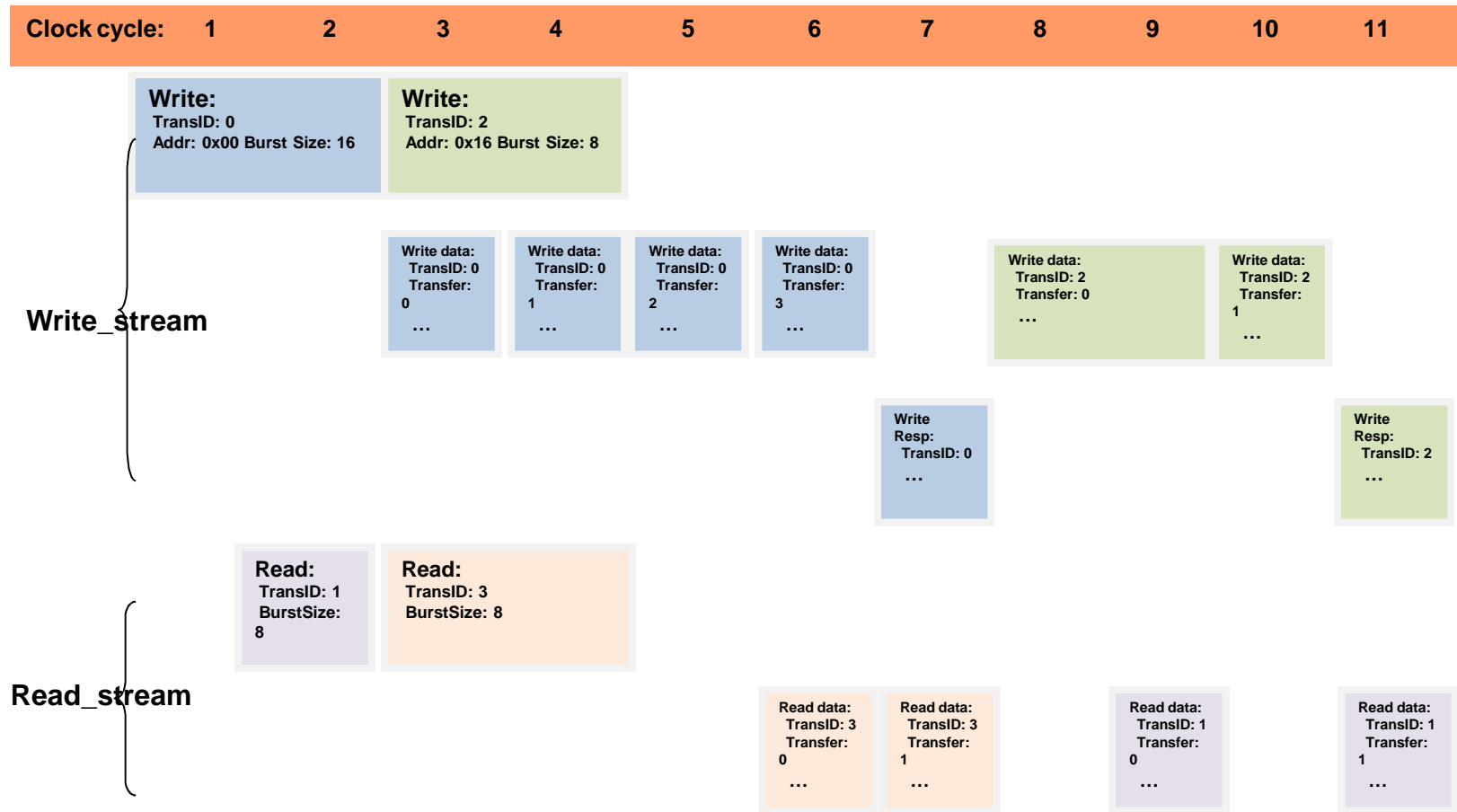
SCV Transaction Recording

- Standard transaction recording APIs
 - Ensure instrumentation code portability
- Layered structure powerful and flexible
 - Transaction has a begin time, end time, and any number of data attributes (e.g. int address, int data)
 - Generator (`scv_tr_generator<>`) creates instances of transactions of a specific type (e.g. read request, completion data, etc.)
 - Stream (`scv_tr_stream`) groups related and potentially overlapping transactions together
 - Database (`scv_tr_db`) contains a set of transaction streams
 - An ASCII database provided by SCV, vendors can provide optimal underneath implementations

AXI TLM-2.0 AT Model – Phase Extension

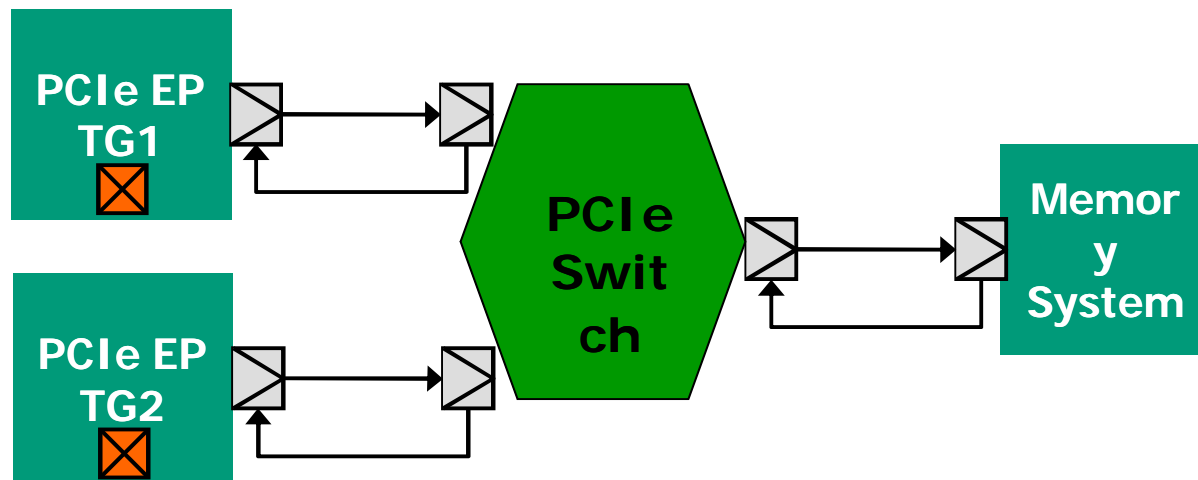
TLM-2.0 Extended Phases	AMBA AXI Representation	Called by	Comments
READ_REQ	Read address/control	Initiator	
END_READ_REQ		target	
READ_DATA	Read data	target	Can be called several times to model separate data transfers within a burst
END_READ_DATA		Initiator	
WRITE_REQ	Write address/control	Initiator	
END_WRITE_REQ		target	
WRITE_DATA	Write data	Initiator	Can be called several times to model separate data transfers within a burst
END_WRITE_DATA		target	
WRITE_RESP	Write response	target	
END_WRITE_RESP		Initiator	

AXI TLM-2.0 AT Model - SCV Instrumentation



Out of order data return

Experiment - PCI Express Switch Model



Switch TLM model:

- QoS support through Traffic Class (TC) and Virtual Channel (VC)
- Two level arbitration
 - Port arbiter
 - Virtual channel arbiter
- Peer to peer
- PCI Express ordering

PCI Express TLM model:

- Credit initialize/update
- Ack/Nck protocol
- Transaction layer buffering
- PCI Express ordering
- Blocking transport call transaction delay

Results

- The ability to visualize transaction flow at the communication interface and internal pipeline dramatically improves the efficiency of debugging/validating TLM-2.0 AT performance models
- Critical micro-architectural design bugs were identified and possible solutions recommended at early stage
 - E.g. arbitration algorithm causing starvation of certain Virtual Channel (VC) traffic

Multiple Uses of Recorded Transaction Data

- Performance Analysis
 - Derive system or local communication protocol performance (throughput, utilization, min/max/average transaction latency, etc.) by post-processing the database
 - ASCII database can be parsed by script (e.g. Perl)
- Coverage Analysis
 - Similar to RTL verification practice, information from transaction recording can be used to dynamically adapt tests to exercise the DUT TLM model

Potential Improvements on SCV Transaction Recording

- Assisted Transaction Recording
 - Automate the transaction monitoring of TLM-2.0 based interconnect protocol
 - Switch on/off all recording or portion of platform to balance the simulation speed and debugging requirement
- Correlate TLM and RTL
 - Debugging the performance discrepancy between TLM model and RTL is not trivial
 - Abstract RTL signal waveform to transaction level view
 - Run TLM and RTL in parallel and display transaction view to cross-check performance model and RTL implementation

Summary

- Transaction recording/visualization essential in performance modeling using TLM-2.0 AT coding style
- The SCV standard achieves tool portability and model interoperability
- SCV transaction data can serve many useful purposes
- Potentials to improve SCV standard