CHIP ASSEMBLY FLOW : Quick and Easy Way To Reduce the Timing Analysis Cycle Time

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Traditional Hierarchical Flow

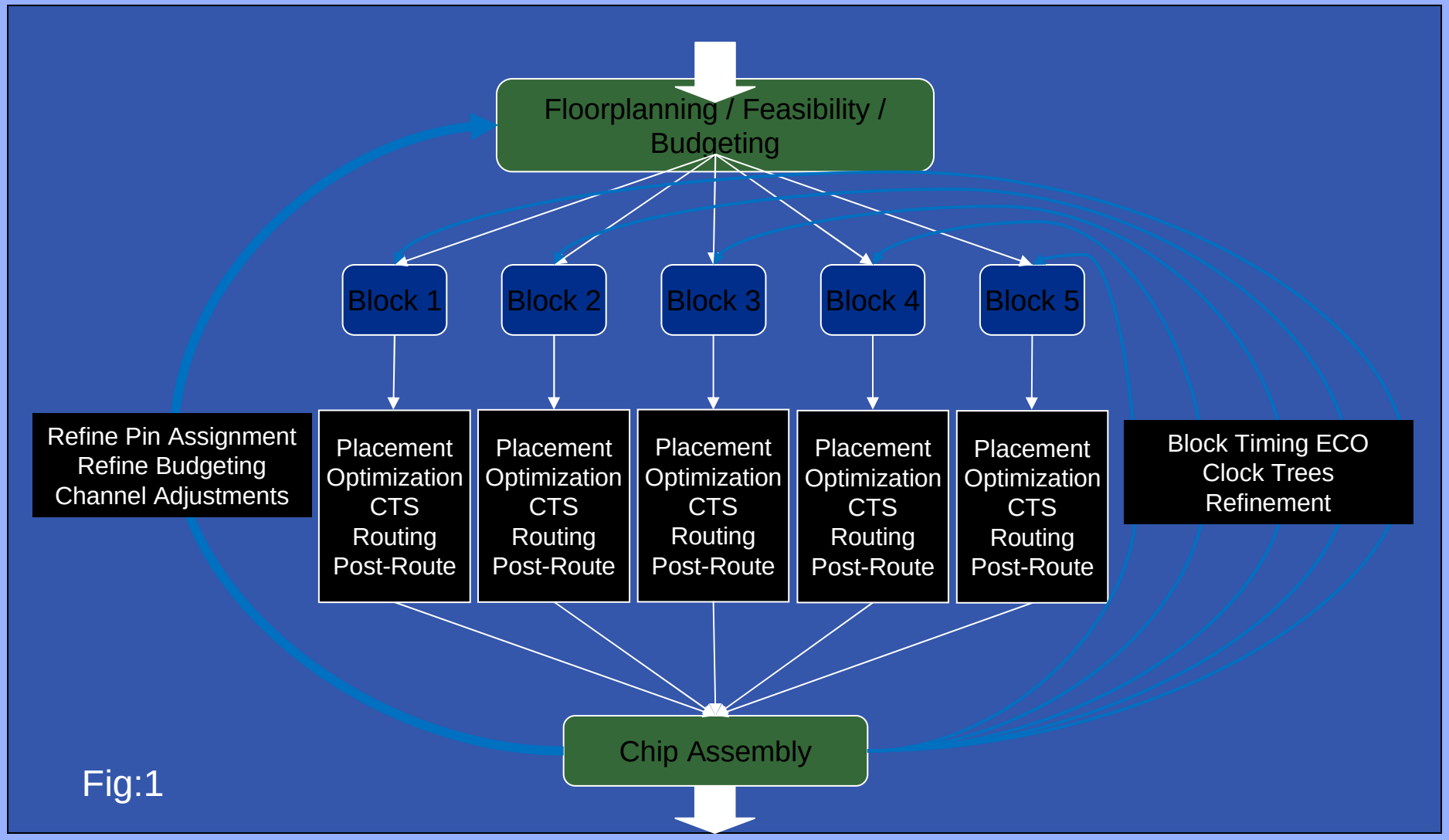


Fig:1

Issues seen during chip assembly

- Bad timing budgets allotted during chip planning caused I/O timing violations that couldn't be corrected using the abstraction models.
- Abstraction models used to overcome tool capacity limitations were not accurate enough to close chip-level timing.
- Due to abstraction model usage , top level CTS may not be able to see Skew and latency values as seen by STA tools which could affect optimization.
- Full chip static timing analysis required a separate timing run for each corner/mode scenario, and the limited tool capacity caused unreasonable runtimes.

Recommended flow

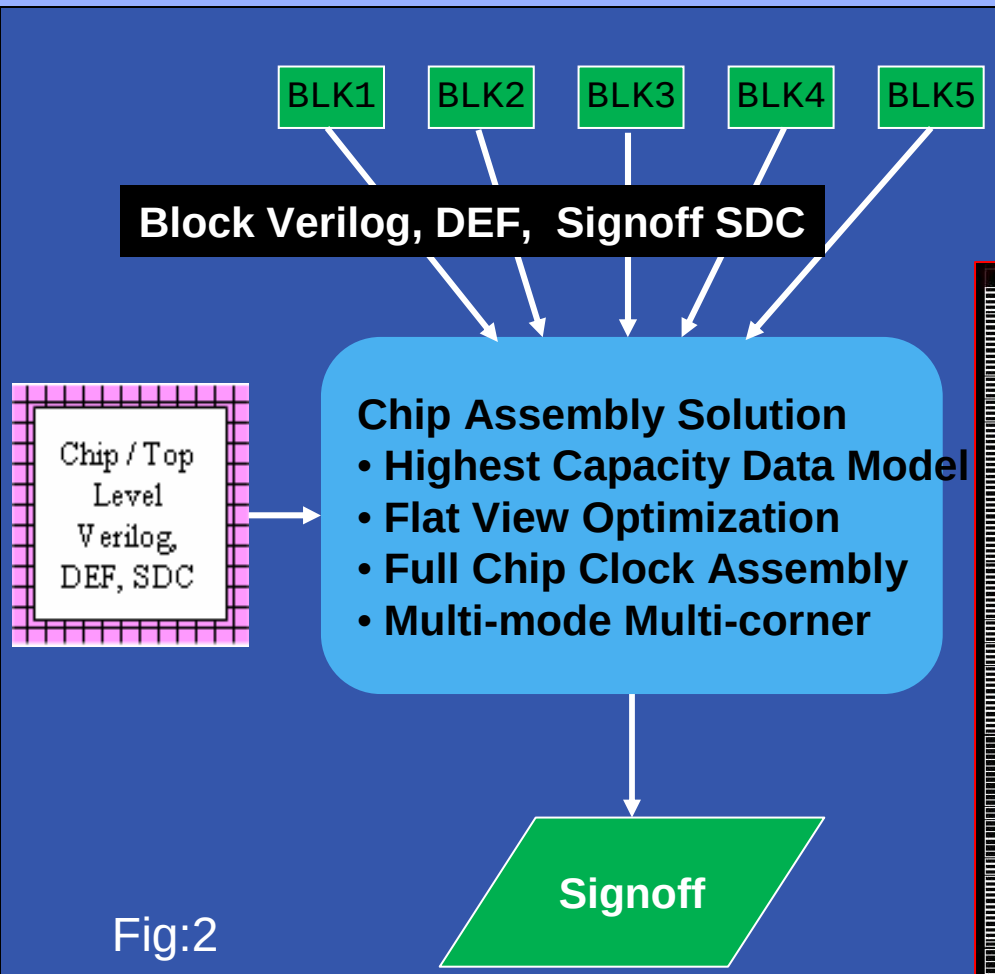
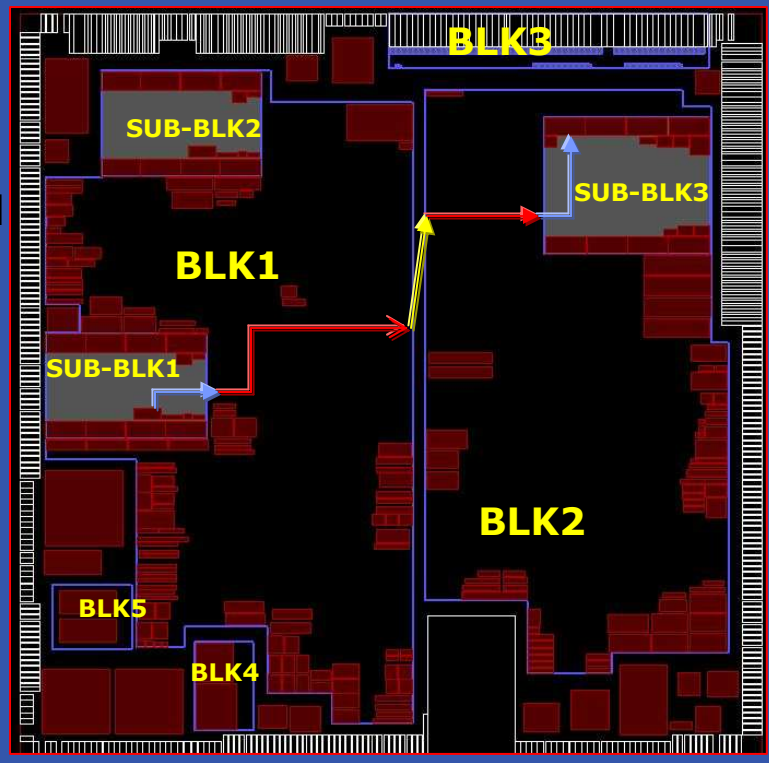


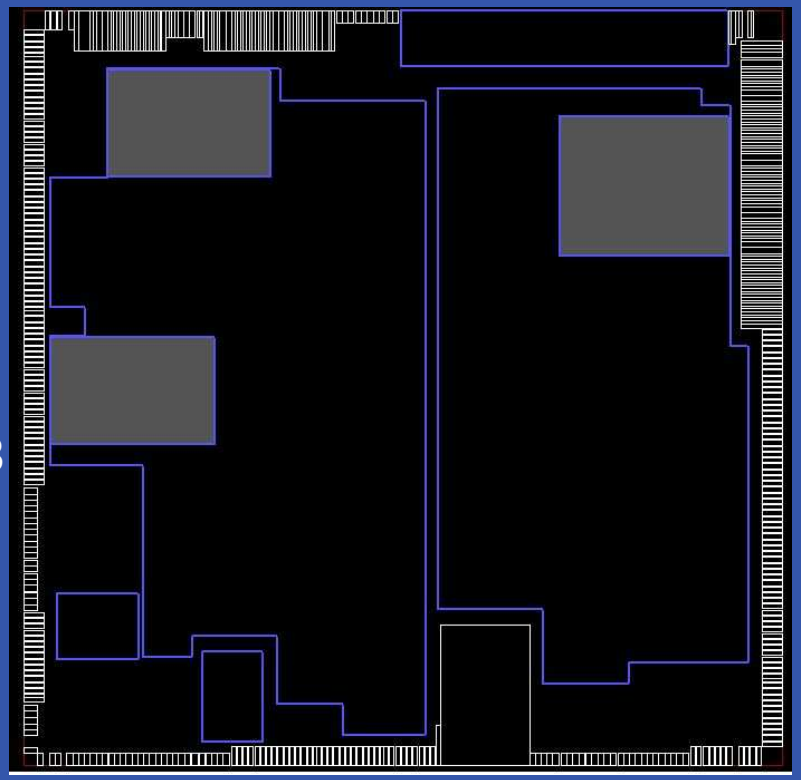
Fig:2

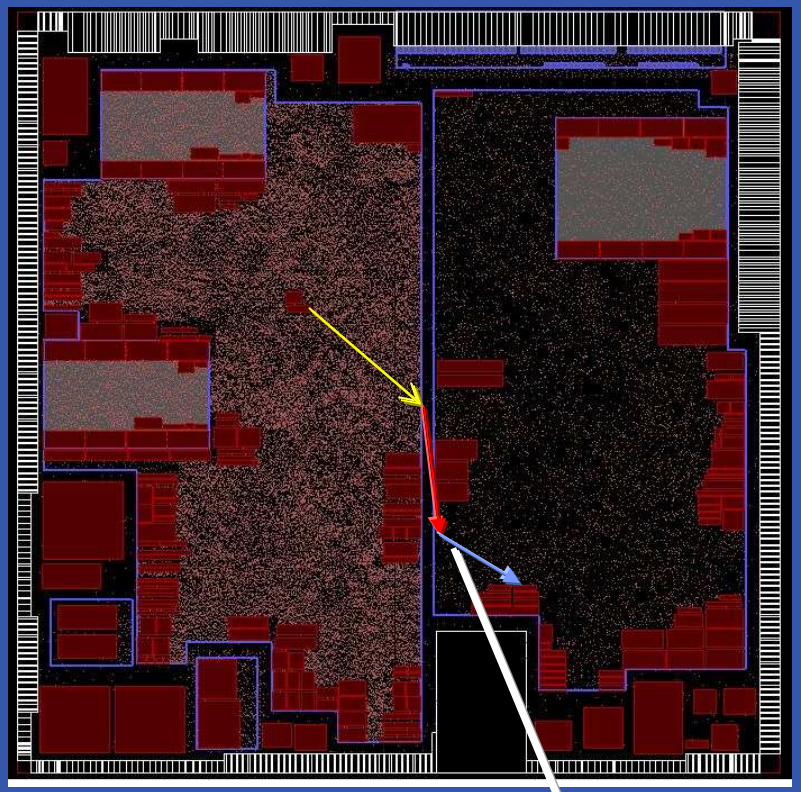
- Flexible Abstraction
- Variability aware Full Chip analysis
- Chip closure optimization



Chip Assembly – Flat View With Hierarchy

Fig:3





- **A Partition Enforces a strict boundary for tool Except Timing Analysis**

Using Real Design

- 65nm SoC.
- 34.9mm2 including padring in 55nm.
- 3.16M Instances(Olympus) , 247 Macros and 595 IO's.
- Includes ST40 and ST231 CPU hard cores.
- USB HARD PHY including DDR2 array.
- Heirarchical implementation IP in 2 partitions.
- Padring, PHYs, and small number of std cells at top level.

Olympus Chip Assembly flow

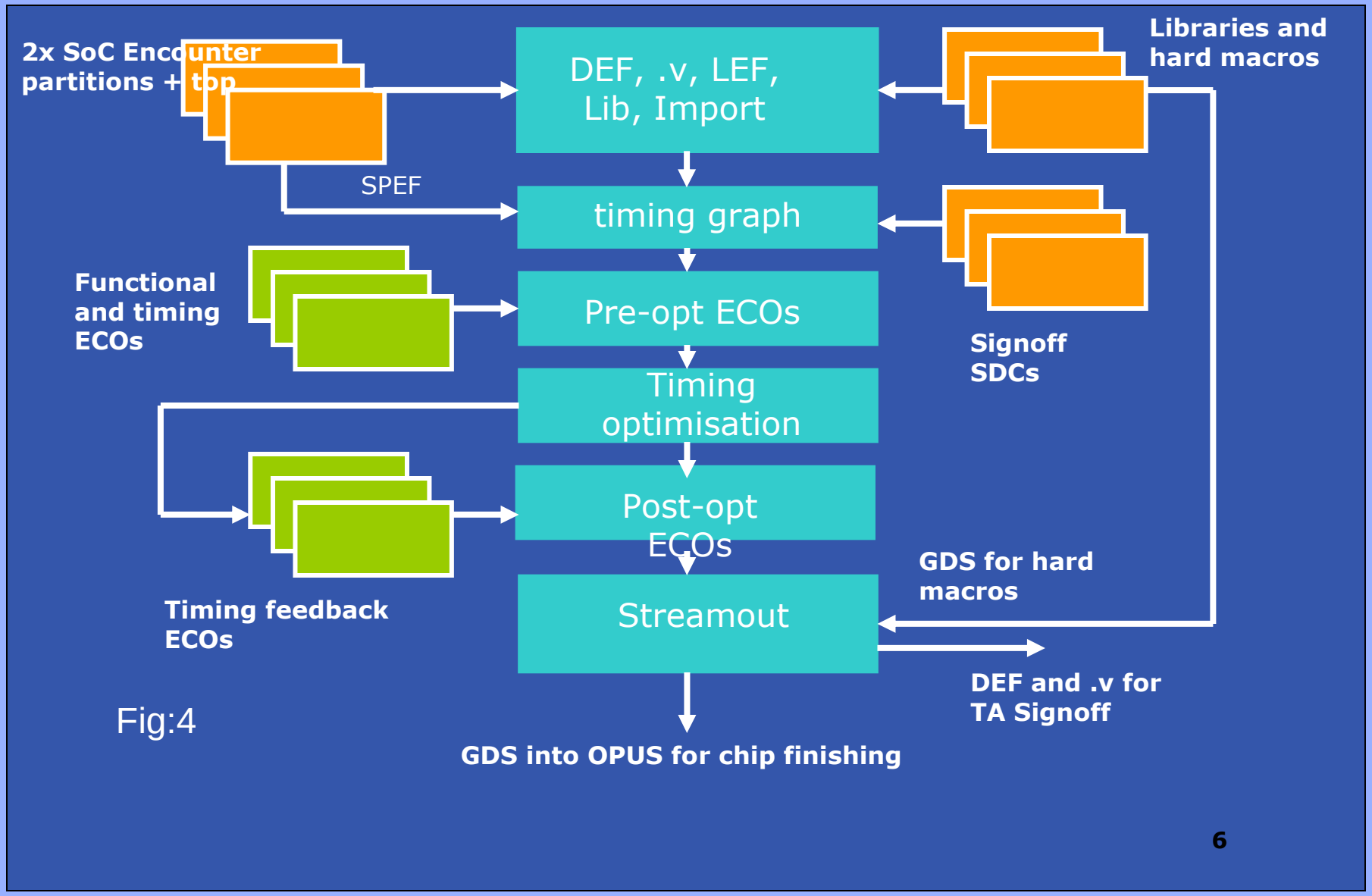
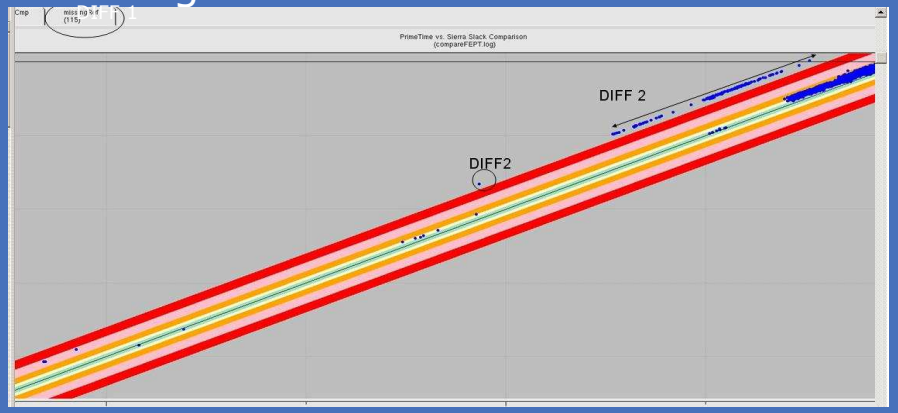


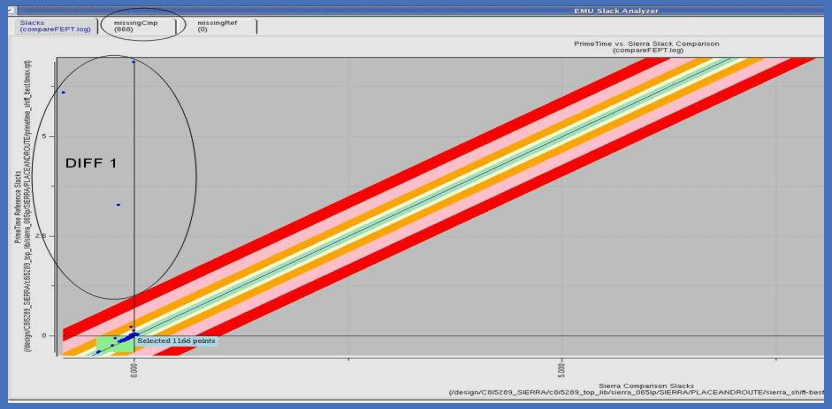
Fig:4

Timing Correlation Results

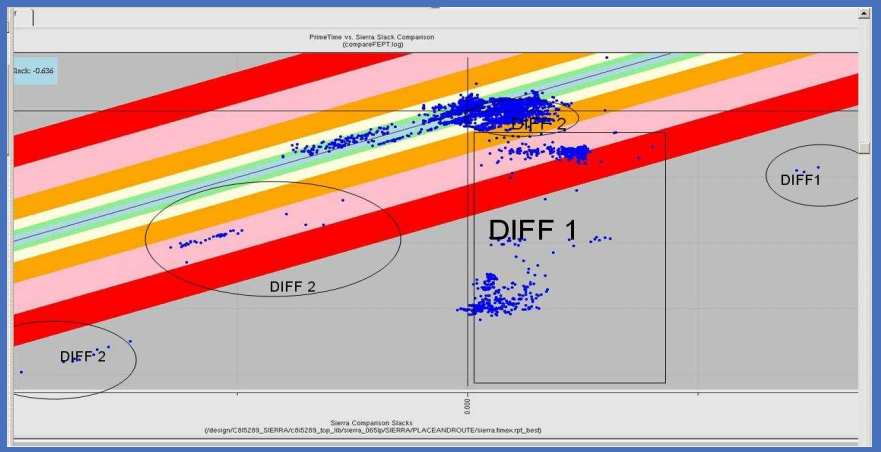
- Picture below Shows Timing Correlation Between Olympus and Signoff Tool using Cadence Time Ex.



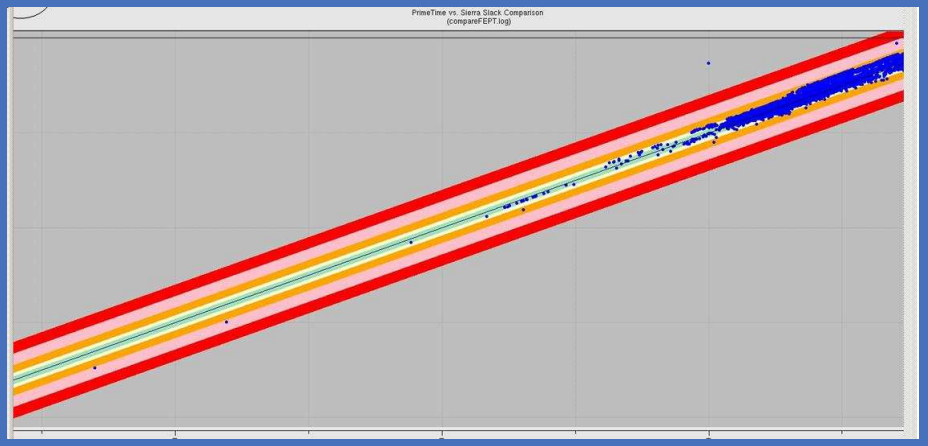
Functional Worst: Average Correlation Diff : 120ps



Scan-shift Best: Average Correlation Diff : 8ps



Functional Best: Average Correlation Diff : 79ps



Scan Capture Worst: Average Correlation Diff : 79ps

Fig:5

Understanding Correlation Differences

Apart from different timing analysis engines of two tools few reasons for correlation differences which were later worked upon classified into 3 categories were :

- Olympus Timing related Bugs/issues.
- Timing Signoff Tool Bugs.
- Understanding of the timing constraints differently by the two tools.
- Different setting of the default switches within two tools.

Optimization

- Optimization Done Across 10 MMMC Scenarios for Setup , Hold and DRVs.

FUNC-FLAT : WC-RCMAX , BC-RCMIN
WC-RCMIN , BC-RCMAX
SCAN-CAPTURE : WC-RCMAX , BC-RCMIN
WC-RCMIN , BC-RCMAX
SCAN-SHIFT : BC-RCMIN , BC-RCMAX

- Optimization Modes : White Space Driven
Normal (For Selected Clk Groups)

Optimization Results

Before optimization

After optimization

Functional Worst **Table:1**

Total no of paths	WNS	TNS	Violating paths
1572468	-11431.0	-3283809.0	13947
1572468	-4059.0	-89229.0	8046

Capture Worst **Table:2**

Total no of paths	WNS	TNS	Violating paths
254936	-3246.0	-858335.0	3101
254936	-43	-1484.0	90

Functional Best **Table:3**

Total no of paths	WNS	TNS	Violating paths
1130870	-853	-56207	2099
1130870	-530	-6023	170

Optimization Results

Capture Best **Table:4**

Total no of paths	WNS	TNS	Violating paths
688019	-498.0	-37627.0	2003.0
688019	-121.0	-4121.0	150.0

Shift Best **Table:5**

Total no of paths	WNS	TNS	Violating paths
582114	-770	-81297	4355
582114	-125	-3399	341

53% improvement across all modes and corners in worst case. Most of remaining Setup Violations were within acceptable TA Signoff range

92 % improvement across all modes and corners in best case.

Advantages of Chip Assembly Flow

- Flat Design optimized across various modes/scenarios.
- Design Accurately Analyzed in terms of clock insertions and clock skew specially for inter partition paths.
- No more Abstraction Required for the partitions which overcomes the problem of inaccurate timing budgets.
- Reduced cycle of full chip static timing analysis for across various modes and corner.

Issues Faced During the Flow

- No CRPR was calculated by the tool for Interfaces (IO Pads).
- Issues with Parasitic file dumped by the tool. Was not read by Timing signoff tool.
- Layout Editing Capabilities of the tool needs to be improved.
- Incorrect Change file dumped by EcoByverilog utility for functional ECOs.
- Initial Crashes while reading the parasitic files using multithreaded timer was not always reproducible.

Enhancements / Workarounds

- Big Functional ECO's were implemented using awk script which converted the FE ECO file to olympus compatible syntax as EcoByVerilog was not working.
- A utility was developed to incorporate the late requests in olympus database from Analog experts by reading incremental DEF as layout editing capabilities of tool were not so good.
- A tcl script was written to implement the timing ECOs from signoff tool.
- For Metal Mask ECO's Delta Routing Changes in olympus database were replicated in Final Virtuoso database using tcl and skill utility. This avoided repeating tasks to reach Final Signoff database.

Conclusion

- Timing signoff eco cycle greatly reduced across all modes and corners.
- Skew from top is completely seen and taken care leading to better and comprehensive timing optimization.
- Good Database handling capacity with flat database loaded and optimized across 10 MMMC scenarios.
- Very good correlation with the Signoff tool with first time silicon success.
- The timing violations were fixed across all MMMC scenarios (Modes/Corners) in one session.