

A Novel Frequency Domain Noise Analysis through Different Power Domains for large SoC Designs

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Motivation

Analog circuit analysis in SoC requires

- **Precise simulation**

Analog circuits are very sensitive

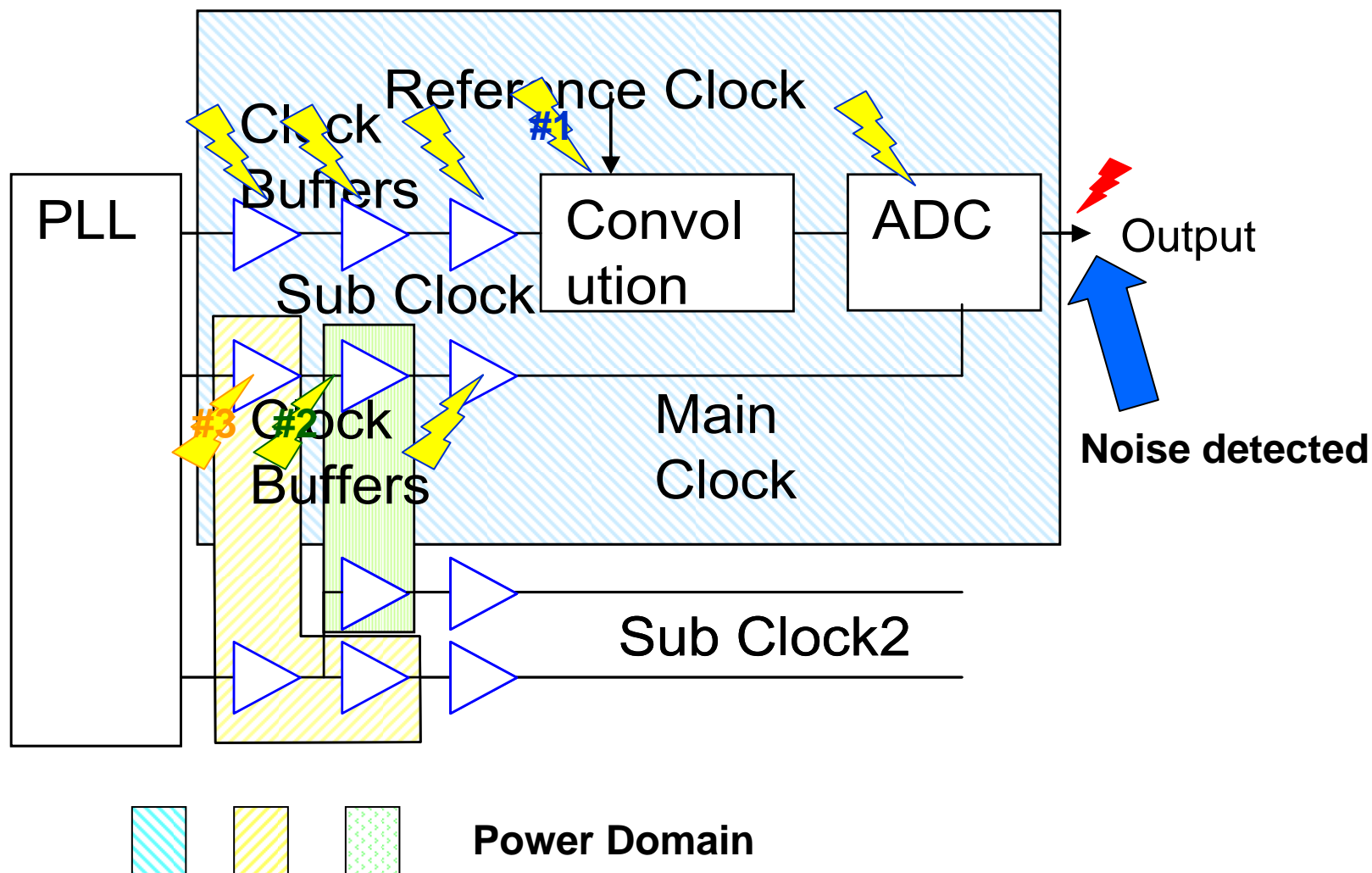
- **Large Capacity**

Varieties of noise source exist in SoC which have to be considered.

- **Automated Operation under Common Infrastructure**

Easy of use is important to apply the methodology

Background (Targeted Circuit)



Noise Source

■ Noise Resonance Frequency

	Reference Clock	Noise Source Clock
Noise #1	X1 freq.	X2 freq.
Noise #2	X2 freq.	X1 freq.
Noise #3	X3 freq.	X2 freq.

Background (Detected Noise)

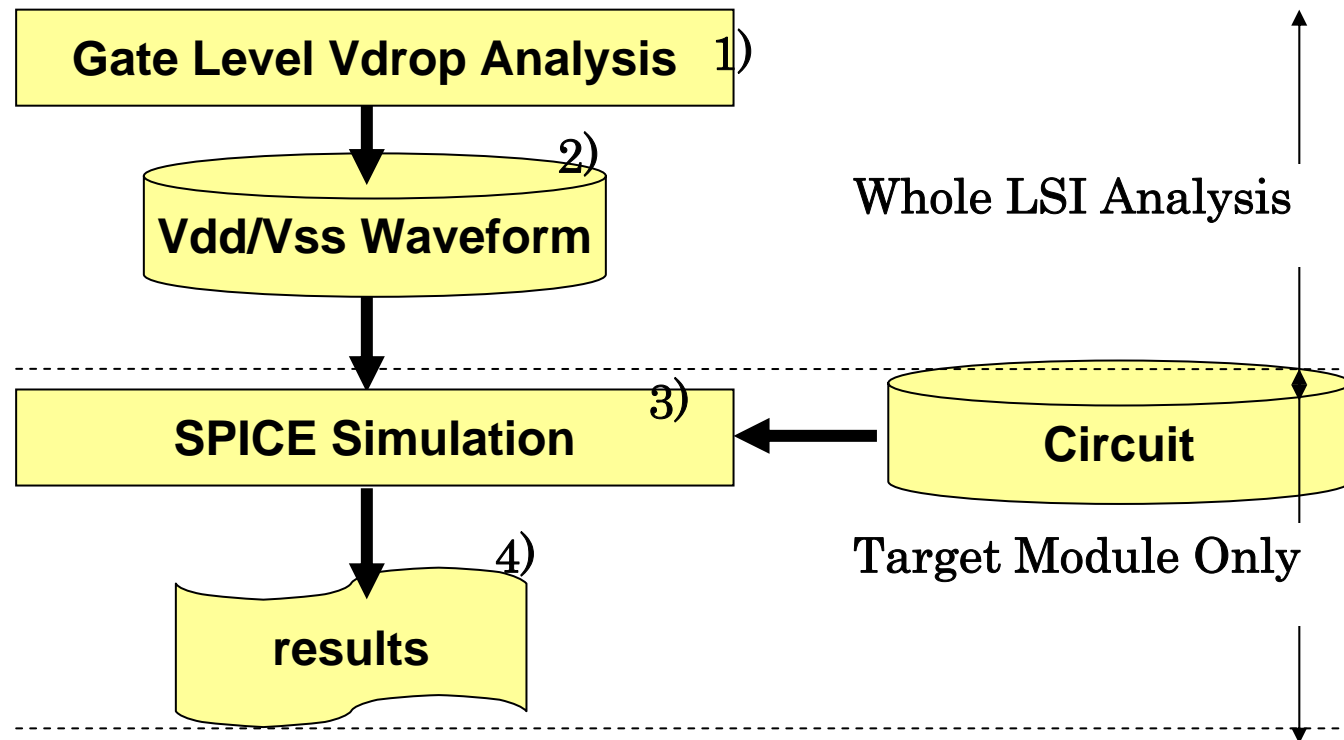
- The strongest noise frequency is captured.

However

- The 2nd strongest and 3rd strongest noise could not be detected.

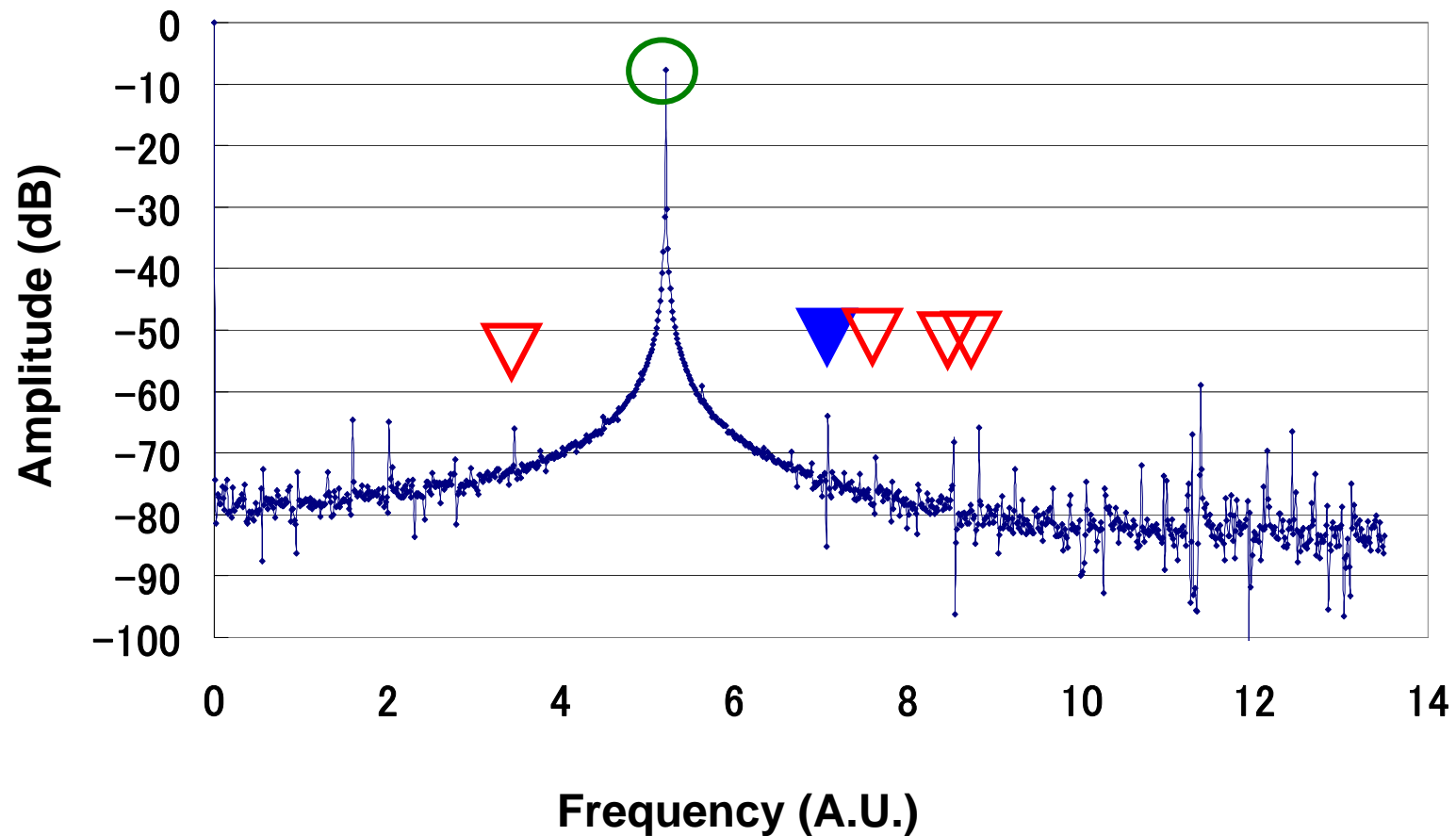
Conventional methods cannot detect noise phenomena.

Proposed Method



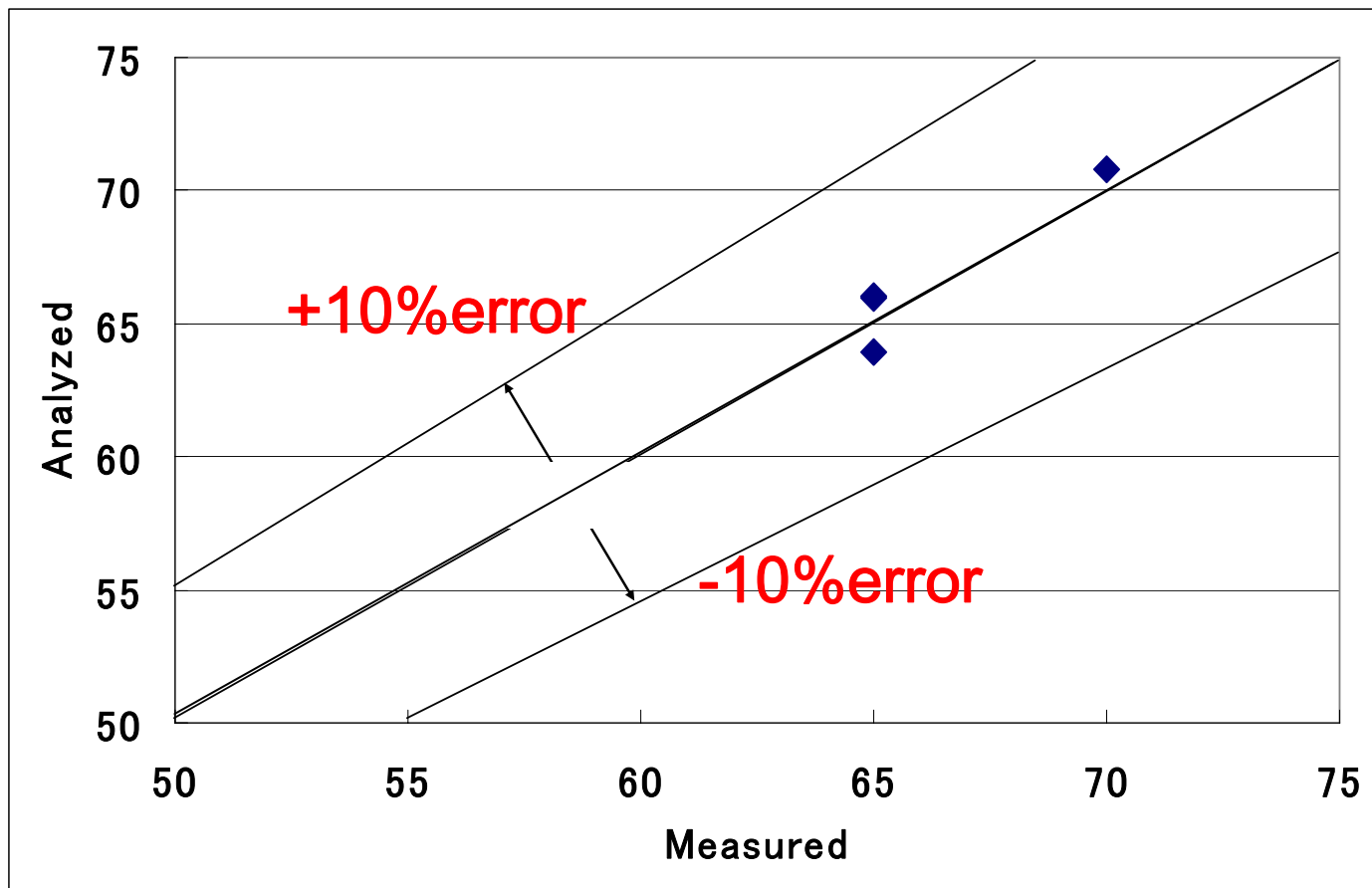
- 1) Gate Level Dynamic Voltage Drop Analysis (**Commercial**)
- 2) SPICE PWL Waveform (for targeted instances) (**Standard format**)
- 3) SPICE Simulation (target circuits only) (**Commercial**)
- 4) Result

Simulation Result



All noise frequencies found in chip are successfully detected

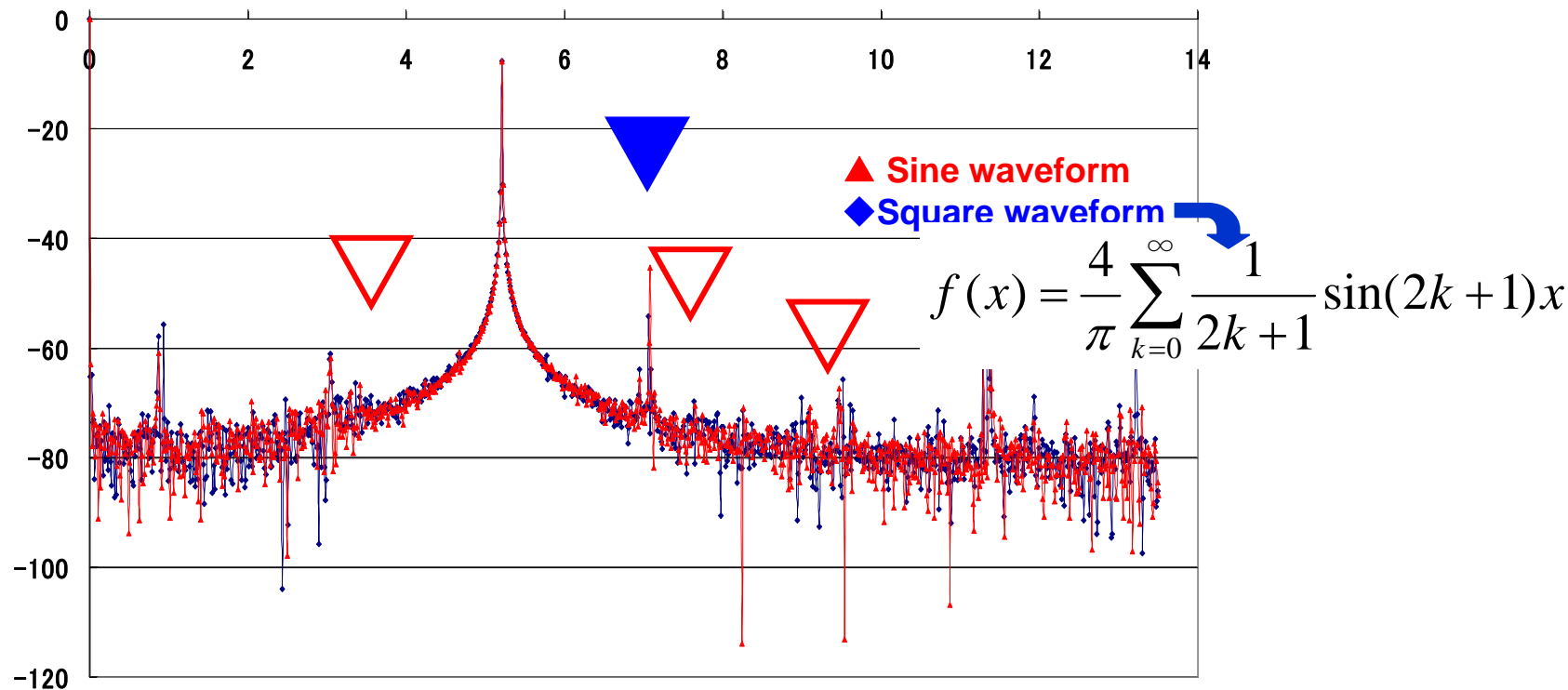
Comparison with measurement



Precise matches can be got

Simplified Approach

- Sine wave or Square wave for noise



Simplified approach (cont.)

Pros.

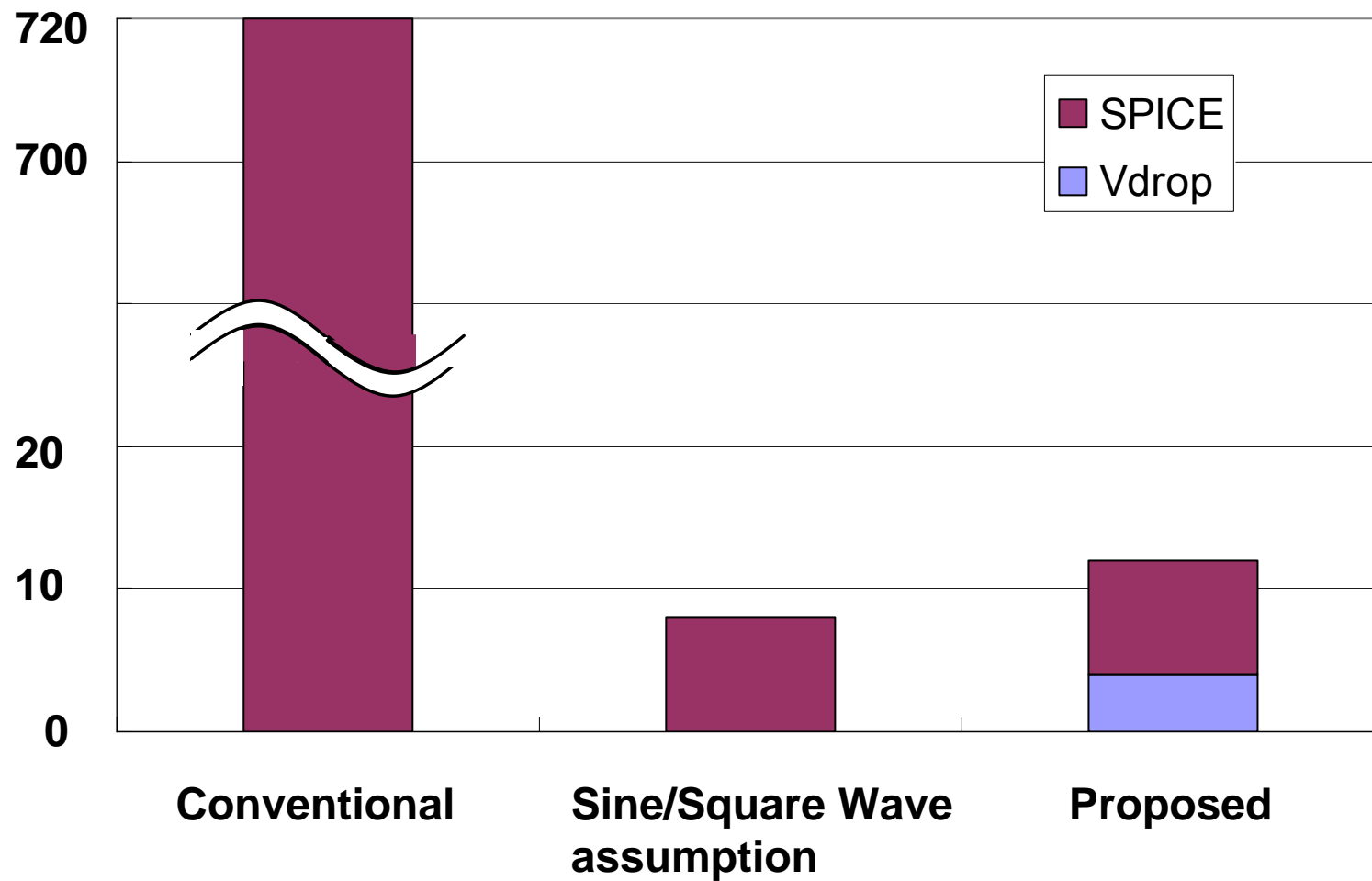
- No need voltage drop analysis
 - Faster TAT
 - No need many data preparation
 - No need special skills for gate level dynamic analysis tools

Cons.

- Limited detectable frequency
 - Sine waveform : Targeted frequency only.
 - Square waveform: Odd order frequency only.
- Amplitude depends on the waveform amplitude.

Usually disadvantage is much more serious.

Run Time



More than 50 times faster!

Summary

A practical noise analysis method is proposed.

The methods shows

- 10% accuracy against measurement can be achieved.
- Run Time is less than one day.
- It is constructed on the common infrastructure.