

Timing Margin Reduction with Statistical Characterization for SRAM Cell

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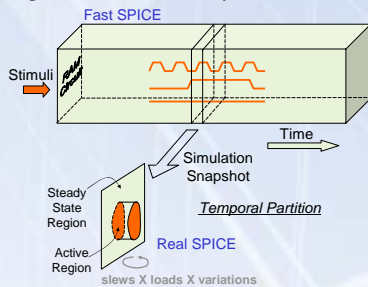
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Background

- SSTA is a powerful tool for reducing timing margin and avoiding overdesign.
- However, there are still a number of obstacles to be overcome in adopting the methodology for chip level design.
- One of them is the treatment of circuits which include SRAM cells.
- The paths which include SRAM cells are often the critical paths in a design.
- Therefore there is a strong need for an SRAM statistical characterization technology which offers short TAT yet maintains high accuracy.
- The current main difficulties for SRAM characterization are :
 - performing statistical characterization of an SRAM cell in a reasonable TAT
 - detecting and specifying the critical path in the SRAM cell
- If a statistical library for SRAM cells in the critical path is adopted, then a large timing margin reduction can be expected.

Key Technology

- Generation of highly accurate statistical SRAM library with fast TAT.
 - (1) Detect and extract the critical path in the SRAM cell which is temporal and spatial segment using fast SPICE for the whole SRAM cell automatically.
 - (2) Characterize only the extracted path by using real SPICE.
 - (3) Determine the timing sensitivity with respect to each transistor in the path automatically.
 - (4) Use parallel processing.
- These techniques are used in Altos's Variety MX for the statistical characterization of SRAM cells and the generation of SSTA library models.



Benchmark for Characterization

- Evaluation Items
 - (1) Characterization TAT Evaluation
 - (2) Accuracy of the statistical library
- SRAM Data (45nm)

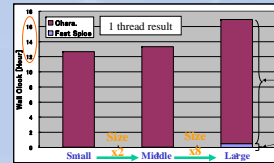
	PORT	SIZE	#WORD	#BIT	#Tr.
1	Single	Small	256	8	21k
2		Medium	256	22	51k
3		Large	2048	32	434k

Characterization Conditions

- Table Size
 - 8 x 8 : Delay, Transition, Input Capacitance, Timing Constraint (Nominal & Sensitivity)
 - 5 x 5 : Constraint (Nominal & Sensitivity)
- Variation Parameters (22 = 14 + 8)
 - Global : 14 (7/Memory + 7/Peripheral)
 - Local : 8 (4/Memory + 4/Peripheral)
- VT Condition : Vdd = 0.9V, Temperature = 125C

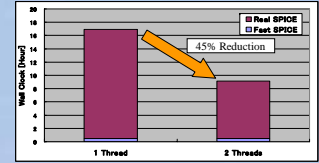
Result of Characterization TAT

Characterization TAT for SRAM cells



- The circuit size dependence is small.
- The library could be generated in 12~17 hours.
- TAT for real SPICE is dominant for the total characterization TAT.

Characterization TAT for 2 threads



The TAT is reduced by 45% compared to the 1 thread TAT.

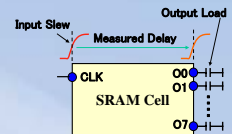
Result of Accuracy Evaluation

- Condition
 - Small Size SRAM used
 - Waveform Edge : Rise
 - Measurement : Delay from CLK to OUTPUT
- Accuracy Criteria
 - In comparison with SPICE
 - Relative Error for Delay Mean < 5%
 - Relative Error for Delay Sigma < 20%
- SSTA tool
 - ExtremeDA : GoldTime

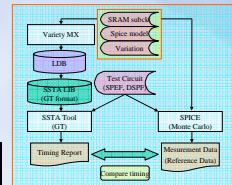
Accuracy Evaluation Result : Delay Mean and Sigma

Address : 11000001
Variation : 14Global + 8Local

Output PIN	Delay Mean		Delay Sigma	
	Rel. Error [%]	Abs. Error [ps]	Rel. Error [%]	Abs. Error [ps]
o0	0.19%	2.20	5.74%	3.96
o1	0.25%	2.86	6.47%	4.49
o2	0.19%	2.22	6.52%	4.53
o3	0.19%	2.14	6.24%	4.32
o4	0.08%	0.94	6.91%	4.82
o5	0.08%	0.95	5.37%	3.68
o6	0.11%	1.23	6.57%	4.56
o7	0.11%	1.28	6.74%	4.69



Flow of Accuracy Evaluation

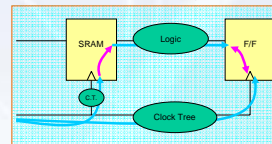


Delay accuracy criteria for both mean and sigma is satisfied easily.

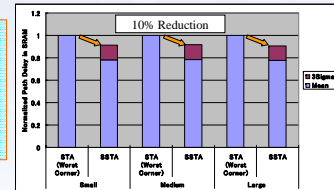
Timing Margin Reduction

- Path delay reduction by using the statistical SRAM library compared with STA worst corner library

Schematic Diagram for Circuit including SRAM



Normalized Path delay in SRAM Cell



Up to 10% delay reduction for timing margin is obtained

Conclusion

- We were able to demonstrate that Variety MX could quite easily generate a statistical SRAM library with both short TAT and high accuracy.
- The statistical treatment of SRAM cell leads to timing margin reduction.
- This timing margin reduction has an impact on the ease of timing closure in the chip level design flow.