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中国科学院计算技术研究所



A Case Study: Applying Semi-Custom Design Flow to Address Routing Challenge

Jun Xu, Ge Zhang, Jiangmei Wang, Weiwu Hu

xujun@ict.ac.cn

Institute of Computing Technology, Chinese Academy of Sciences
Loongson Technology Corporation Limited



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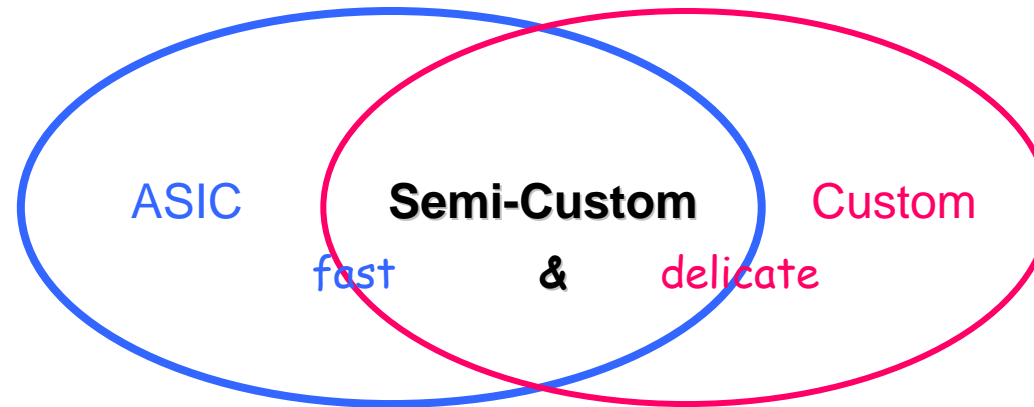
Agenda

- **Introduction**
- Problem Description
- Solutions
- Results
- Conclusion



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Semi-Custom Design Flow



- Semi-custom flow is a efficient design methodology with delicate manipulations for place & route of circuits
- Depends on the programmable interface provided by the EDA tools to accelerate the development
- Requires designers to have deep comprehensions for both designs and tools

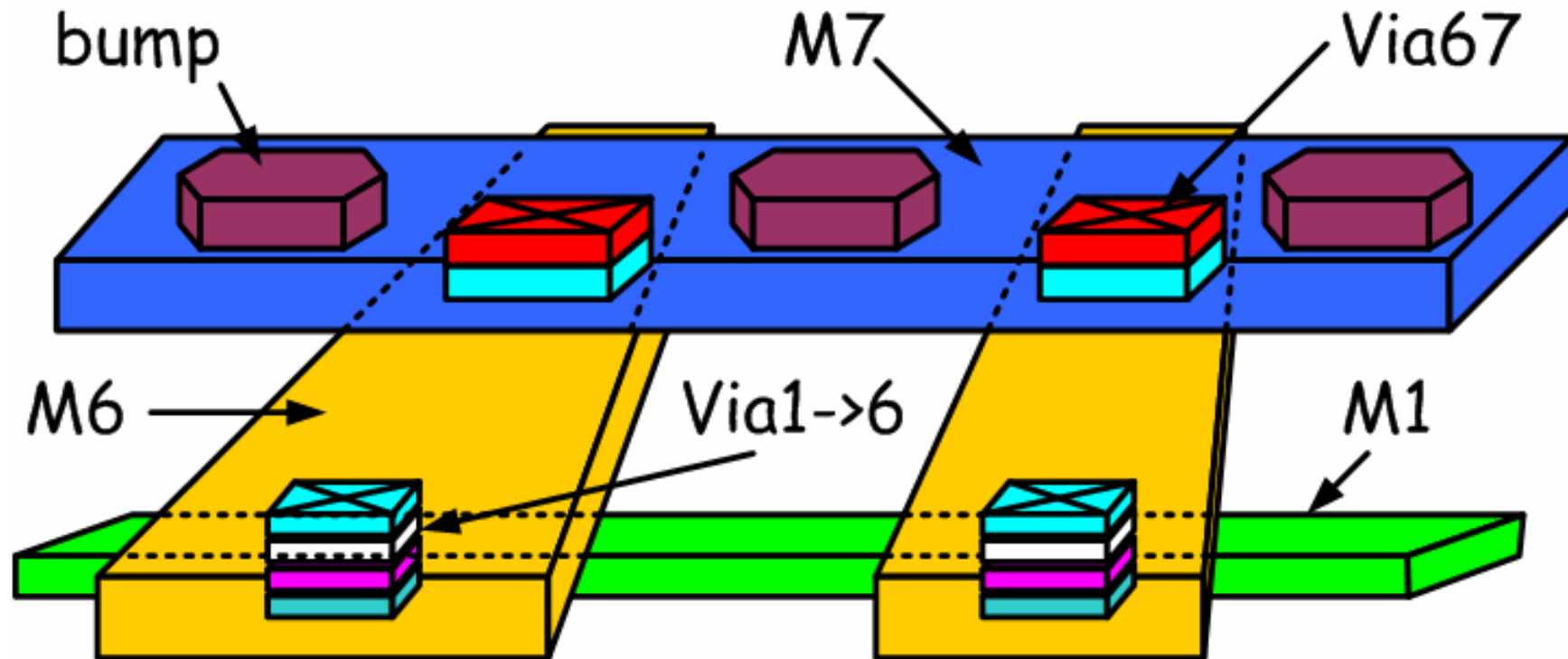


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Power Network Construction For Standard Cells

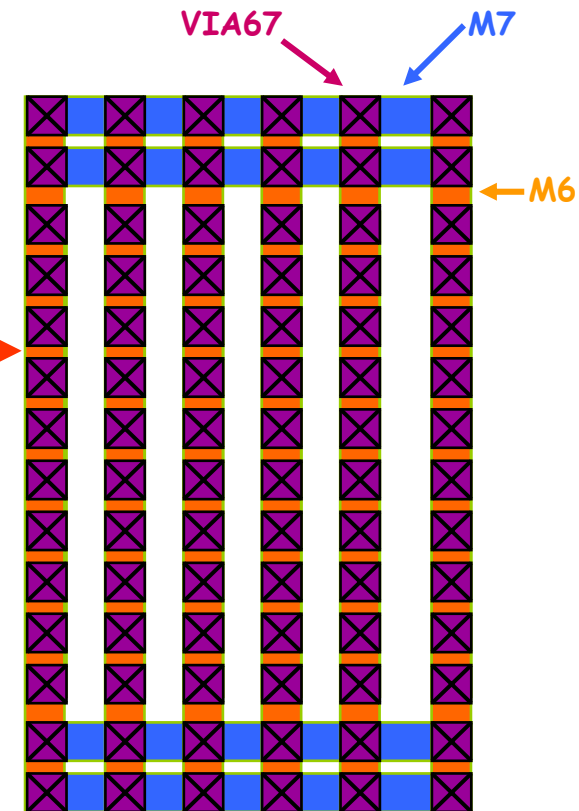
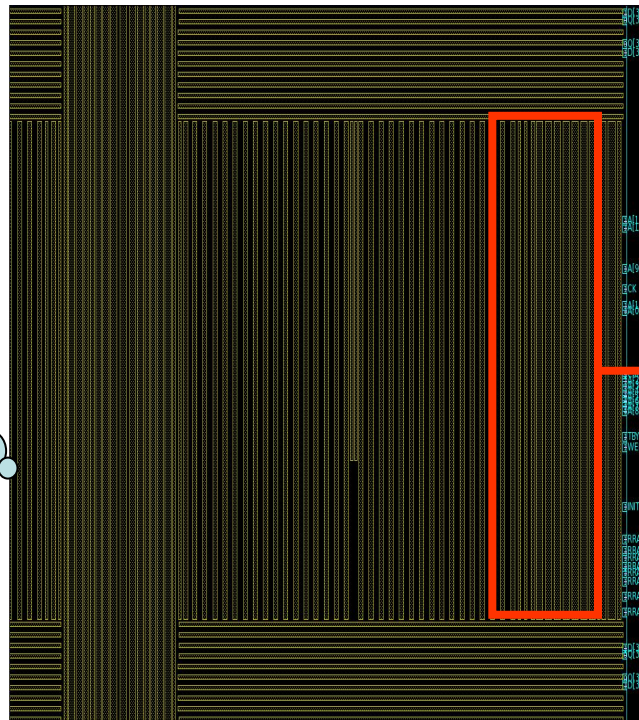
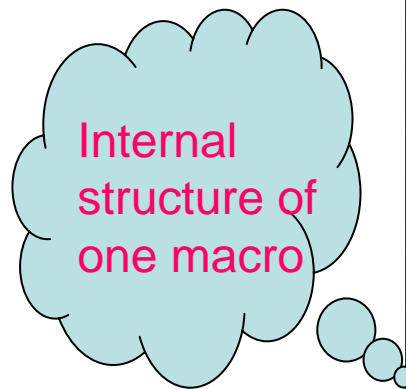


- M7 and M6 act as the power/ground network in the Godson-3 project.
- M1 serves as the follow pins of the standard cells.
- But hard macros employ different measures.....



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Power Network Construction For Macros

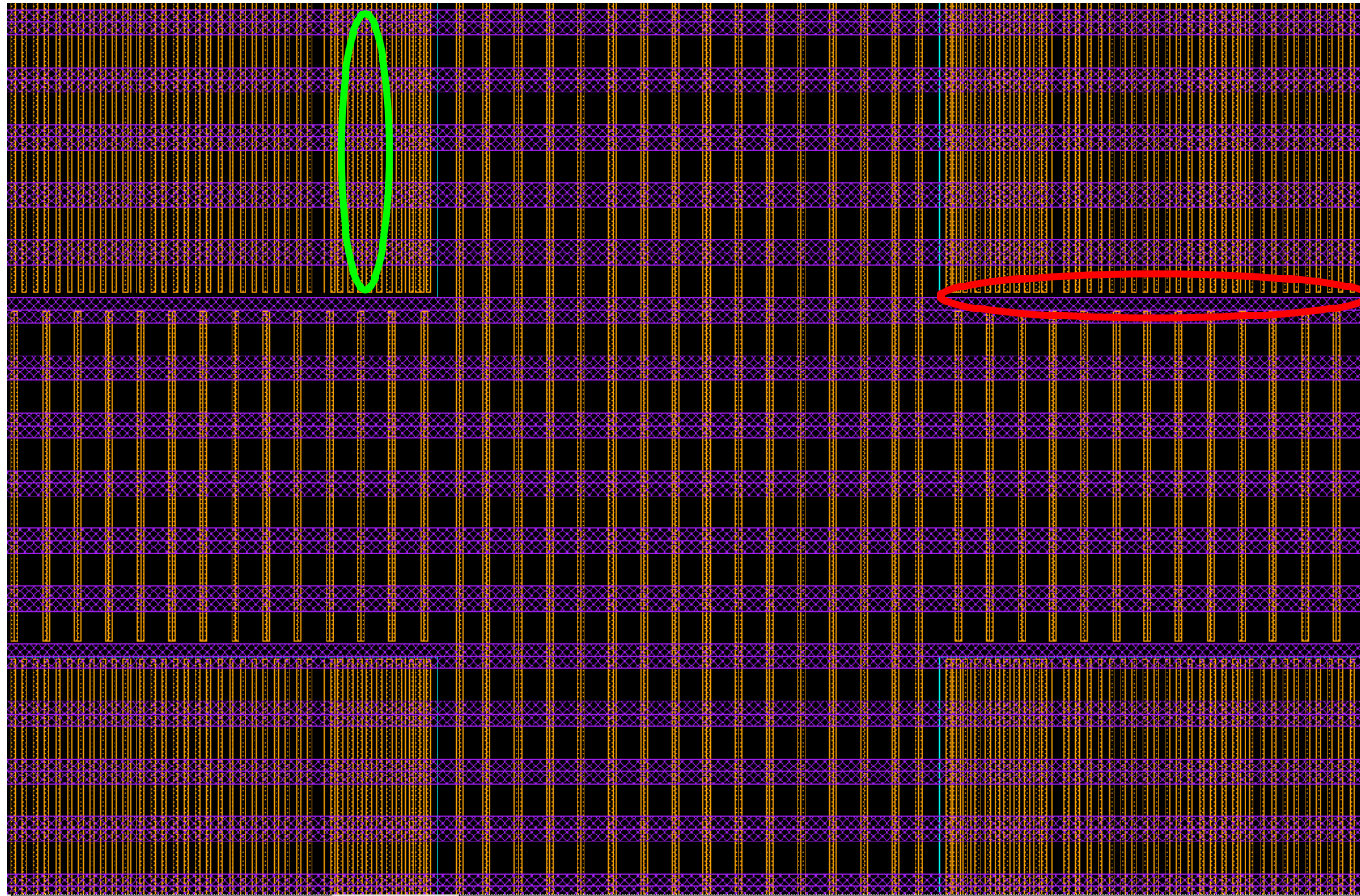


- M5 acts as power/ground pins of macros.
- To guarantee their power supply, M6 power straps are “pasted” on M5 pins.
- The top of the macros can only accommodate the horizontal M7 and the vertical M6 signal wires among the narrow M6 straps.



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Different Power Network Between Std Cells & Macros





Floorplan of L2 Cache

Size of L2 Cache:

$$Size = \underset{\substack{\uparrow \\ \text{words}}}{4096} \times \underset{\substack{\uparrow \\ \text{bits}}}{(72-8)} \times \underset{\substack{\uparrow \\ \text{ecc}}}{32} / 8 = 1MB$$

Needed wires for 1 way:

$$Num = (\underset{\substack{\uparrow \\ \text{D}}}{72} + \underset{\substack{\uparrow \\ \text{Q}}}{72} + \underset{\substack{\uparrow \\ \text{A}}}{12} + \underset{\substack{\uparrow \\ \text{ctrl}}}{13}) * 8 = 1352$$

But the channel can hold:

$$Num = \underset{\substack{\uparrow \\ \text{width}}}{89.4} \times (1 / \underset{\substack{\uparrow \\ \text{pitch}}}{0.2} \times \underset{\substack{\uparrow \\ \text{M2+M4}}}{2}) = 894$$

At most accommodate
890 wires for the
89.4um channel





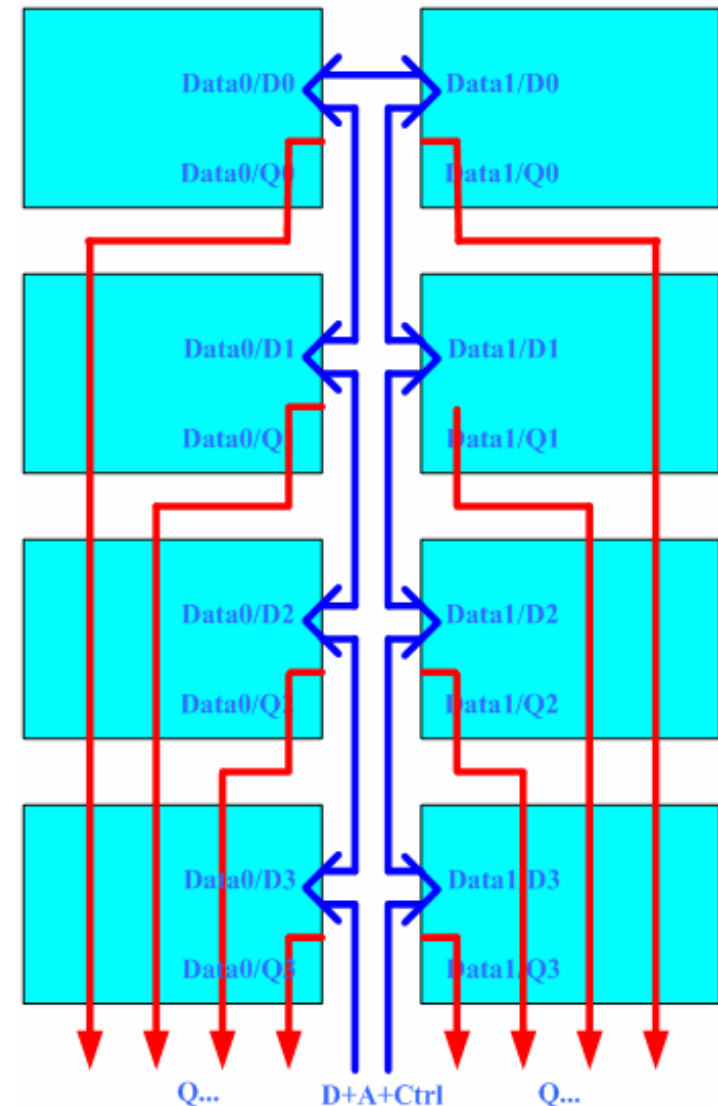
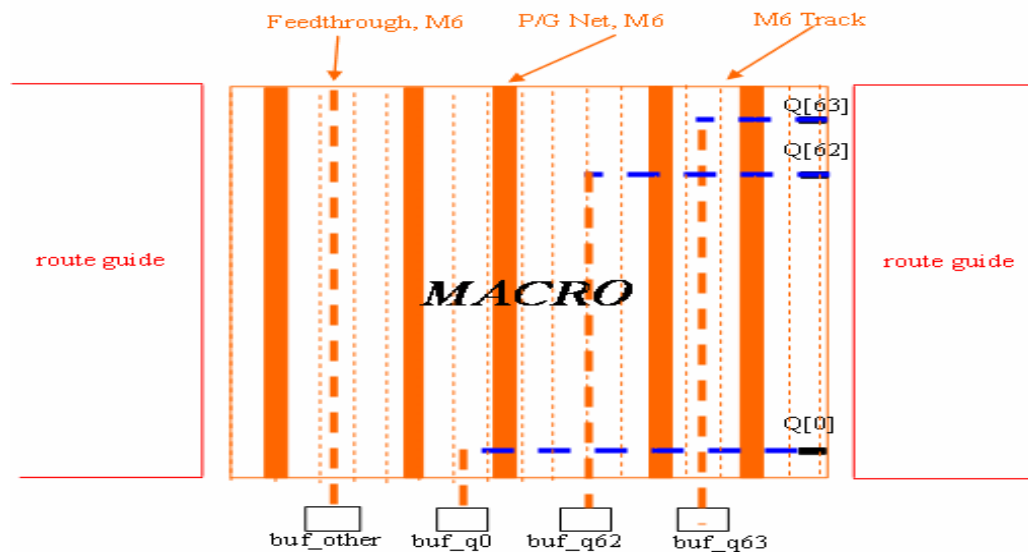
Challenge for the Routing

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- If the wires related to Q pins are passed over the macros, the channel would accommodate:

$$(72+12+13)*8=776$$

It is less than 890 so feasible.
- But the wires related to Q pins can only pass through the narrow space among the M6 straps, and the available routing resource are not on the tracks! So tools can not help.





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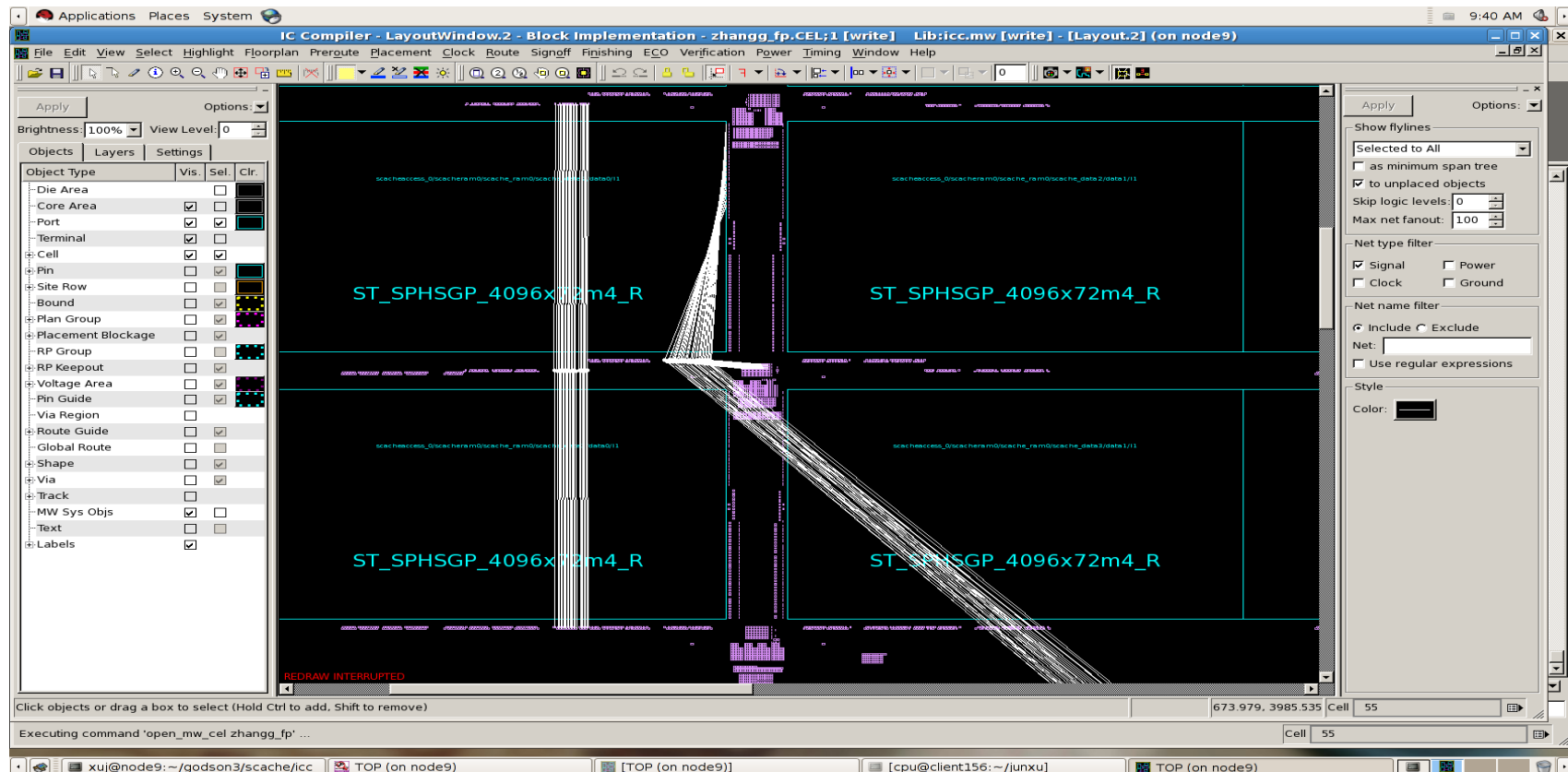
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Insert Guide Buffer

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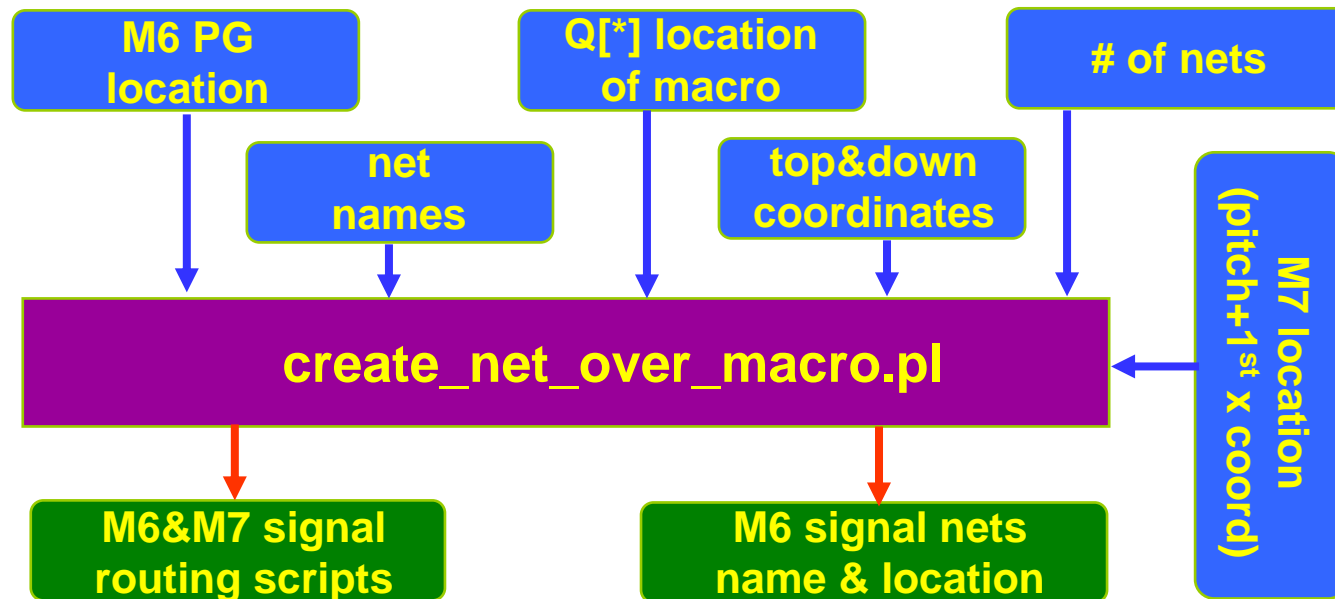
- Include them in the RTL codes and name them specifically.
- Use “set_cell_location” to place them during floorplan.





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Write Perl to Generate the Routing Commands



- Primary data structure
 - `array_pin_x[]` & `array_pin_y[]`: `Q[*]` location
 - `m6_x[]`: M6 signal location
 - `m7_y[]`: M7 signal location



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Input pattern and data structure building

Input file recording location of Q[*]:

```
... ..  
scacheaccess_0/scacheram0/scache_ram0/scache_data0/data0/l1/Q[16] {661.630 5140.450} {662.150 5140.550}  
scacheaccess_0/scacheram0/scache_ram0/scache_data0/data0/l1/Q[17] {661.630 5143.250} {662.150 5143.350}  
scacheaccess_0/scacheram0/scache_ram0/scache_data0/data0/l1/Q[18] {661.630 5150.250} {662.150 5150.350}  
... ..
```

↑ ↑ ↑ ↑ ↑
index **llx** **lly** **urx** **ury**

$$\$array_pin_x[\$index] = (llx + urx) / 2$$
$$\$array_pin_y[\$index] = (lly + ury) / 2$$

Input file recording location of M6 PG straps (sorted by x coord):

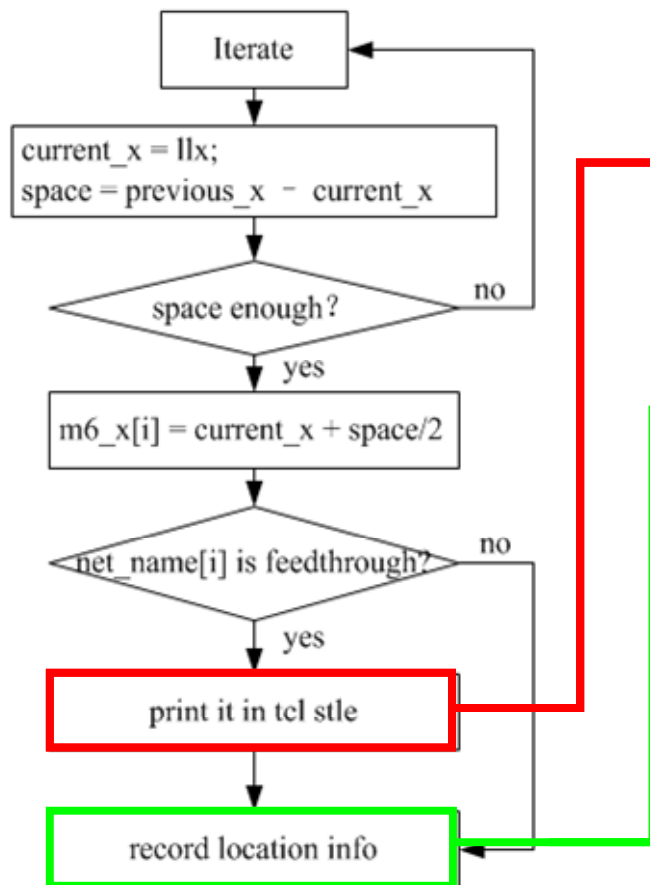
```
... ..  
create_net_shape -no_snap -type path -net gnd -layer M6 -datatype 0 -path_type 0 -width 0.7 -route_type pg_strap  
                  -points {{ 661.635 223.31} {661.635 649.51}}  
create_net_shape -no_snap -type path -net vdd -layer M6 -datatype 0 -path_type 0 -width 1.44 -route_type pg_strap  
                  -points {{ 660.125 223.31} {660.125 649.51}}  
create_net_shape -no_snap -type path -net gnd -layer M6 -datatype 0 -path_type 0 -width 0.66 -route_type pg_strap  
                  -points {{ 658.645 223.31} {658.645 649.51}}  
... ..
```

 ↑ ↑ ↑ ↑ ↑
llx **lly** **urx** **ury** **width**



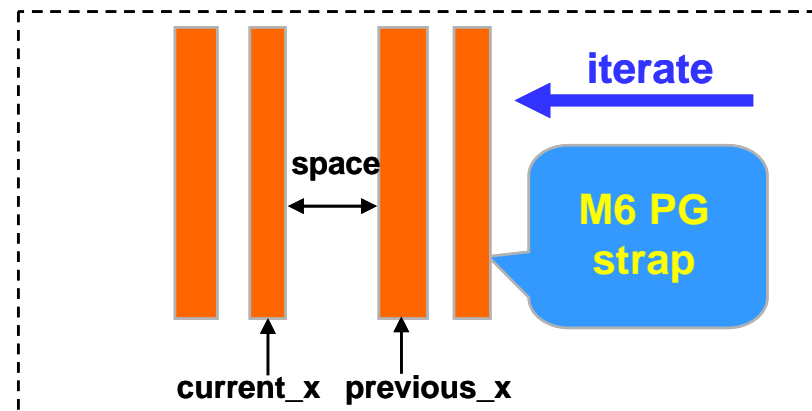
Generate M6_x[]

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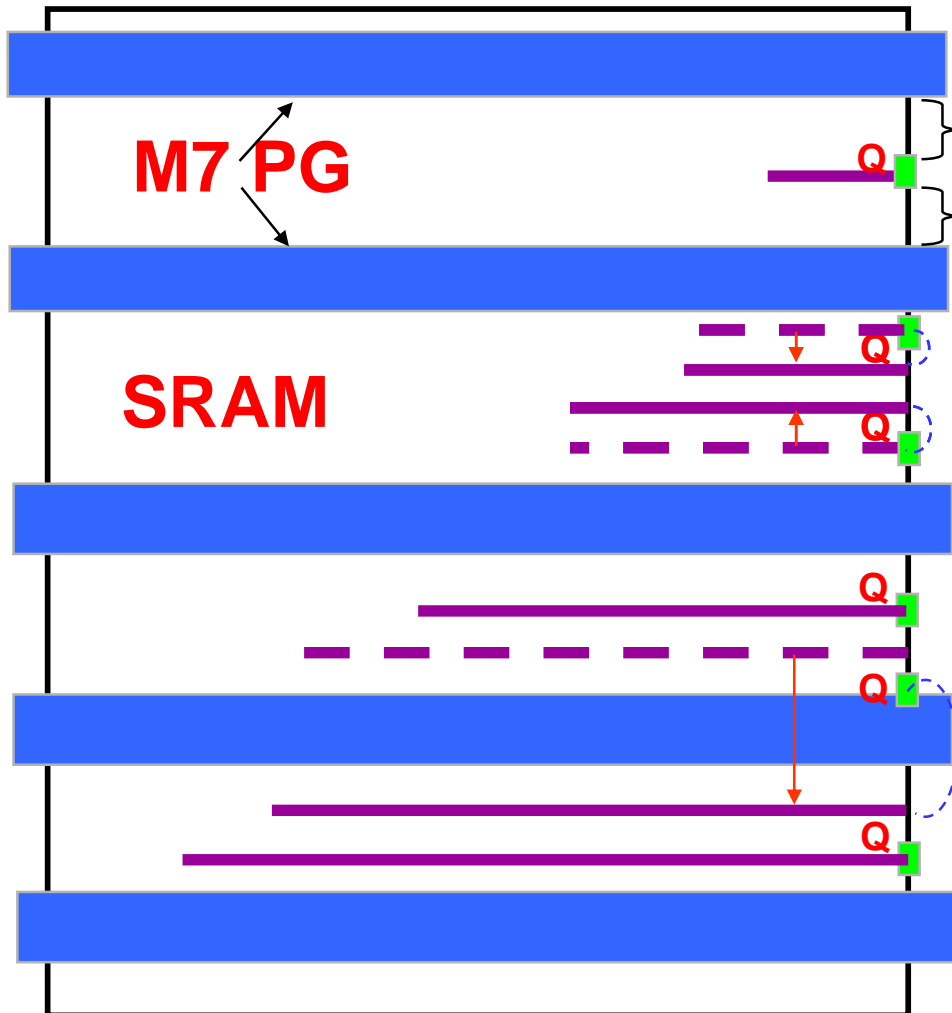
```
print <<EOF;
create_net_shape -no_snap -type path \
-net $net_name[$index] \
-layer M6 -datatype 0 -path_type 0 \
-width $this_width -route_type user_enter \
-points {{ $this_x $this_bottom} {$this_x $this_top}}
EOF
```

```
# Output to another file for later use
print OUTPUT "$net_name[$index] $this_x
$this_bottom $this_top", "\n";
```





Generate M7_y[]



(a) Both spaces are safe

(b) When only one is safe,
add one offset to meet the
minimal requirement

(c) When it conflicts with
the up net, continue to
adjust!



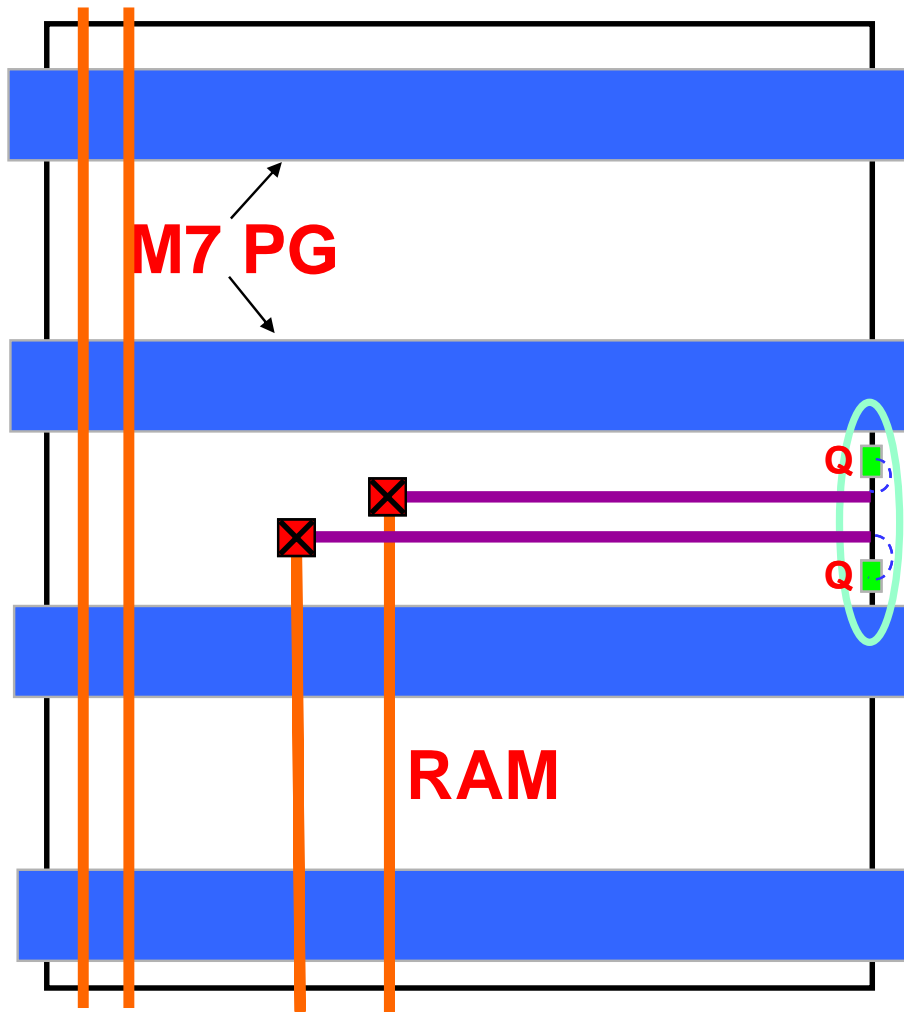
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Code Clip for M7_y[] Generation

```
for ($index = $NUMBER-1; $index >= 0; $index--) {  
    $m7_pg_low = sprintf "%d", ($array_pin_y[$index]-$m7_pg_first_y)/$m7_pg_pitch;  
    $low_m7_pg_loc = $m7_pg_low*$m7_pg_pitch + $m7_pg_first_y;  
    $high_m7_pg_loc = $low_m7_pg_loc + $m7_pg_pitch;  
    $high_space = $high_m7_pg_loc - $q_pin_y[$index];  
    $low_space = $q_pin_y[$index] - $low_m7_pg_loc;  
  
    if ($high_space >= $safe_distance && $low_space >= $safe_distance) {  
        $m7_y[$index]=$q_pin_y[$index];  
    } elseif ($high_space < $safe_distance) {  
        $m7_y[$index]=$high_m7_pg_loc - 2.25 - 0.7;  
    } else {  
        $m7_y[$index]=$low_m7_pg_loc + 2.25 + 0.7;  
    }  
  
    ##adjust m7_y[]  
    if (($m7_y[$index+1] - $m7_y[$index])<1.2) {  
        $m7_y[$index] = $m7_y[$index+1] - 1.2;  
        if (($m7_y[$index] - $low_m7_pg_loc) < $safe_distance ) {  
            $m7_y[$index]=$low_m7_pg_loc - 2.25 - 0.7;  
        }  
    }  
}
```



Drawing M7, M6 wires and Via67 once M6_x[]&M7_y[] are done



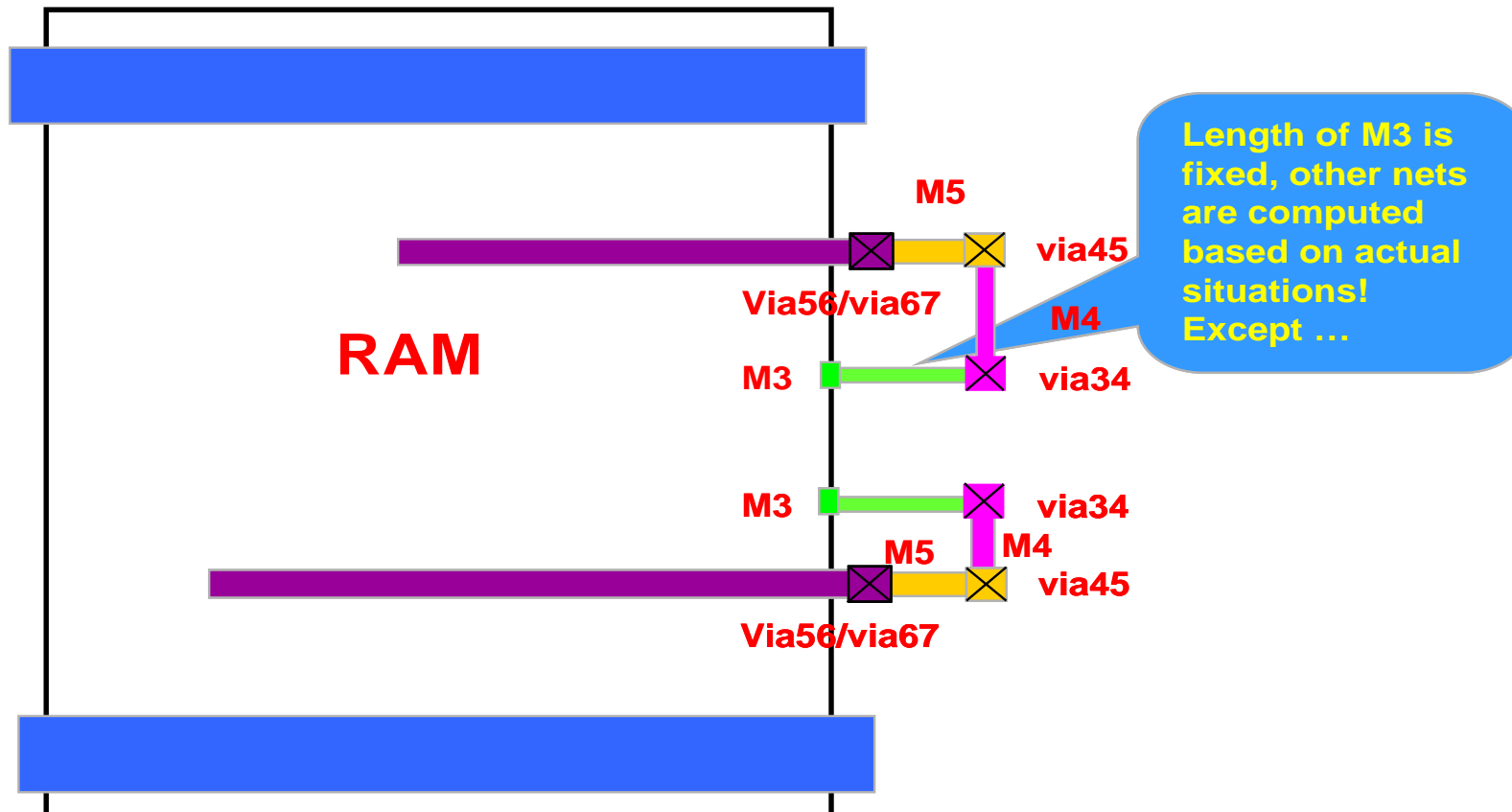
```
print <<EOF;
create_net_shape -no_snap -type path \
-net $dgr_net[$net_index] \
-layer M6 -datatype 0 -path_type 0 -width
$this_width -route_type user_enter \
-points {{ $m6_x[$net_index]
$this_bottom} {$m6_x[$net_index]
$m7_y[$net_index]}}
```

```
create_net_shape -no_snap -type wire \
-net $dgr_net[$net_index] \
-layer M7 -datatype 0 -path_type 0 -width
$this_width -route_type user_enter \
-length $m7_length \
-origin {$m6_x[$net_index]
$m7_y[$net_index]}
```

```
create_via -no_snap -type via \
-net $dgr_net[$net_index] \
-master AVNT_via6 -route_type
user_enter \
-at {$m6_x[$net_index]
$m7_y[$net_index]} -orient N
EOF
}
```



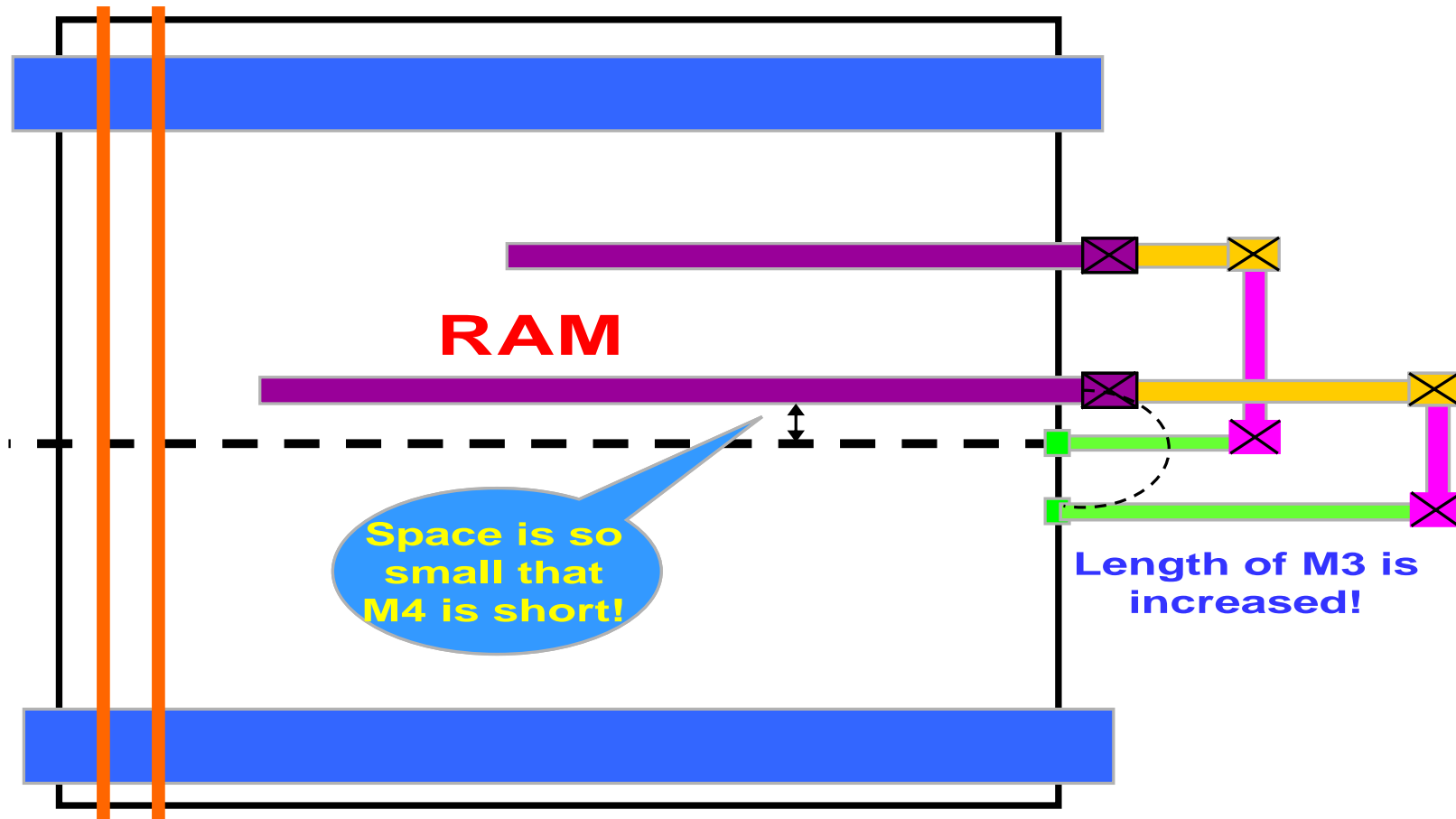
Connecting Q pins with M7 wires - situation 1





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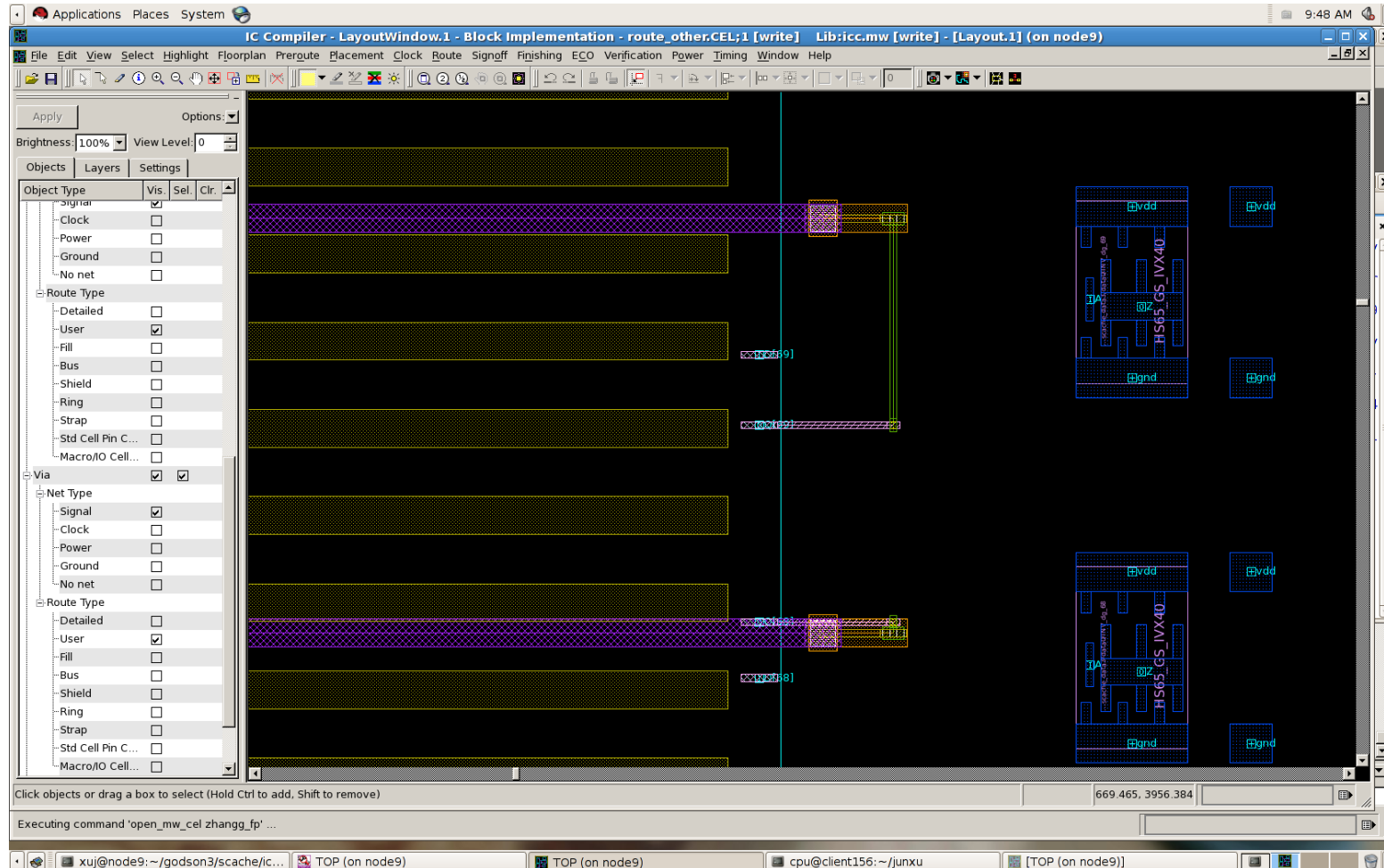
Connecting Q pins with M7 wires - situation 2





Actual picture

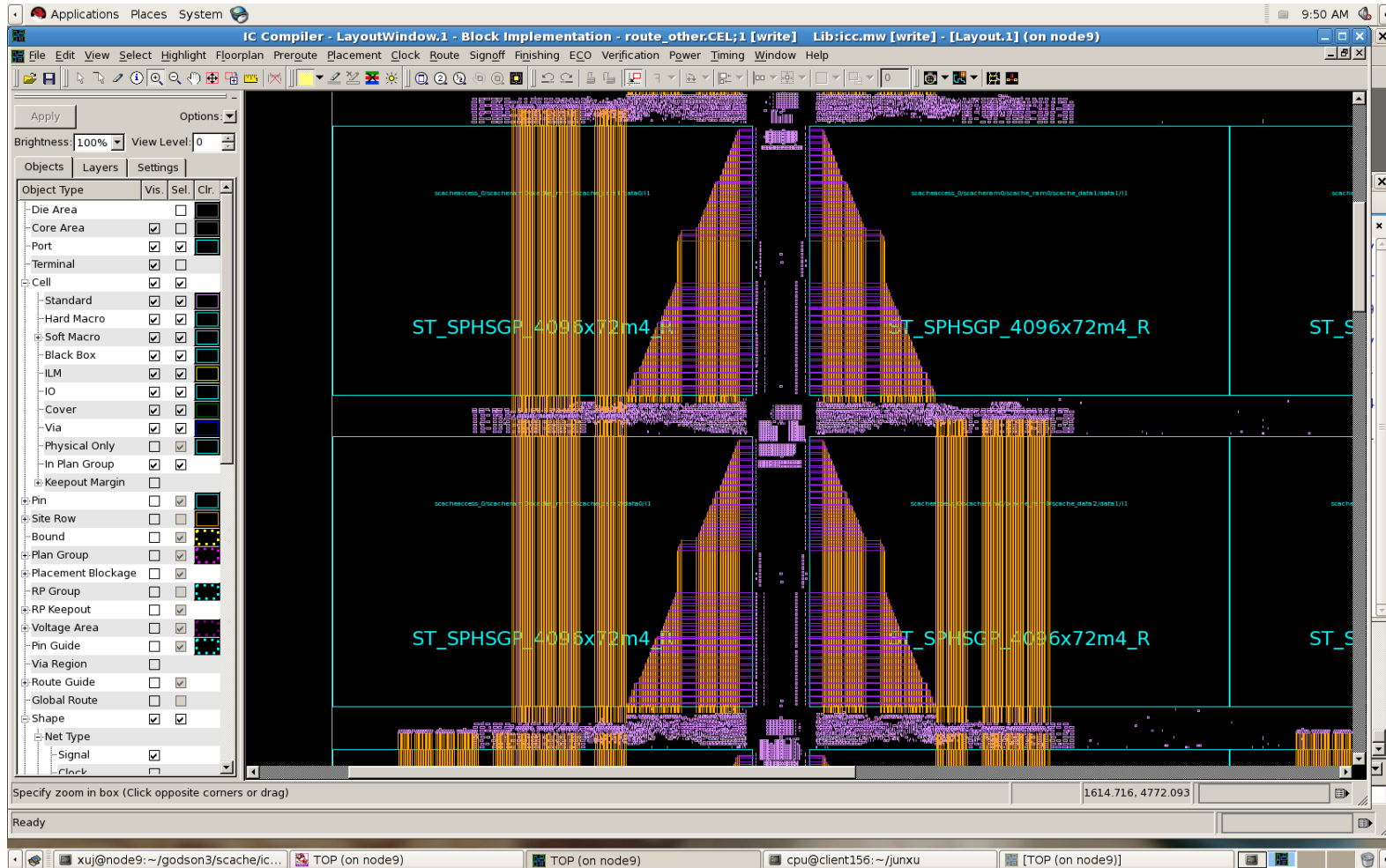
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Actual routing wires

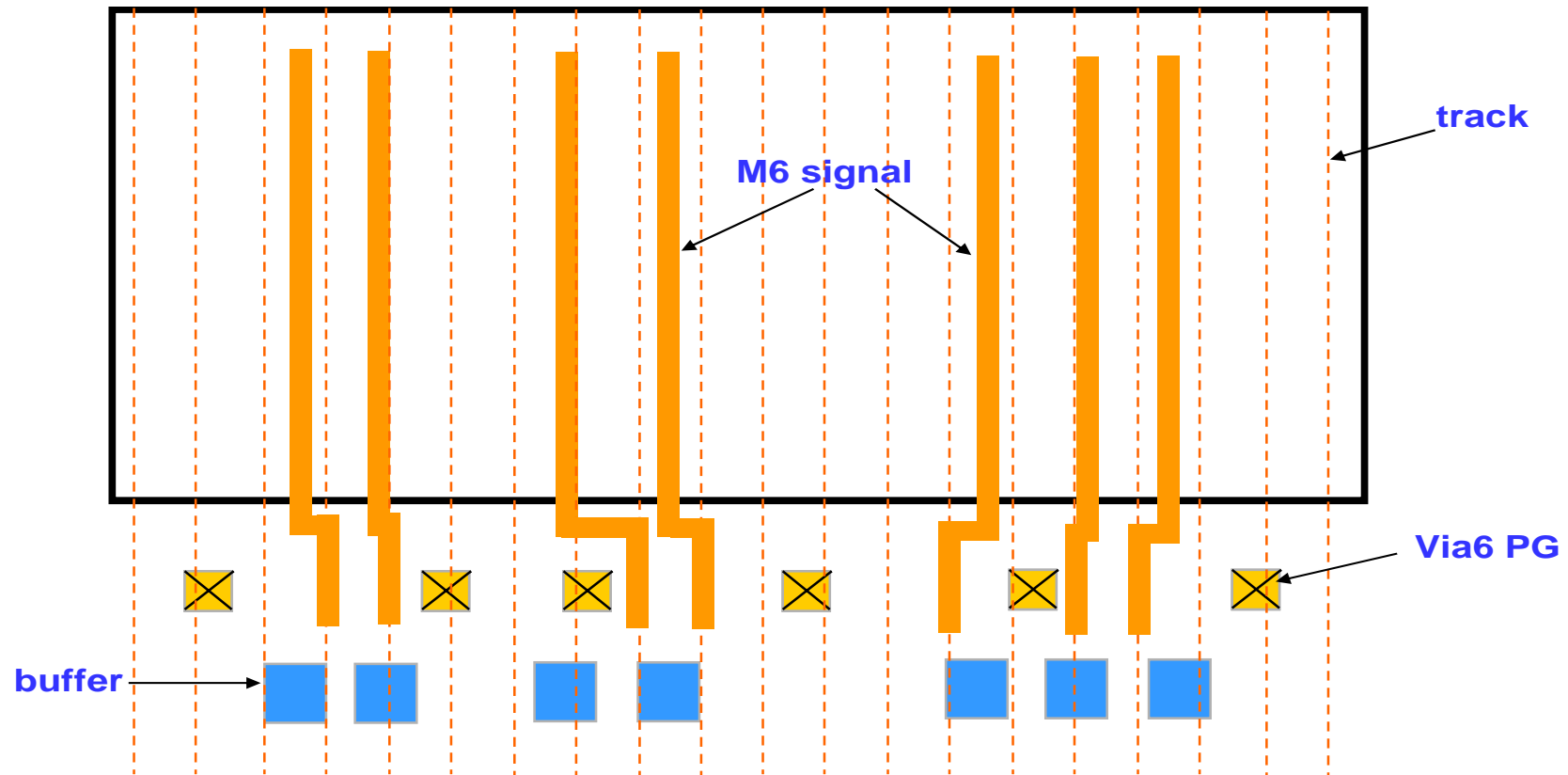
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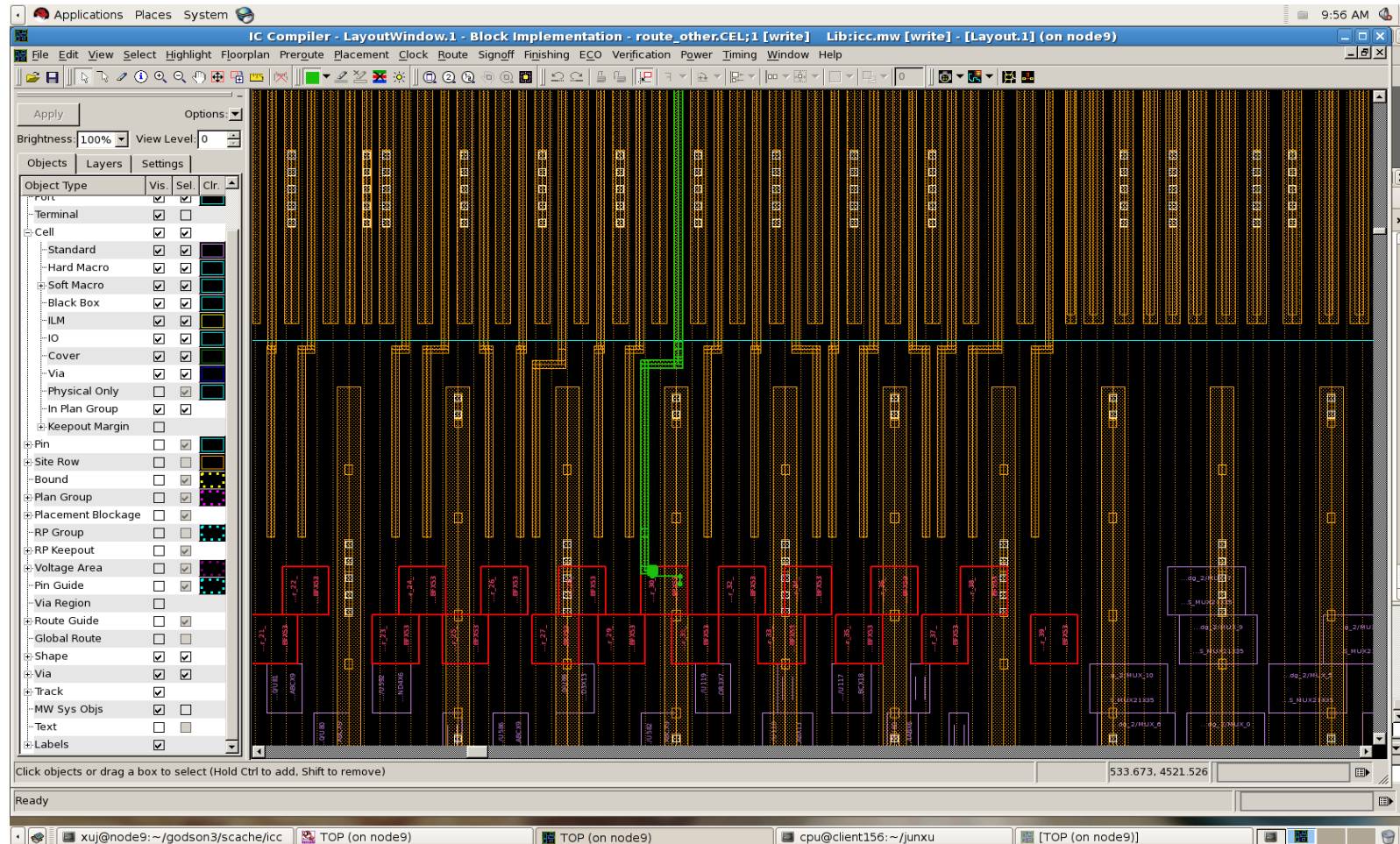
Drag off-track wires on tracks





Actual wires

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Develop Once & Enjoy Multiple Times

	Pure ASIC Flow	Only Inserting Guide Buffers	Pre-route w/o dragging off-track wires	Semi-Custom Flow
# of cells (post-synthesis)	72,528	100,384	100,384	100,384
# of nets (post-synthesis)	84,879	112,735	112,735	112,735
# of pre-placement cells	0	27856	27856	27856
# of pre-route nets	0	0	6160	6160
# of search & repair	50	50	50	5
# of DRC violations	>50,000	>20,000	>7,000	0
Place & Route Time (hours)	>20	>20	>20	3



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Experience & Suggestion

- Designs are designed by designers not tools.
- Designers should understand both design characteristics and tool features in order to use semi-custom flows.
- EDA vendors should provide more programmable interfaces for users to extend the capability of the tools.



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Thanks!