

FIXING HOLD IN TEST SHIFT MODE WITHOUT USING BUFFERS

AREA OF APPLICATION: DIGITAL DESIGN HAVING SCAN FLOPS

IMPLEMENTATION METHOD : USING TCL SCRIPT

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Traditional Method of Hold Fixing in shift Mode

- **At least as many buffers are added as the number of violations.**
- **This approach used during the implementation stage for hold fixing has following impact :**
 - **Increase in Design Utilization.**
 - **More power consumption in a design.**
 - **Degradation of critical timing paths in congested designs.**
 - **Post Mask Hold Timing ECO's consume spare buffers.**

New Approach to Fix Hold in shift Mode

- **Scan reordering is used in controlled way to fix violations.**
- **What is Desired End Result**
 - **To reduce the TNS for Hold.**
 - **To preserve the WNS for Hold.**
 - **No new transition/Capacitance violations.**
 - **No congestion hot spots.**
- **Benefits of this approach**
 - **Overall Gain in terms of design utilization.**
 - **Preserve the Setup Slack , No cells moved.**
 - **Reduces Power Consumption.**

New Approach to Fix Hold

- Identify the Violating Path.
- Trace the scan chain from violating flop.



Fig 1

- Reorder the scan chain to fix the violation.

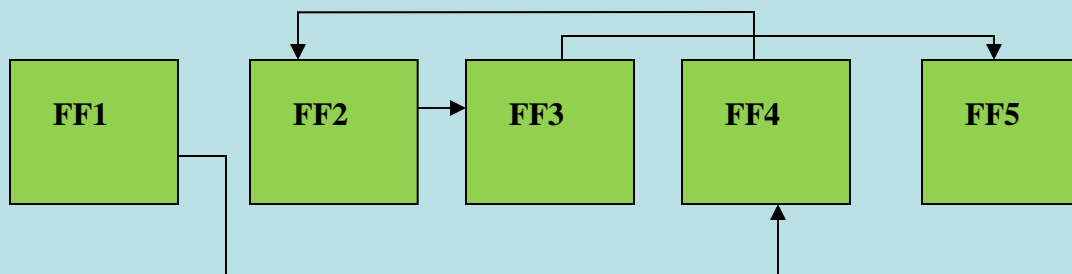


Fig 2

- Do not touch paths already fixed for hold

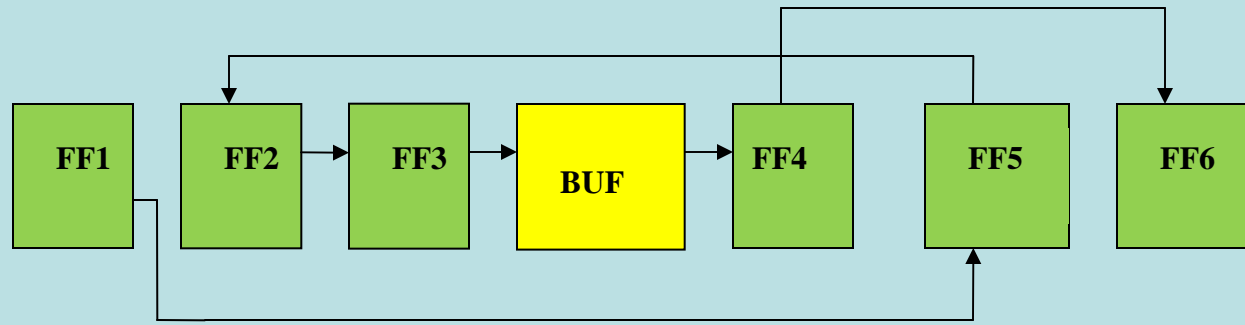


Fig3

- While reordering make sure the local skew for new pair of flops is favourable for Hold.

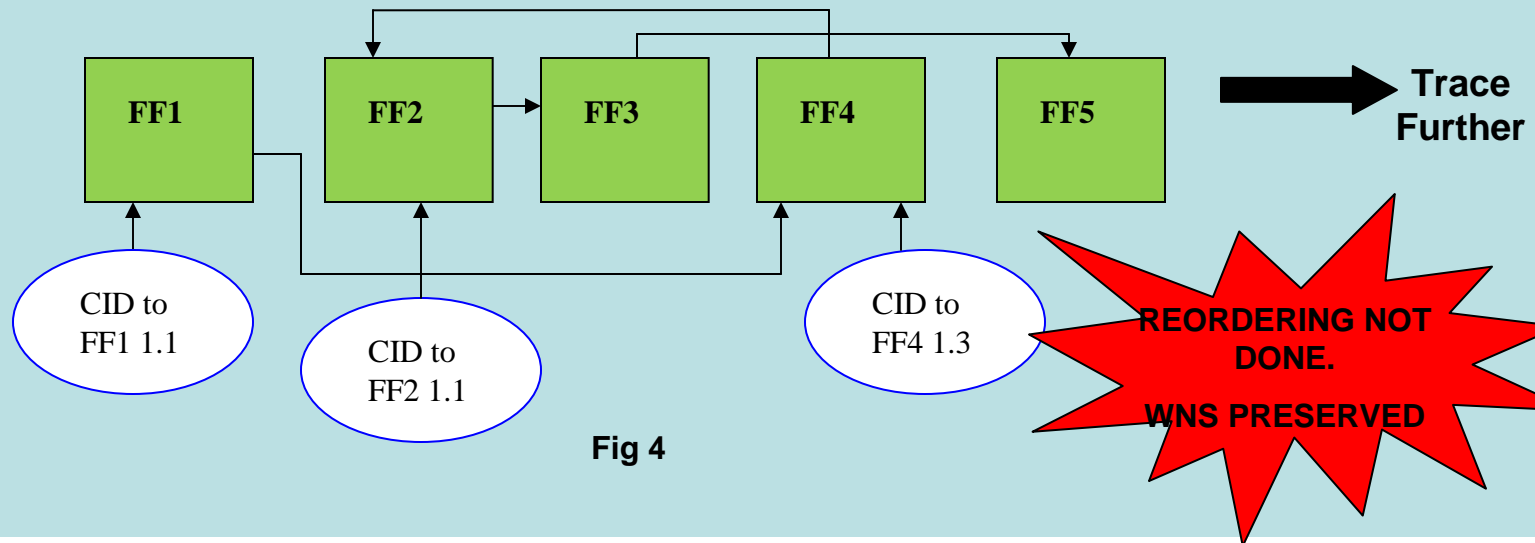
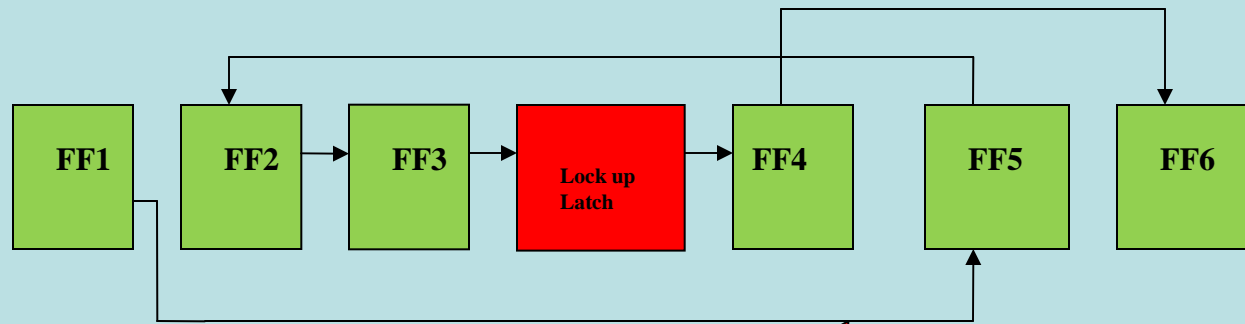


Fig 4

- **DFT Guidelines are respected.**



**WRONG : Never cross a
lock up latch or any
combinational cell to fix the
hold violation**

Fig 5

- **Maximum distance between reordered flops is not more then user given value.**

- Both forward tracing and reverse tracing is tried to fix the violation by scan reordering.

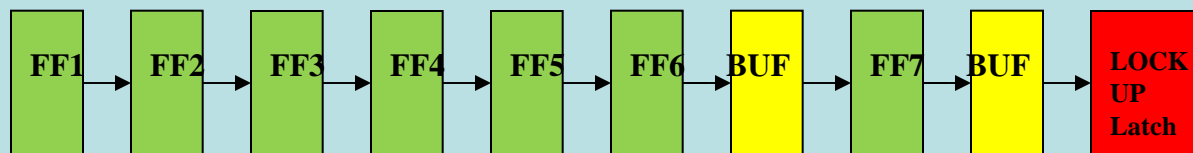


Fig 6

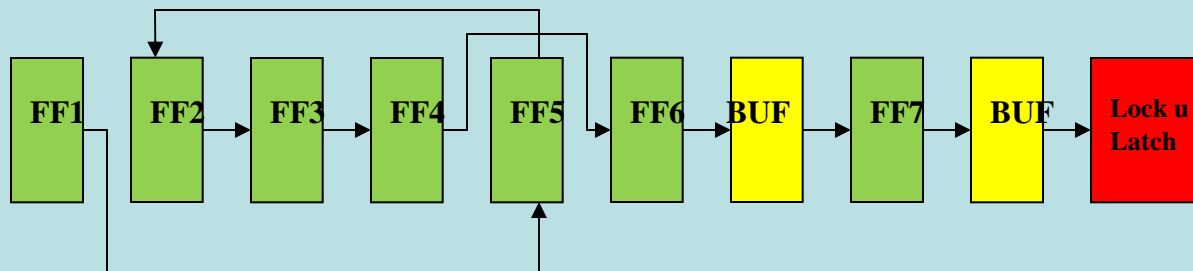
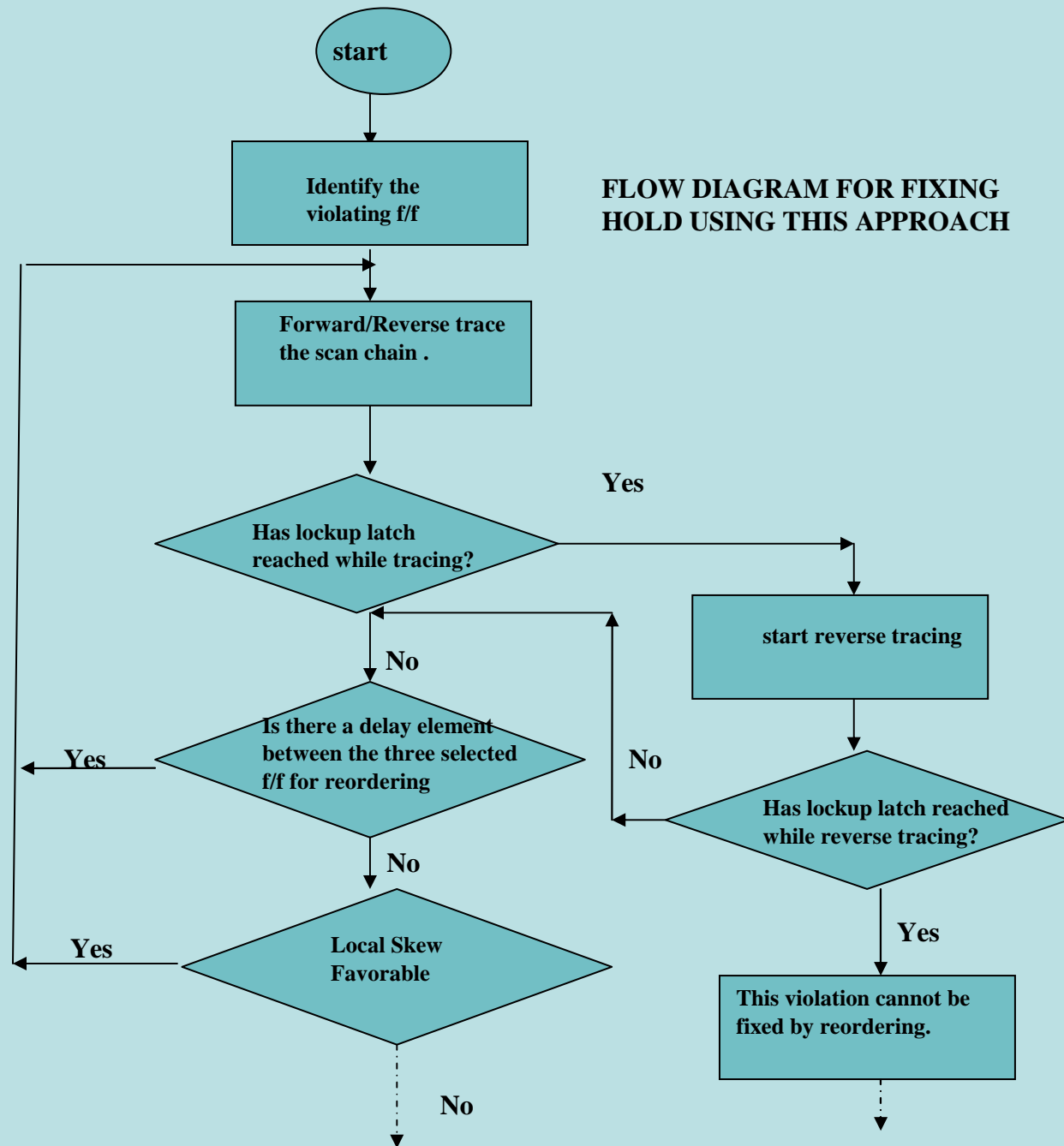
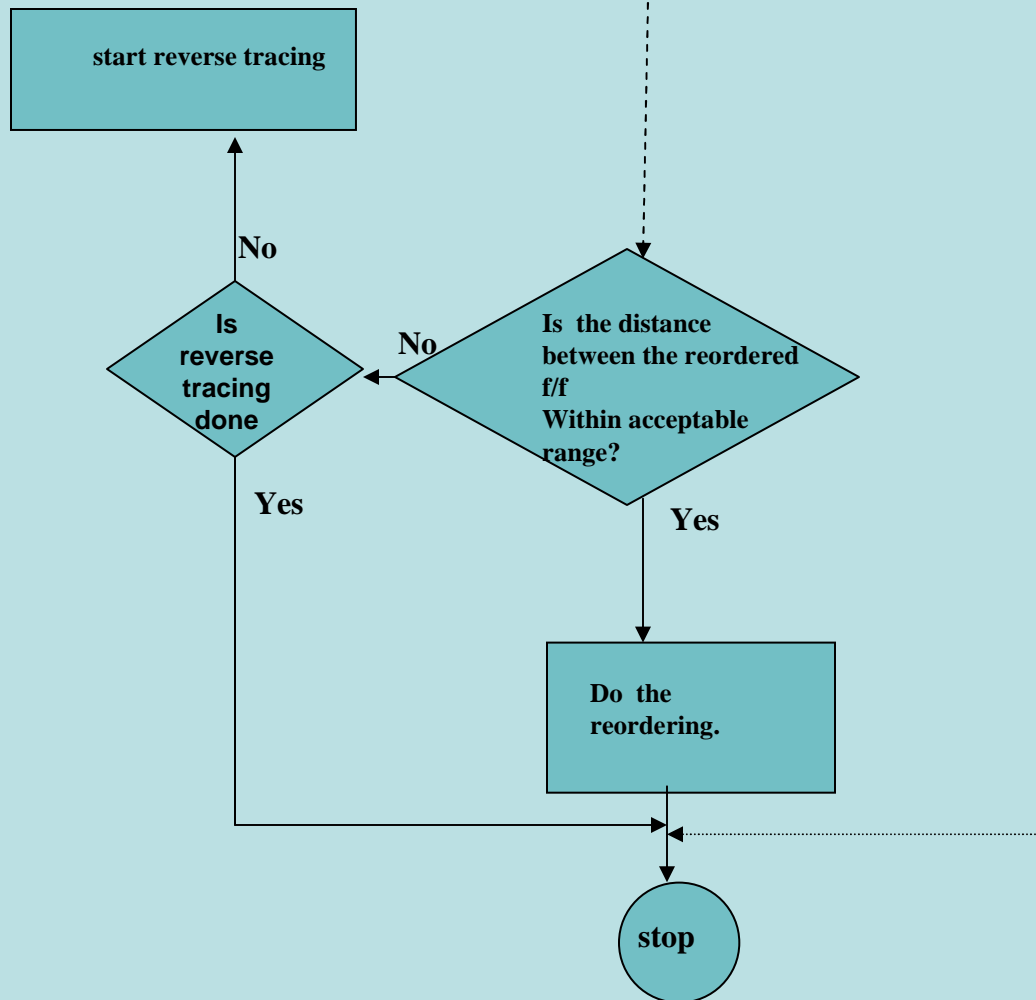


Fig 7





Results of 90nm STB chip

**90nm STB chip
28.62mm in size, 1.3M
instances.**

**Due to correlation
Difference Signoff TA
reported 3k violations
not seen in
implementation tool.**

**These 3K violations
were targeted using this
hold fixing approach.**

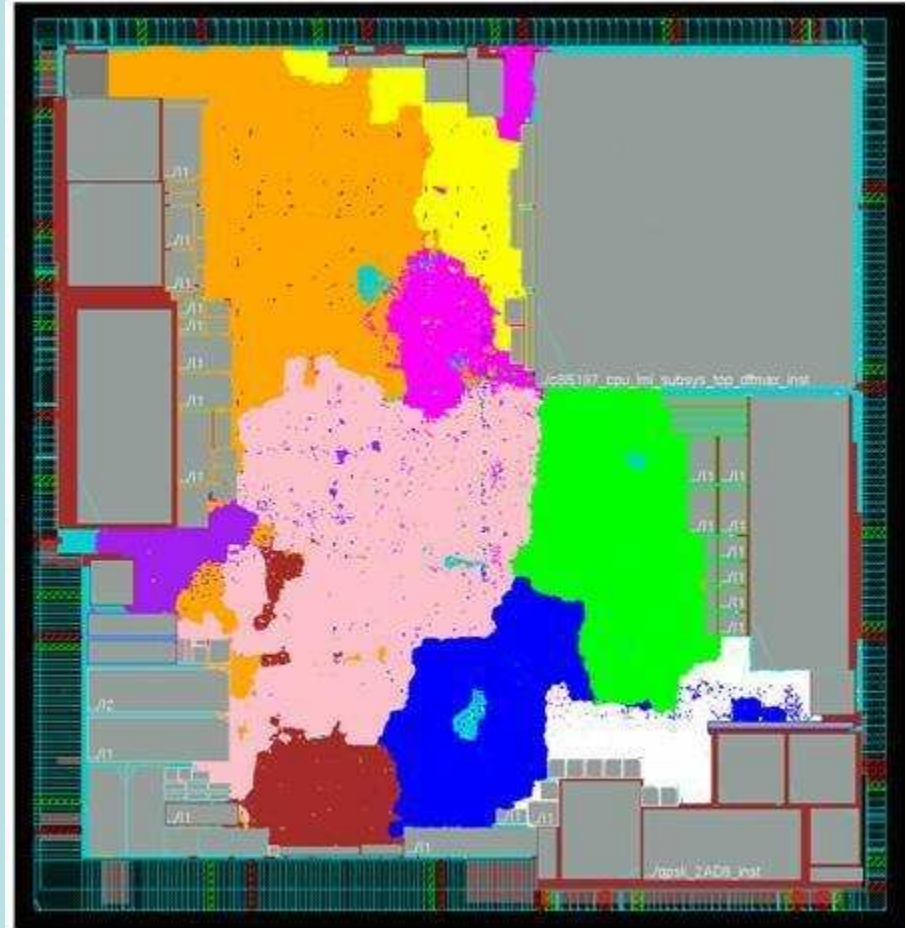


Fig 8

Results of STB, 90nm chip with 1.3M instances

(All results given in ns)

➤ Almost 60% of signoff TA violations were fixed using this approach.

➤ WNS preserved

➤ TNS Reduced

➤ Design was easily routed after scan reordering to fix hold.

Shift mode Hold Before Fixing Using this Technique

Hold mode	<u>all</u>	reg2reg	in2reg	reg2out	in2out	<u>clkgate</u>
WNS (ns):	-0.466	-0.088	-0.466	2.017	4.130	-0.252
TNS (ns):	-37.207	-17.446	-19.762	0.000	0.000	-10.904
Violating Paths:	2224	2079	145	0	0	98

Table1: Hold before fixing

Shift mode Hold After Fixing Using this Technique

Hold mode	<u>all</u>	reg2reg	in2reg	reg2out	in2out	<u>clkgate</u>
WNS (ns):	-0.466	-0.087	-0.466	2.018	4.131	-0.252
TNS (ns):	-27.108	-7.343	-19.764	0.000	0.000	-10.908
Violating Paths:	1005	860	145	0	0	98

Table2 : Hold after fixing

➤ Only 4 setup violations after fixing because of transition violation on test path.

These were easily fixed.

Functional mode Setup before fixing

Setup mode	<u>all</u>	reg2reg	in2reg	reg2out	in2out	<u>clkgate</u>
WNS (ns):	-3.721	0.096	-0.767	-3.721	-1.496	0.101
TNS (ns):	-351.21	0.000	-158.737	-192.473	-3.409	0.000
Violating Paths:	1525	0	1082	443	8	0

Table3 : Setup before fixing

Effect on functional mode Setup After Hold fixing Using this Technique

Setup mode	<u>all</u>	reg2reg	in2reg	reg2out	in2out	<u>clkgate</u>
WNS (ns):	-3.721	-0.544	-0.767	-3.721	-1.496	0.101
TNS (ns):	-352.719	-1.093	-158.886	-192.741	-3.438	0.000
Violating Paths:	1528	4	1081	443	8	0

Table4 : Setup after fixing

InstPin	Max Tran Time	Tran Time	Tran Slack
c6s4300_top_0/u_core/u_fpu/u_fvec/u_dp16/ u_fmml_1xediff/wb_q_regx26x/TI	3.130	4.002r/1.439f	-0.873r/1.691f
CMP_IC_STBGRP2/GROUP_1xFHS14_GC/ c6sb0_genconv_0xc6sb0_rqmu_0/ rqmu_fifo_module_0xsoft_fifo_packet/ data_reg_regx6xx54x/D	1.066	1.071r/0.621f	-0.004r/0.446f

Table 5: Transition violation report

Only 4 transition violations in shift Mode which caused setup violation. These were easily fixed.

Only 5 new crosstalk violations were reported these were easily fixed by double spacing the nets.

Results of 65nm STB chip

**65nm STB SOC 43mm
in size.**

**3.16M Instances , 247
Macros , 595 IO's**

**New approach was
used to fix hold
violations of one of clk
groups @400MHZ**

**Hold fixing on clk
group by buffer
addition was
degrading the setup
slack.**

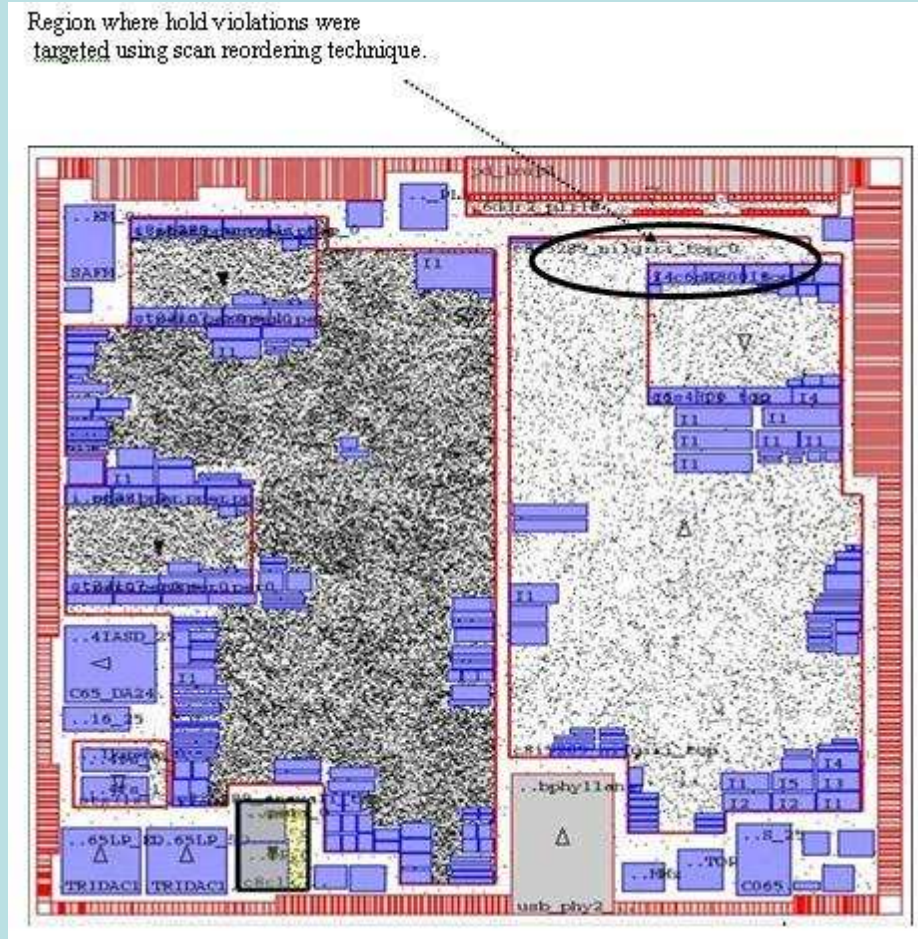


Fig 9

Results of 65nm STB chip

(All results given in ps)

Shift mode hold before reordering f/f					
Hold mode	Endpoints	Violating Endpoints	Violating Endpoint %	WNS	TNS
pio3[7]_SCAN_SHIFT	29042	632	2.2	-158.0	-17188

Shift mode hold after reordering f/f					
Hold mode	Endpoints	Violating Endpoints	Violating Endpoint %	WNS	TNS
pio3[7]_SCAN_SHIFT	29042	342	1.2	-158.0	-12065

- Almost 50% of Hold Violations were fixed for specific clock group using this approach.
- WNS for Hold was preserved.
- TNS for Hold was reduced.
- Design was easily routed after scan reordering to fix hold.

Results of 65nm STB chip

(All results given in ps)

Functional setup time before fixing hold

Shift mode	Endpoints	Violating Endpoint	Violating Endpoint %	WNS	TNS
Clk lmi reg FUNC FLAT	21440	632	2.2	-85.0	-16752

Table 6

Functional setup time after hold fixing

Shift mode	Endpoints	Violating Endpoint	Violating Endpoint %	WNS	TNS
Clk lmi reg FUNC FLAT	21440	632	2.2	-85.0	-16758

Table 7

- WNS for setup preserved.
- No new transition violation reported.

Results of 65nm STB chip (*All results given in ps*)

Slack histogram before fixing shift violation of test clock
PIO3[7]_SCAN_SHIFT

Slack	End Points	Total End Points
-175 - -151	1	1
-150 - -126	1	2
-125 - -101	16	18
-100 - -76	70	88
-75 - -51	47	135
-50 - -26	75	210
-25 - -1	422	632

Table 8

Slack histogram after fixing shift violation of test clock PIO3[7]_SCAN_SHIFT

Slack	End Points	Total End Points
-175 - -151	1	1
-150 - -126	0	1
-125 - -101	8	9
-100 - -76	63	72
-75 - -51	39	111
-50 - -26	42	153
-25 - -1	189	342

Table 9

Slack histogram Showing Number of Paths in Different Slack range.

Conclusion

- **50-60% of fixing done for test shift paths.**
- **No cells Added/Moved.**
- **WNS for Setup and Hold Time Preserved.**
- **No transition/Capacitance violation created on reordered nets.**
- **Power and Area Saved.**