

Objective of Interconnection BIST

Advantage of SiP

System-in-Package (SiP), which consists of **multiple dies in a single package**, is becoming more important for digital consumer appliances.

- (1) High yield for each system component in its most appropriate technology.
- (2) Shorten time-to-market.

SiP and Memory KGD (Known-Good-Die)

- (1) The overall yield of SiP depends on the probability of individual die and interconnection between dies being defect free.
- (2) Require every die in the SiP exhibits a very low defect level.
- (3) **Only KGD components are used, we focus on the faults that originate from the assembly process.**

Motivation

We present the design and implementation of an interconnection BIST embedded in ASIC chip designed for SiP (as shown in Figure 1).

- (1) Memory dies are tested at wafer-level and guaranteed as KGD.
- (2) **The BIST only test the interconnection between ASIC and memory die, but not for memory cell defect screening.**

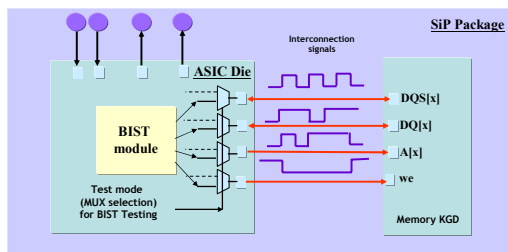


Figure 1. The embedded BIST in ASIC die to test the SiP interconnection

Features of Interconnection BIST

- (1) **Automatic BIST circuit generation to support various memory types, including SDRAM, DDRI and DDRII.**
- (2) Low hardware overhead and short testing time. For example, only 2.5K gate counts and 2K test cycle for 1Mx16 SDRAM testing.
- (3) High test coverage with short test pattern with unique data background.
- (4) Support diagnosis while fault occurs.

Proposed BIST Algorithm

STEP1, Write the **unique data** (as shown in Figure 2) into **walking 1/0 address sequence** (as shown in Figure 3)

STEP2, Read and compare data from walking 1/0 address sequence.

If address pins have defect, the previous write location will be overwritten, and the data read from that location in the second step will be different from expected data.

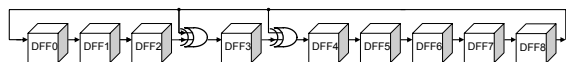


Figure 2. Data generator is a 9-bit-LFSR (initialized to 0x1) to generate 210 distinct 8-bits (DFF1 ~ DFF8) data patterns (including all 0, walking 1) and expand to 16-bits or 32-bits depending on memory data width.

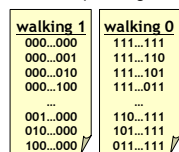


Figure 3. Walking 0/1 sequence

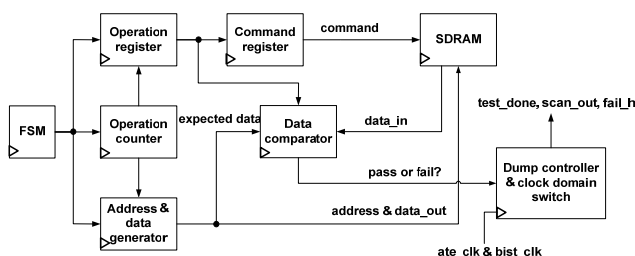


Figure 4. BIST Block Diagram

BIST Architecture

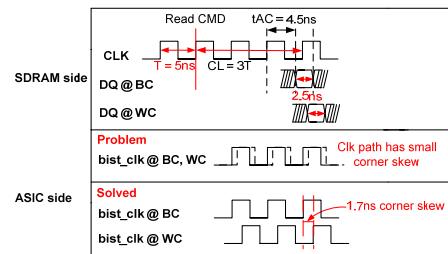
The **BIST architecture** and function blocks are shown in **Figure 4**. A Finite State Machine (FSM) controls dump circuit, pattern generator, initialize, and command logic.

- (1) Operation counter and register are used to arrange command, data, address, and read/write latency to satisfy specification.
- (2) Command register is used to decode memory access command by output of operation register.
- (3) The operation register also enables the data comparator which do the data capture and compare after read operation was asserted.
- (4) Once mismatch occurs, FSM could halt the following operation, and shift out the information on faulty location synchronous to tester clock for diagnosis by dump controller.

Discussion and future improvement

At-speed testing issue

There is a problem to capture the correct data in **all the corners**, due to **pad delay variation** and data keeps **valid only for 2.5ns** when SDRAM runs at 200Mhz.



Method1 (w/o DLL):
Insert delay cells to account for the 1.7ns corner skew (CLK pad + DQ pad)

Method2 (with DLL):
Use two kinds of DLL configuration, namely pattern A and B, to correspond to BC and WC respectively, and re-test by pattern B if the test result of A were fail.

Figure 5. Two methods for overcoming the large pad delay process variation

High quality (low DPPM) requirement

For higher quality demands (e.g. large panel product), more BIST algorithms can be implemented. For example, **CKB (CheckerBoard)** is inserted to our BIST to check some damage of KGD memory dies during assembling. The testing time of CKB is 23ms in 1Mx16 bits SDR SDRAM runs at 200Mhz.

Results

We have adopted our BIST methodology in many SiP project. The root cause of these **failure chips** is caused by **poor bonding wiring**. We have use the diagnosis feature to dig out the failure location in SiP. Without this BIST feature, we would suffer assembly defect.

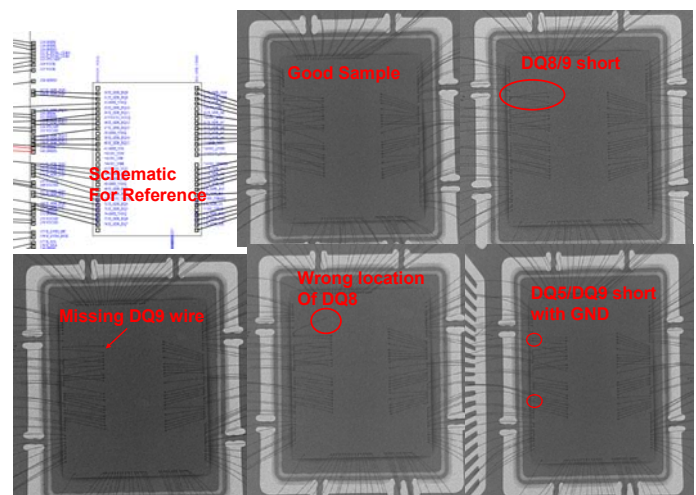


Figure 6. X-ray photo of the failure SiP diagnosis. A stacked SiP with one ASIC (the bottom die) and 1Mx16 SDRAM KGD (the top die).

The up-left figure is the SiP schematic. The up-middle photo is a good SiP sample, and the other 4 X-ray photos with different failure syndromes.