

# **Early Silicon Virtual Prototyping Design Methodology for SoC Design**

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# The Challenges of SoC Design

## ■ Today's SoC design trends

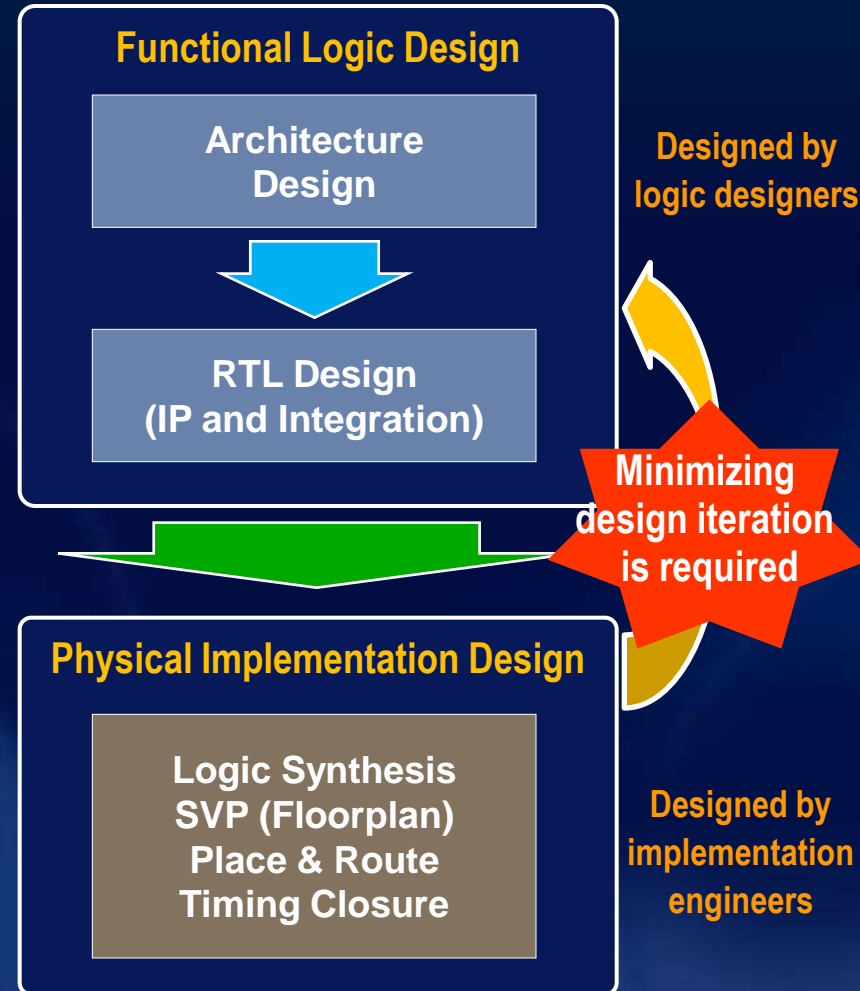
- High complexity and performance
- Shorten Time To Market

## ■ Motivation

- Separated design stages
  - Lack of design information sharing
- Re-spin from late design stage

## ■ Design Challenges

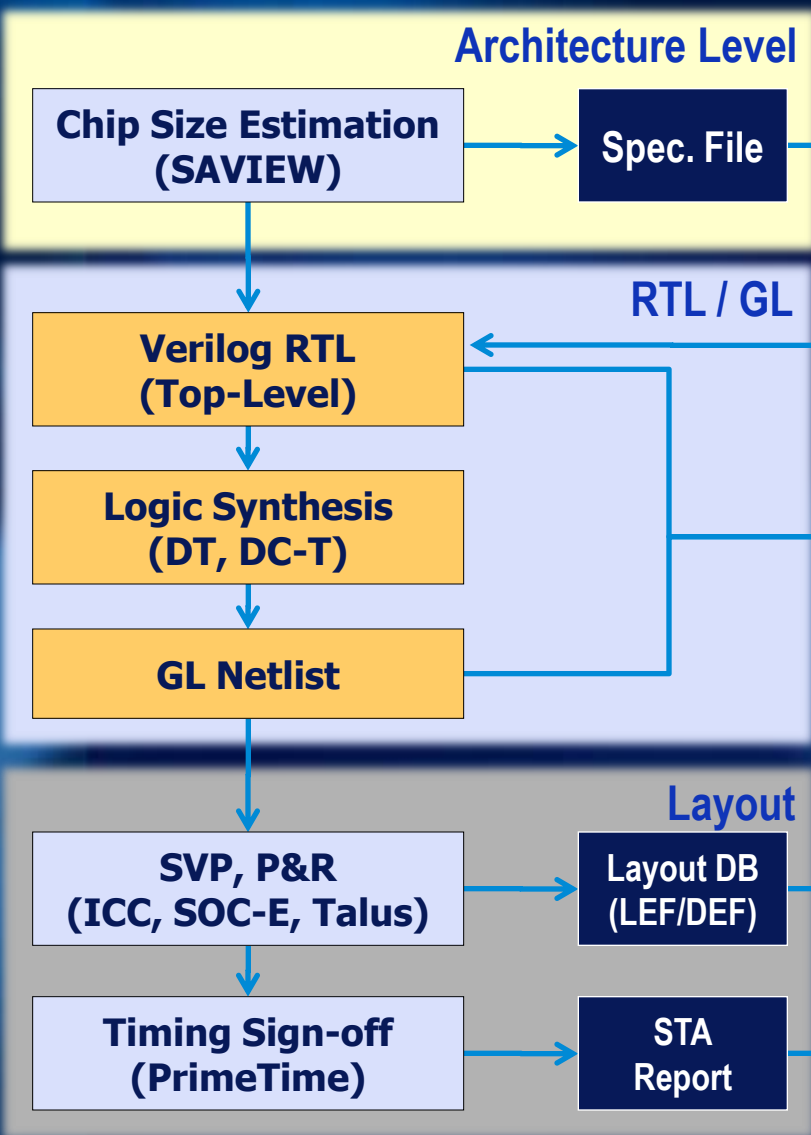
- More efficient and reliable design methods are required
- Fast feasibility analysis of physical design factors at earlier design stage
- Bridge to logic design and implementation
  - Design information sharing (functional, physical)



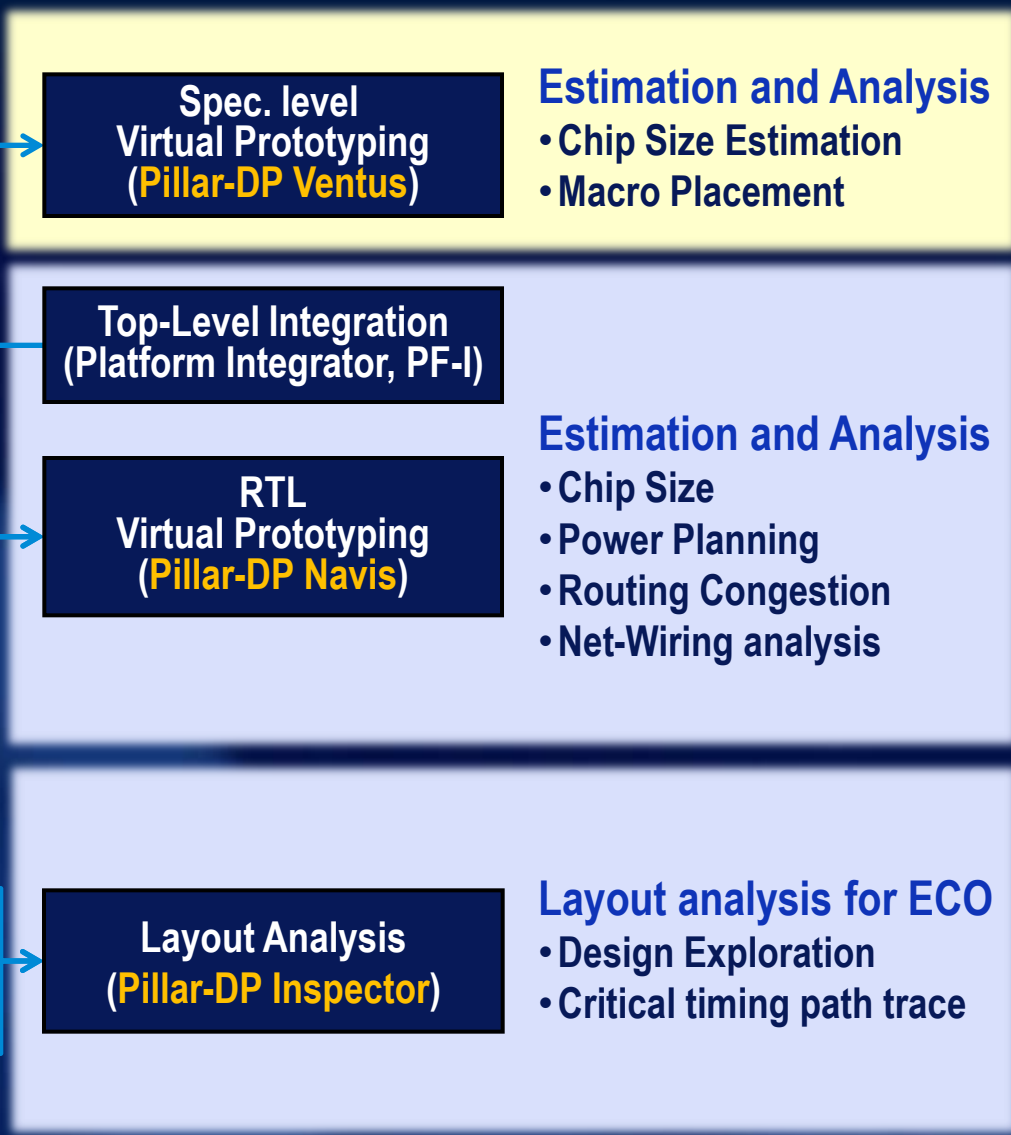
**Early Silicon Virtual Prototyping (E-SVP) design methodology is the key for reducing big design iterations**

# E-SVP Design Methodology and Flow

## Conventional SoC design flow



## E-SVP design flow

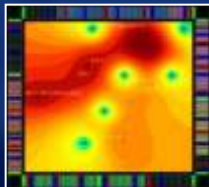


# Physical Design Analysis at Early Design Stage

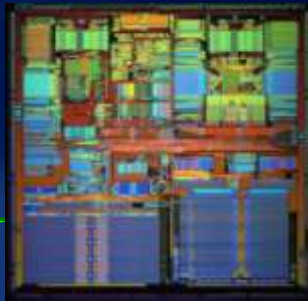
## E-SVP design methods based on Floorplan

### Chip size estimation

- Block level specification
- Hard / soft macros
- I/O pads

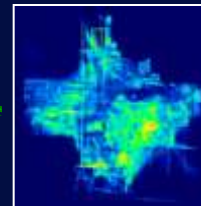


### *Estimation → What-If Analysis*



### Congestion analysis

- Hot-spot routing congestion
- Congestion and redistribution analysis



### Power planning with estimation

- Power estimation and analysis
- I/O pads configuration and optimization
- Power network prototyping

### Net-wiring analysis

- Connectivity analysis
- Inter-block delay for nets

- Minimization of the unnecessary design iterations with E-SVP design methods
- Predictable design turn-around-time

# Floorplanning and Chip size Estimation

## Architecture Specification

- Block level specification
- Design constraints
- Target utilization



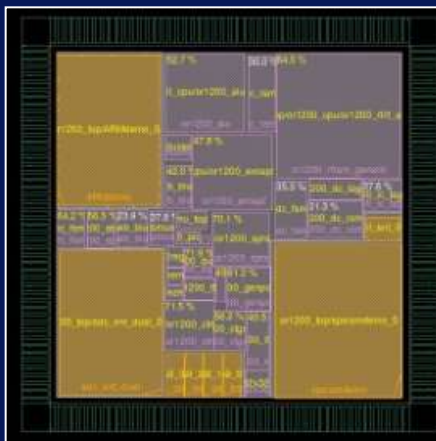
## Process tech. model libraries

- Transistor (P/N) geometries
- Characterized NAND area
- Unit capacitance and resistance
- Power ( $V_{dd}$ ,  $V_{th}$ ,  $I_{leakage}$ , ...)
- Macro LEF, Tech LEF

## RTL Design



## Architectural / RTL Floorplanning



## Chip Size Estimation

- Block placement
  - Utilization & white space
  - Blockage/flip-chip effect
- Multi-Row I/O placement

- Routing Congestion
- Net-wiring Analysis
- Power Estimation
- Power Network Prototyping

**Visualization and quantitative chip estimation methods are helpful for design space exploration at earlier design stages**

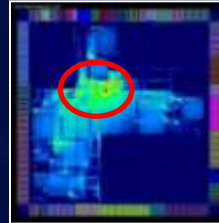


# Routing Congestion Analysis

## ■ Physical architecture design exploration at RTL stage

### ■ Feasibility analysis with routing congestion map

- Block-based routing congestion
- Virtual pin assignment for RTL blocks



### ■ Hot-spot routing congestion

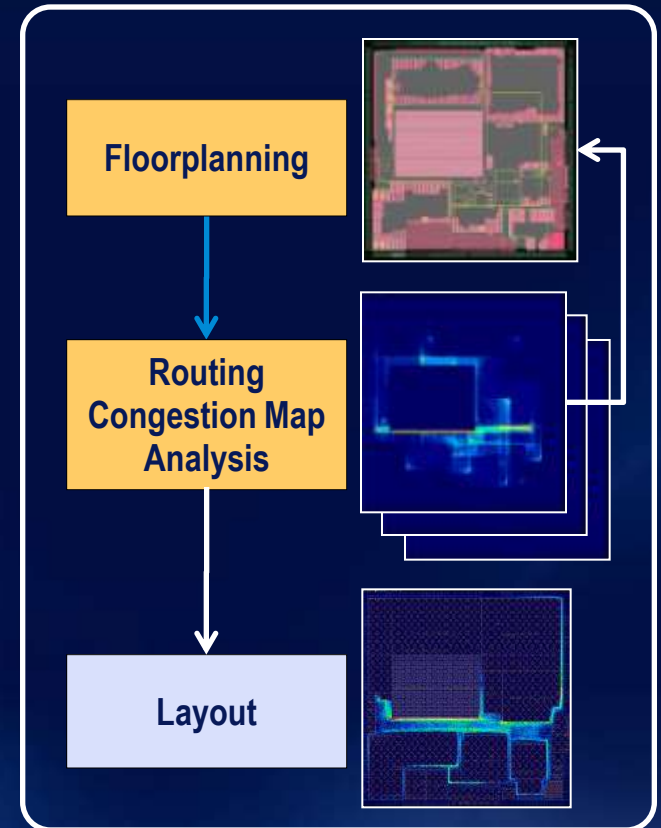
- Congestion redistribution by maximum congestion value
- Floorplan refinement



### ■ What-if analysis

## ■ Net-Wiring analysis for critical timing path

- Net length and delay estimation for inter-block nets
- Clock network trace and analysis



**Hot-spot routing congestion analysis to find the optimal routing congestion**

# Power Estimation and Power Planning Flow

- **Specification of design constraints**

- Floorplanning
- Power consumption data and routing layer information



- **Chip-level Peak Power Estimation**

- Scenario (power/clock domain) based estimation



- **I/O Pad Configuration and Analysis**

- IR-drop / SSN effects analysis
- Required number of power pads estimation
- Finding the proper power pads location
- Power pads and bump placement
- RDL routability analysis



- **Power Network Prototyping**

- Power Rail Resource estimation
- P/G pads and flip-chip bump placement



# Chip level Peak Power Estimation and Analysis

## ■ Target specification of power constraints

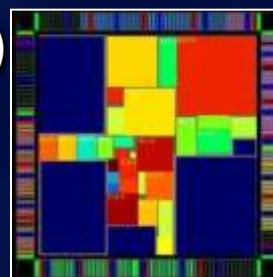
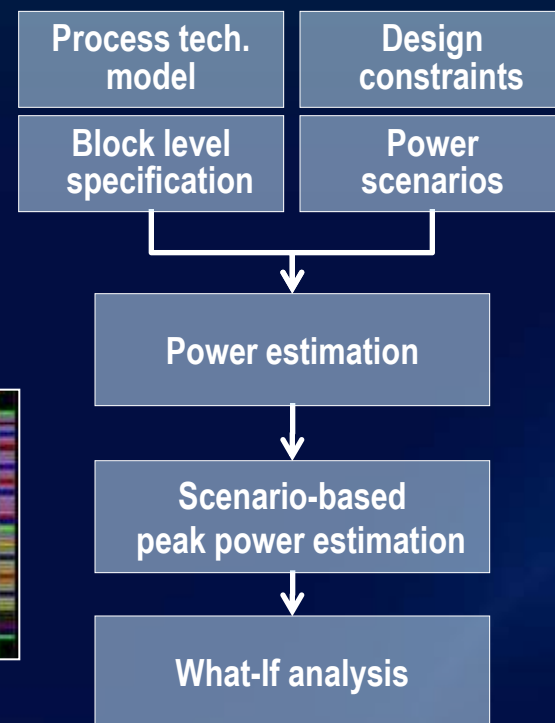
- Power/Clock domain for each block
- Switching activity and user defined power value
- Multiple power/clock domain assignment

## ■ Chip level peak power estimation

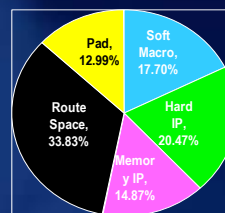
- Scenario-based power estimation (vectorless)
  - Power variation of the instance / power domain
- Peak power estimation

$$P_{peak} = \underset{\text{All blocks}}{MAX} [\underset{\text{For all power scenario}}{\sum} \alpha \cdot V_{dd}^2 \cdot f_{switching}]$$

- Power density estimation with  $P_{peak}$ 
  - Used for power planning



Peak Power: 0.135 [W]



**Finding the hot-spot power scenario that can be used for power rail resource estimation**



# I/O Pads Configuration and Analysis

## I/O Pads configuration

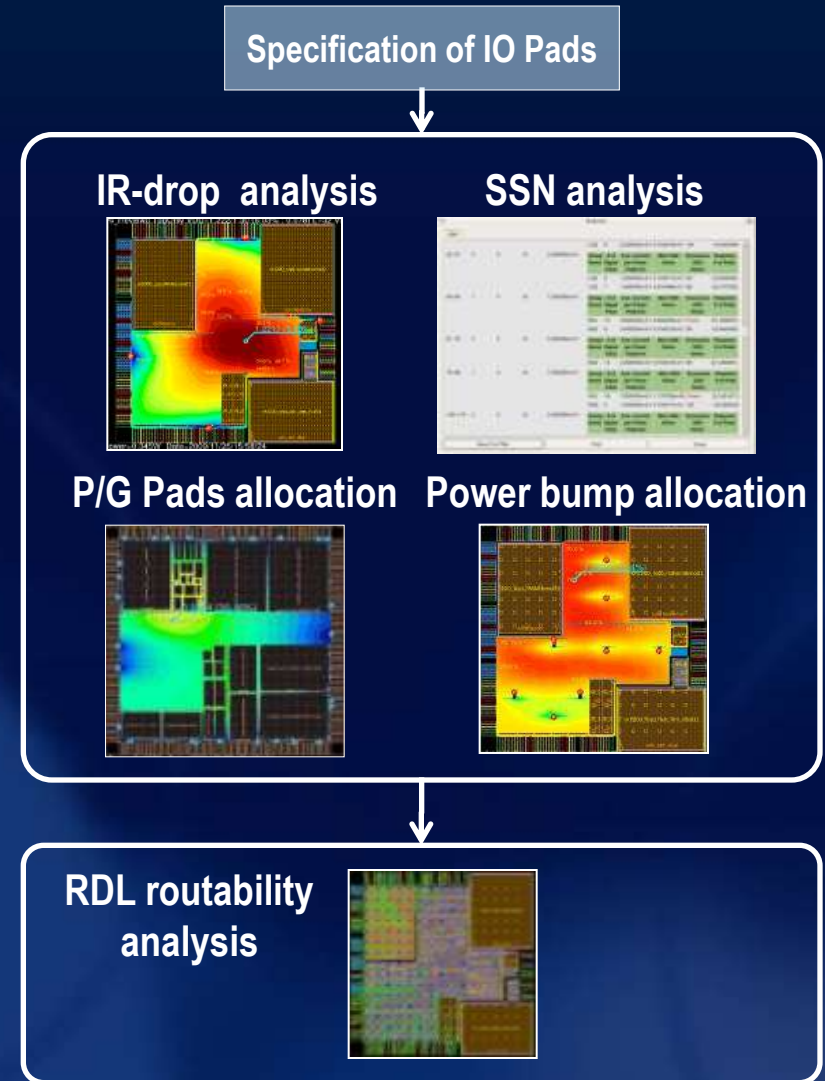
- Estimated chip-level peak power ( $P_{peak}$ )
- Core/block power ring width
- Pad types and package wire model

## Pads configuration and analysis

- IR-drop / SSN analysis
- The number of P/G pads estimation
- Power bump allocation for flip chip
- RDL routability analysis

## Estimation and optimization

- The number of P/G pads
- Pads sequencing for power/signal pads
- I/O pads location
- Power network structuring



# Power Network Prototyping

## ■ Rail resource estimation for power network prototyping

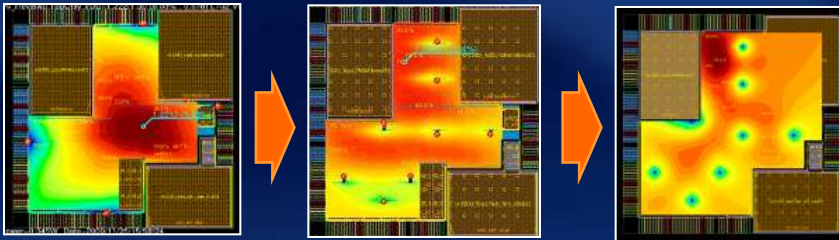
- Specification of target IR-drop rate
- Power bump and mesh allocation

## ■ Estimation of power mesh count

- The number of P/G Pads
- Power layers (type, resistance, min width)
- Target IR-drop rate

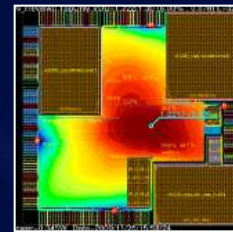
## ■ What-if analysis and refinement

- Hot-spot power re-distribution

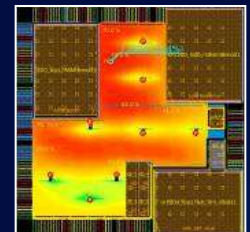


## What-If analysis

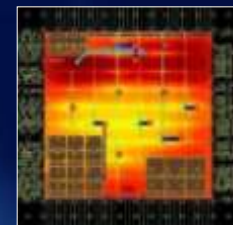
IR-drop analysis



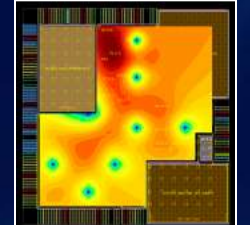
Power bump allocation



Power mesh allocation



Effect analysis

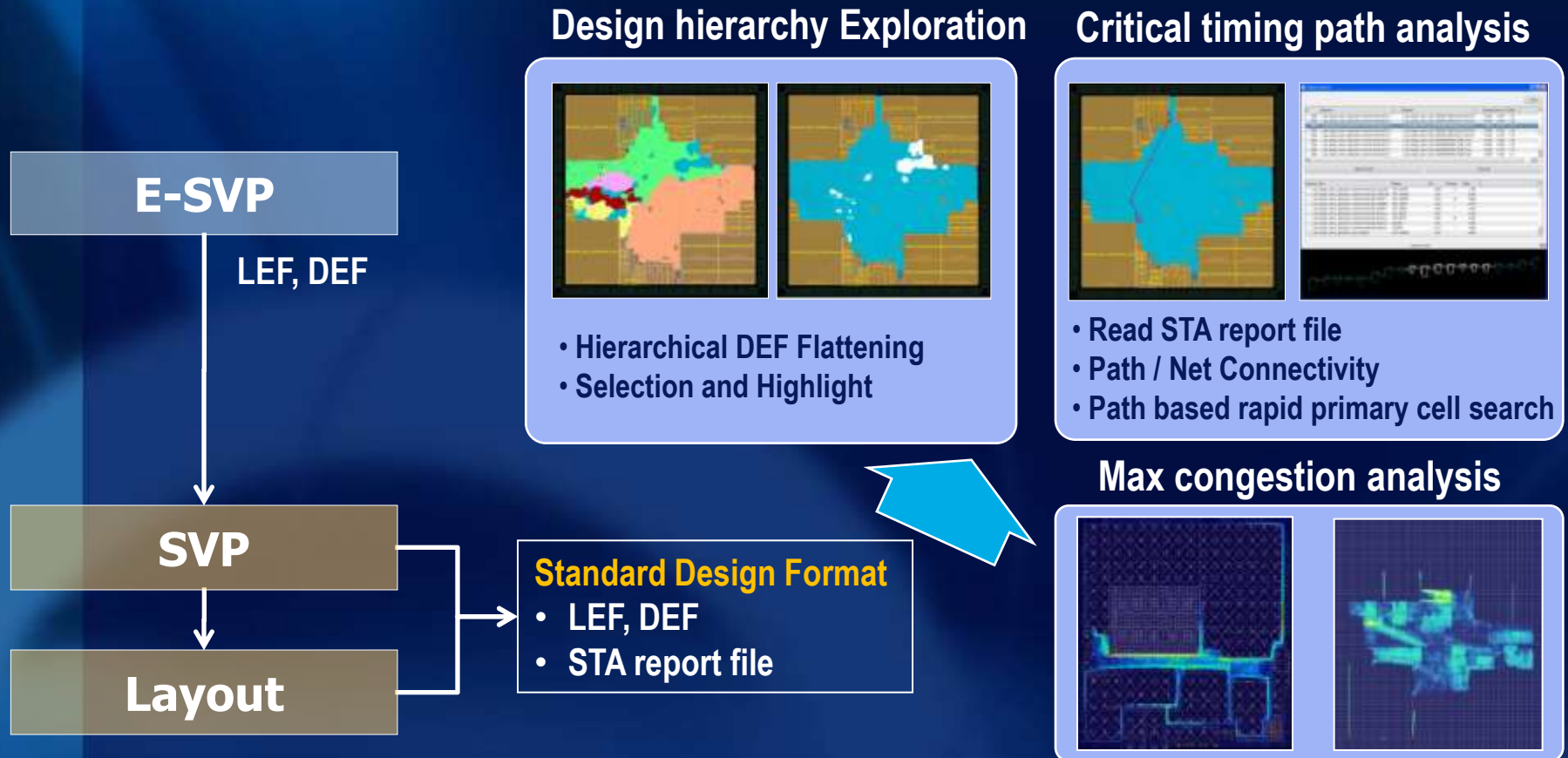


## ■ Power Network Prototyping

- Power rail resource estimation and exploration to minimize IR-drop effects
- Finds the optimal power network prototyping at earlier design stage

# Link to Chip Implementation Flow

## Rapid Layout Design Analysis for ECO



- Iteration time reduction between logic design and layout design
- Efficient layout report confirmation

# Case Study : Applications to SoC Design

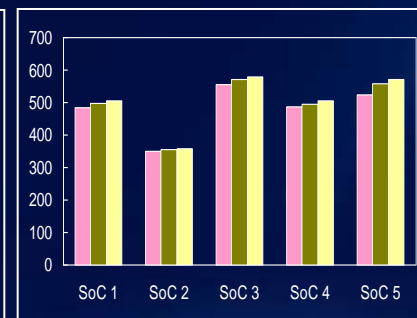
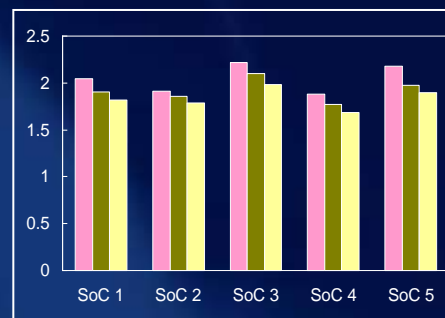
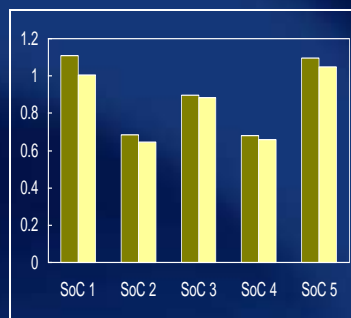
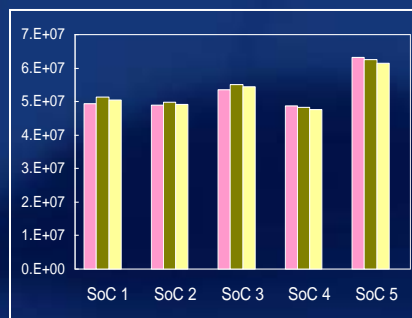
## ■ Applications of SoC designs

- More than 50M G/C including ARM processors, multiple media processing accelerators such as 3D graphics, and wide I/O memories, etc.

## ■ Experimental results with 5 SoC designs

- The estimation result (max difference, reference: layout)

| Design Stage | Area  | Max Congestion | Peak Power | Power Mesh Count |
|--------------|-------|----------------|------------|------------------|
| Arch. Level  | 2.7 % | -              | 14.8 %     | 8.2 %            |
| RTL          | 2.0 % | 10.2 %         | 5.9 %      | 2.3 %            |



■ AL ■ RTL ■ Layout

## ■ Run-time Comparison (reference: layout)

| Design Stage | Area Estimation | Max Congestion Estimation | Power Estimation | Layout Analysis for ECO |
|--------------|-----------------|---------------------------|------------------|-------------------------|
| Arch. Level  | 24 X            | -                         | 240 X            | -                       |
| RTL          | 9 X             | 9 X                       | 10 X             | 2 X                     |



# Summary and Future work

## ■ Early SVP(Silicon Virtual Prototyping) Design Methodology

- Implementation-aware design flow at architectural and RTL design stages
  - Provides an Early SVP solution to prevent unnecessary design iterations
  - Bridges to functional designers and chip implementation engineers
- Designing experiences with some SoC applications:
  - Demonstrated the validity and capability
  - Showed fast design space exploration with physical implementation factors
  - Established a seamless SoC design flow from architecture to layout design
  - Reduced design time by over 30% in SoC designs

## ■ Future work

- Setting up the technology model library for next generation of technology
- Improving the accuracy of timing estimation for critical timing path