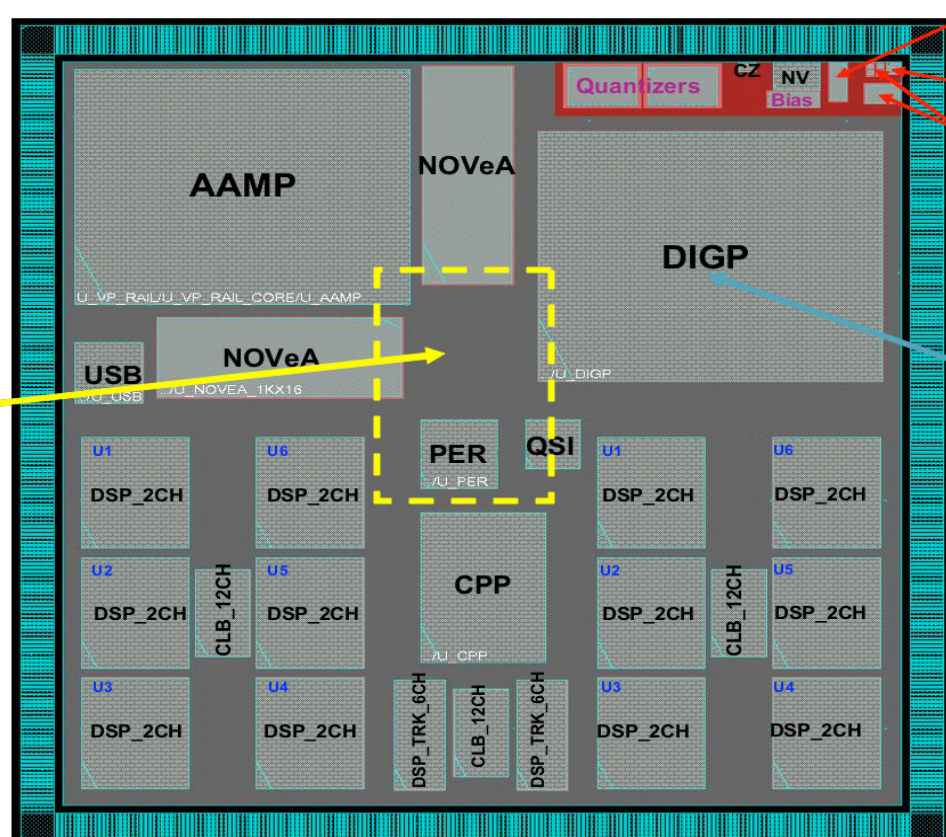


Correlating Predicted and Actual Power in a 90nm ASIC Power Island

Introduction

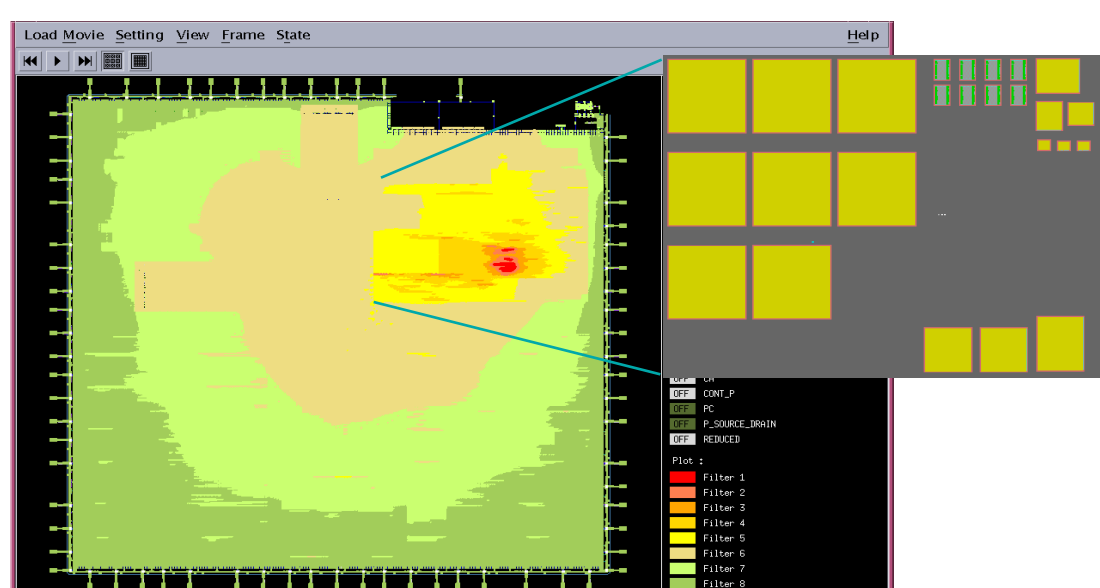
- Low yield drove an investigation into power issues within the internal power islands
- This poster presents results of the power investigation as a real world case study of internal power islands in a 90nm ASIC. Presents details of:
 - Power island structure
 - On-chip IR-drop and peak noise measurements via FIB pads
 - Block-level average power measurements using delta technique
- Comparisons of measured power vs power estimates from EDA tools
- Conclusions and future directions

ASIC Overview



- Process/Library
 - 90nm Low Power
 - 8 Metal Layers, 2 thick
 - 4 Library Thresholds
 - 12 Million Gates
 - 7 Mbits of Memory
- Internal Power Islands
 - Externally Supplied Power Islands
 - Embedded Flash Memory
- Analog Logic
 - Quantizers
 - PLL
 - EFuses
- DFT
 - Analog Test Bus
 - 23 Logic BIST Partitions
 - 78 MBIST Controllers
 - 98.5% Stuck-at BIST coverage
 - 99.8% Stuck-at Manufacturing Test Coverage
 - 95% Transition Manufacturing Test Coverage

Area Selected for Investigation

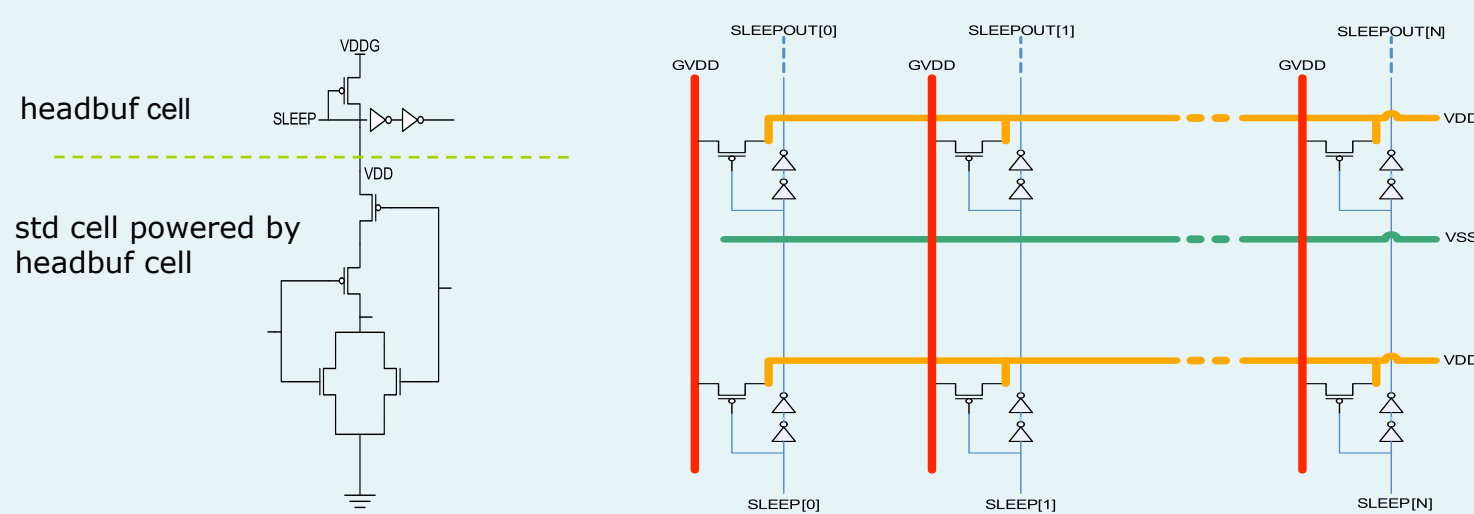


The DIGP Block

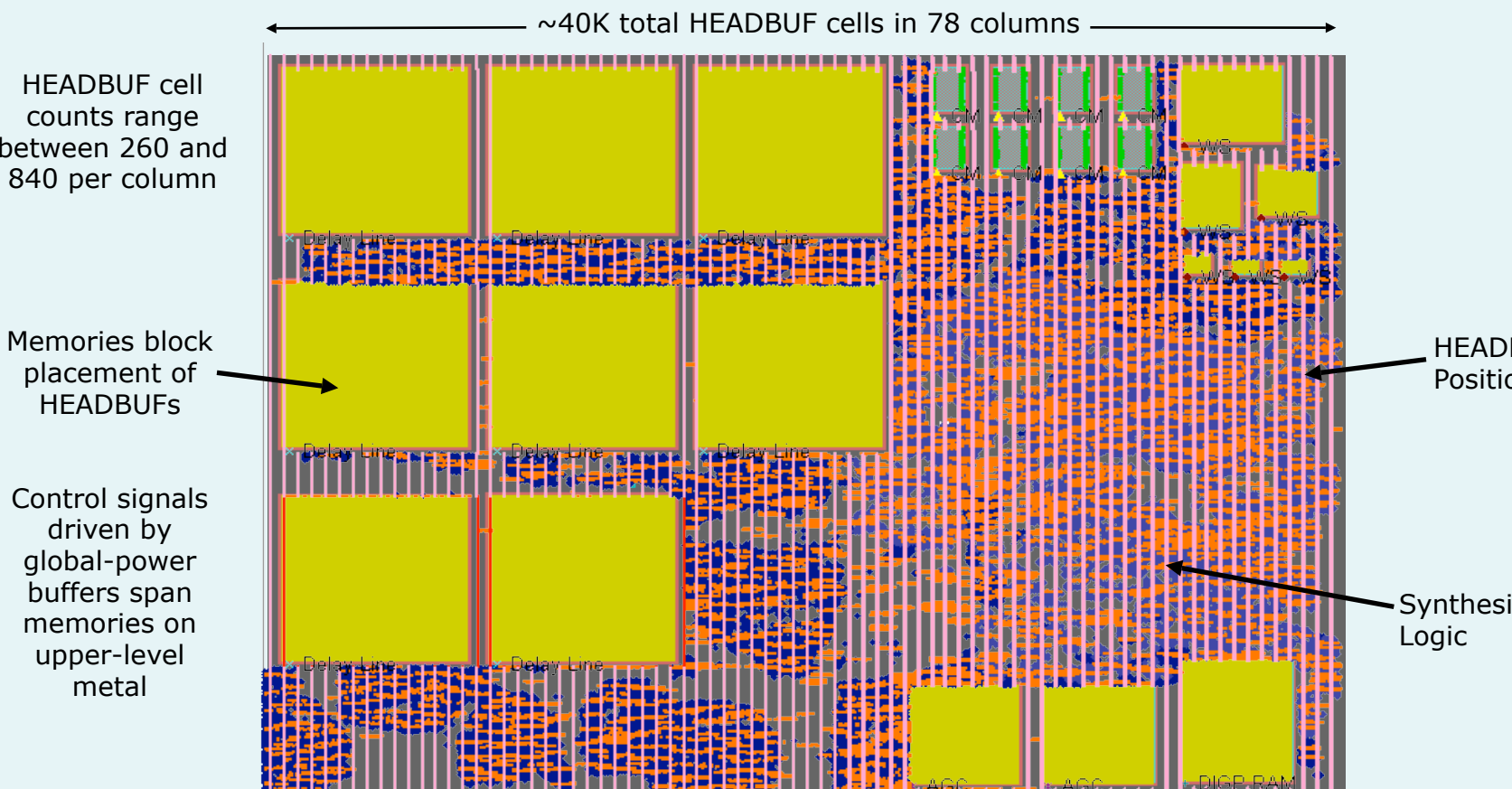
- Largest individual block
- 3.5M logic gates
- 25 memory instances
- Access to core VDD pads limited by adjacent analog logic and an externally supplied power island
- Separate LBIST domain
- LBIST operation represents worst-case power mode
- Separate power island
- Approximately 40K Headbuf cells

Background: Structure of a Block-Level Power Island

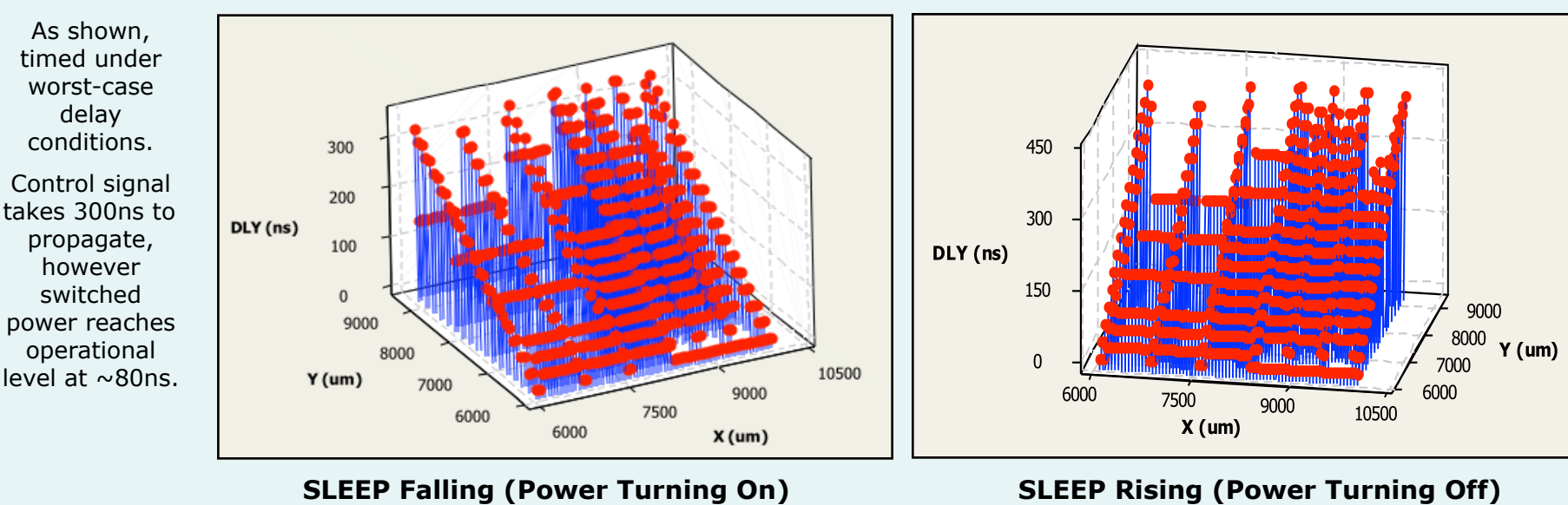
Headbuf Cell and Example Use



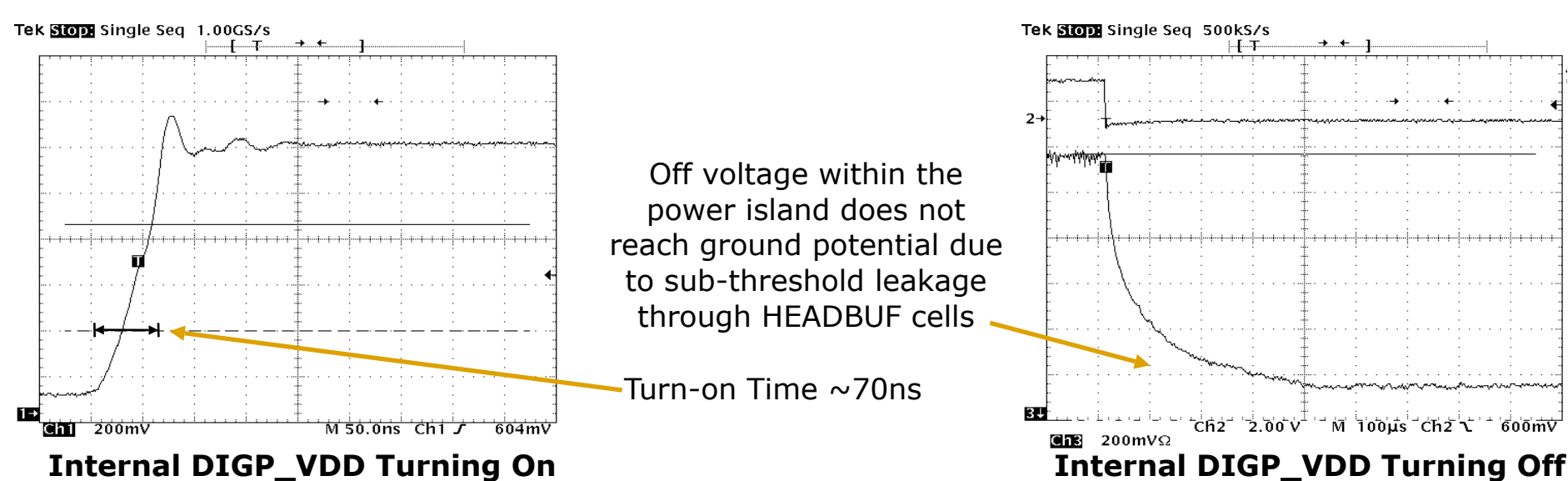
Headbuf Cell Placement in the DIGP Block



SLEEP Control Signal Timing vs. HEADBUF Location



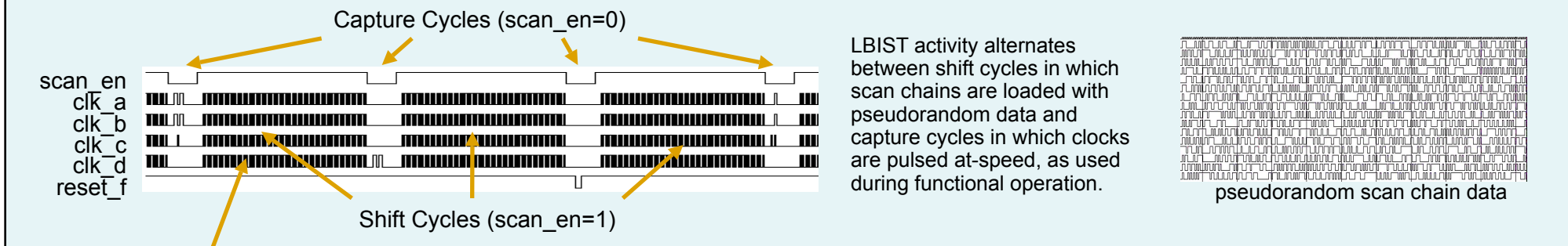
On-Chip Voltages/Currents Observed During Operation



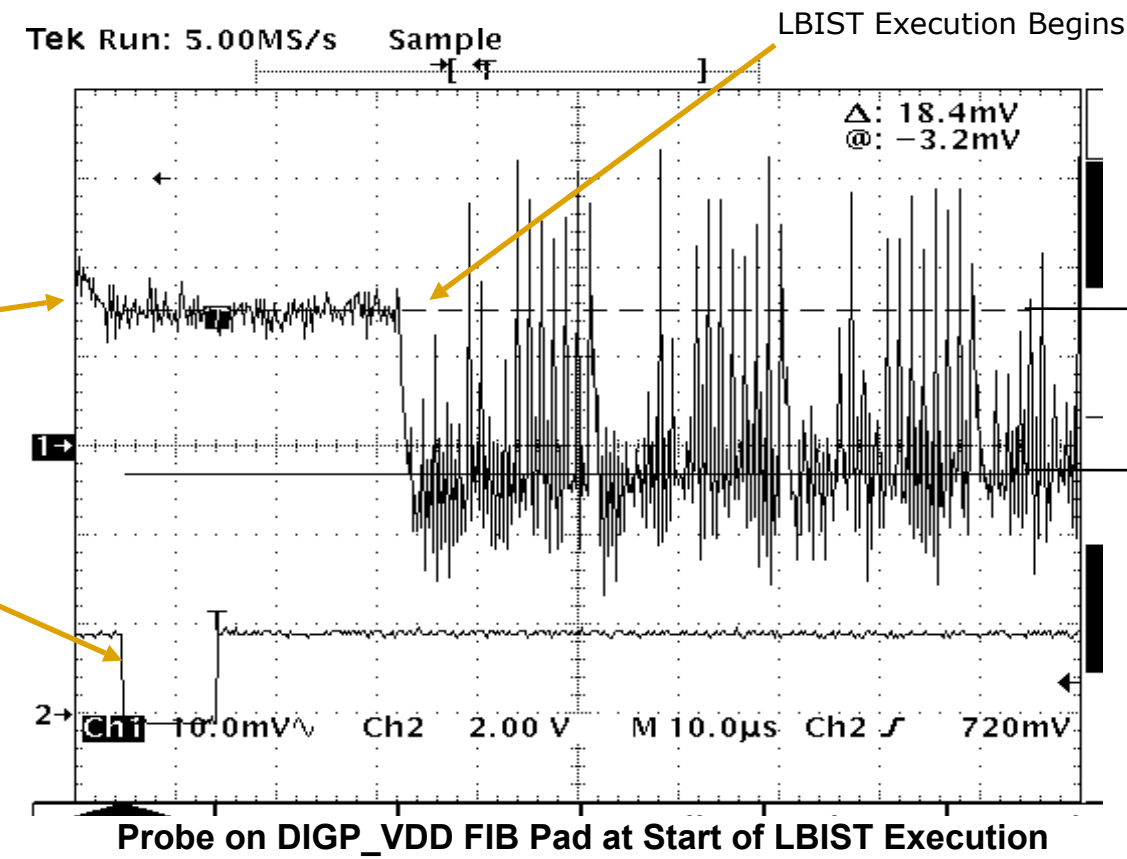
Off voltage within the power island does not reach ground potential due to sub-threshold leakage through HEADBUF cells

Turn-on Time ~70ns

Background: Activity During LBIST Operation



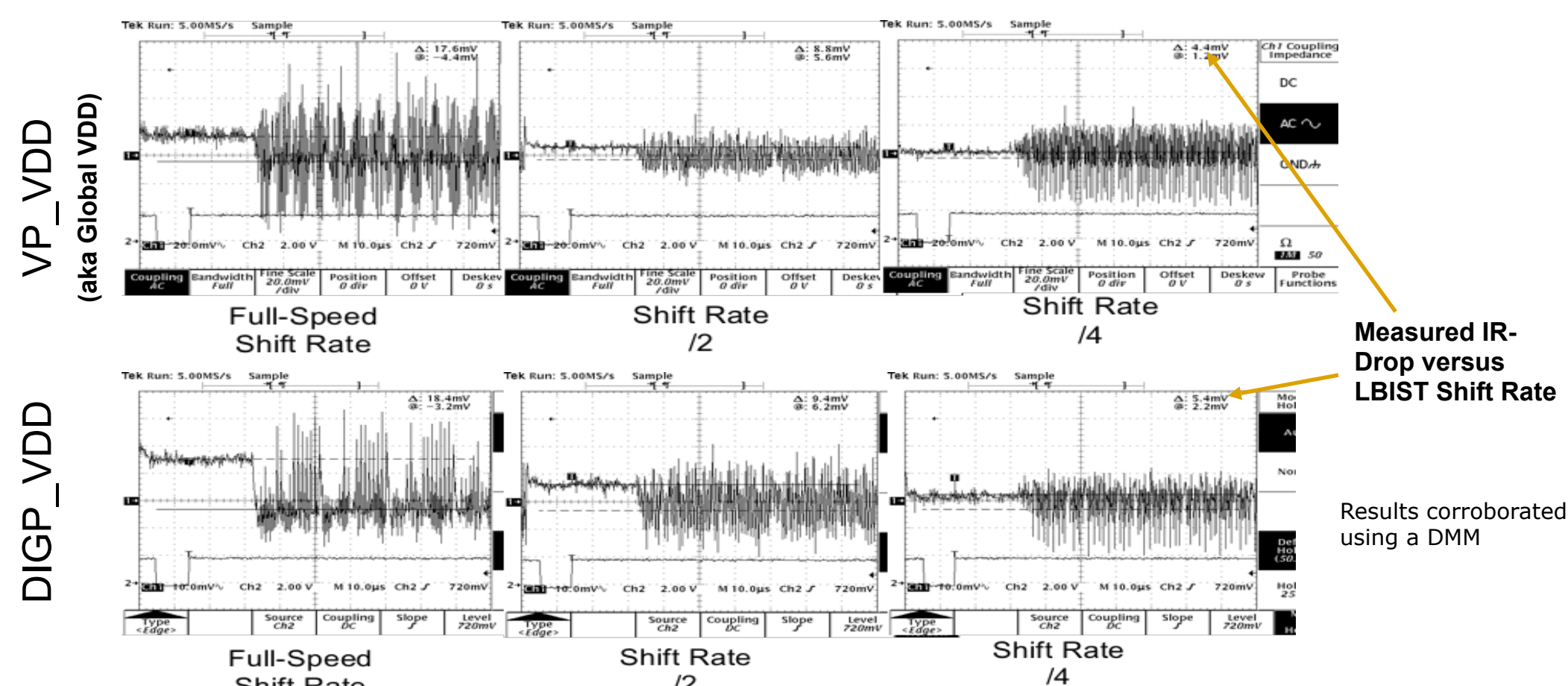
Capture cycles are always applied at the highest rated clock speed. Shift cycles may be programmed to operate at slower frequencies to reduce average power



Change in RMS level indicates IR drop

On-chip cpu programmed to toggle a general-purpose IO pin immediately before commanding LBIST in the probed area for use in triggering the scope

Probe on DIGP_VDD FIB Pad at Start of LBIST Execution



Measured IR-Drop versus LBIST Shift Rate

Results corroborated using a DMM

70mV with island switched off

3mV drop observed when clocks are enabled

Operational State	Measured using DMM		Measured IR drop (mV)		Scope RMS Delta	
	VP_VDD	DIGP_VDD	VP_VDD	DIGP_VDD	VP_VDD	DIGP_VDD
Initial VP_RAIL Power On	1.189	0.070	0	0		
DIGP_VDD On (LBIST inactive)	1.189	1.189	0	0		
DIGP LBIST (Shift Rate /4)	1.186	1.186	3	3		5.4
DIGP LBIST (Shift Rate /2)	1.184	1.184	5	5		8.8
DIGP LBIST (Full-Speed Shift)	1.171	1.170	18	19	17.6	18.4

Summary of Static IR-Drop Measurements

- Only slightly higher IR drop observed on the switched DIGP_VDD node driven by the headbufs.
- Good correlation between measurement methods.

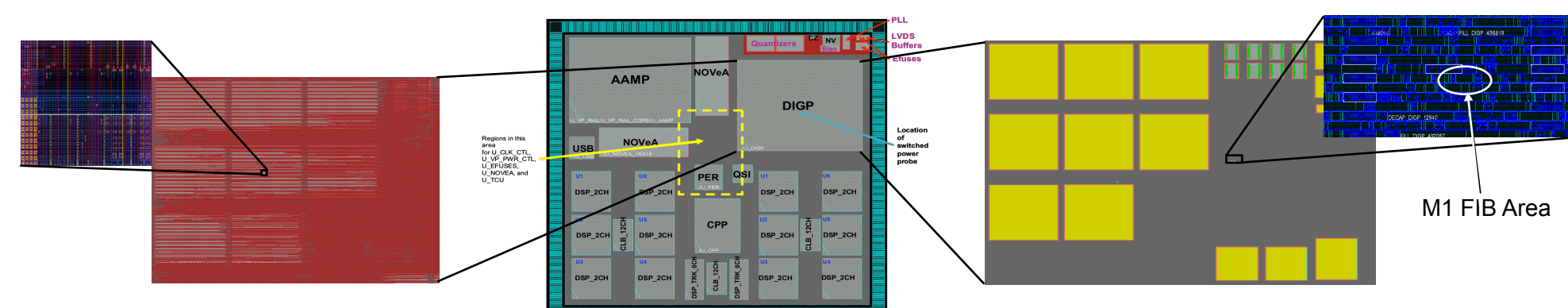
Worst observed IR-drop with maximum activity

Conclusions and Future Work

- As modeled, significant power is consumed by combinatorial glitches. Predicted total average power using zero-delay VCD was very close to measured range, but ~30% higher when using sdf-annotated VCD.
- Power island design was not a major contributor to yield loss. No significant degradation within the power island as compared with global power.
- Parallel investigations revealed problems with metal opens, other process issues contributing to low yield and suspected of causing lower than predicted power consumption.
- Differential technique permits average power measurement of individual power islands.
- Worst-case (Cmax) and best-case (Cmin) SPEF can be used at a particular operating corner to roughly approximate an estimated range of power due to silicon variation.
- A custom probe cell has been designed for use in follow-on chips to allow access to switched VDD on metal 1 in dense logic areas.
- Future work: Investigate sources of inaccuracy, correlate results/predictions for other block types, work to develop flow for more accurate prelayout and RTL (Spyglass) estimates of BIST power for use in architecture planning, power grid design, and test scheduling.

Access to Switched Power via FIB Pads

Planned FIB Locations

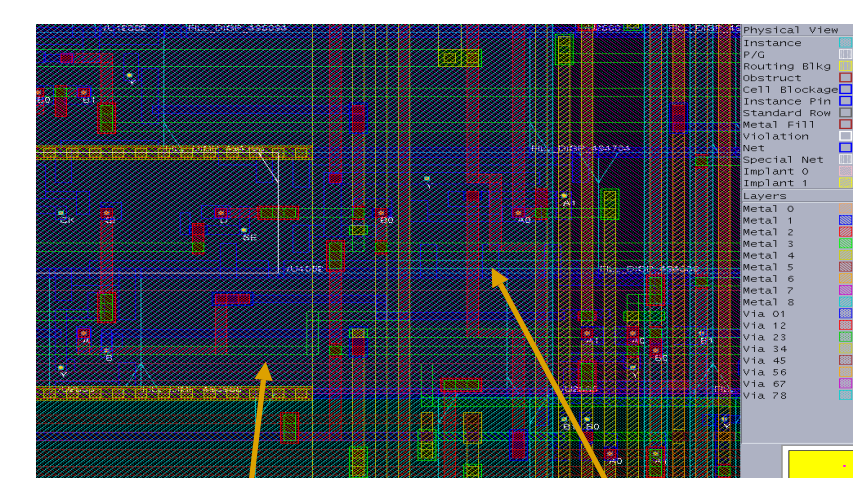
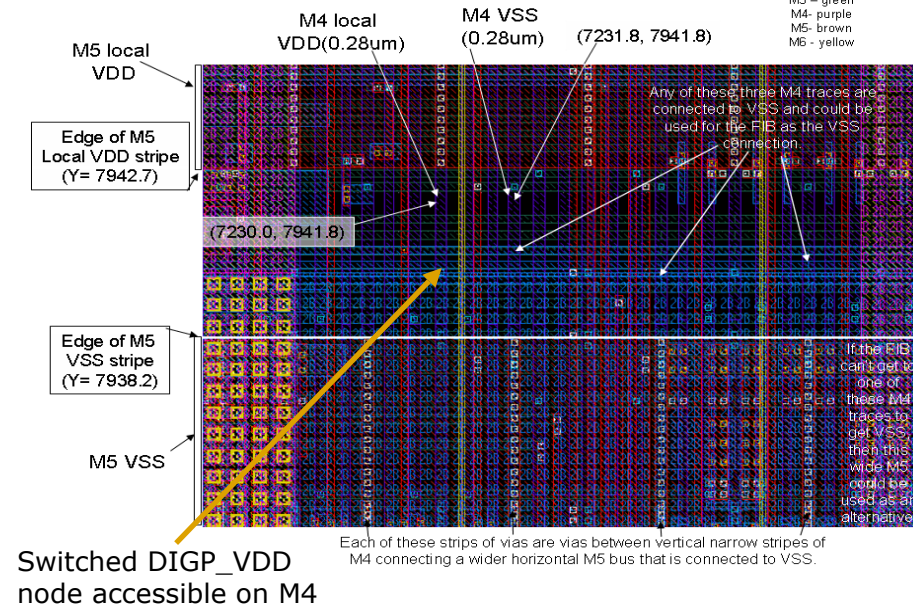


FIB Area Within Memory Array

This FIB successfully added probe pads and connections to the 0.28um switched DIGP_VDD node and global VSS

Attempted FIB Area Within Synthesized Logic

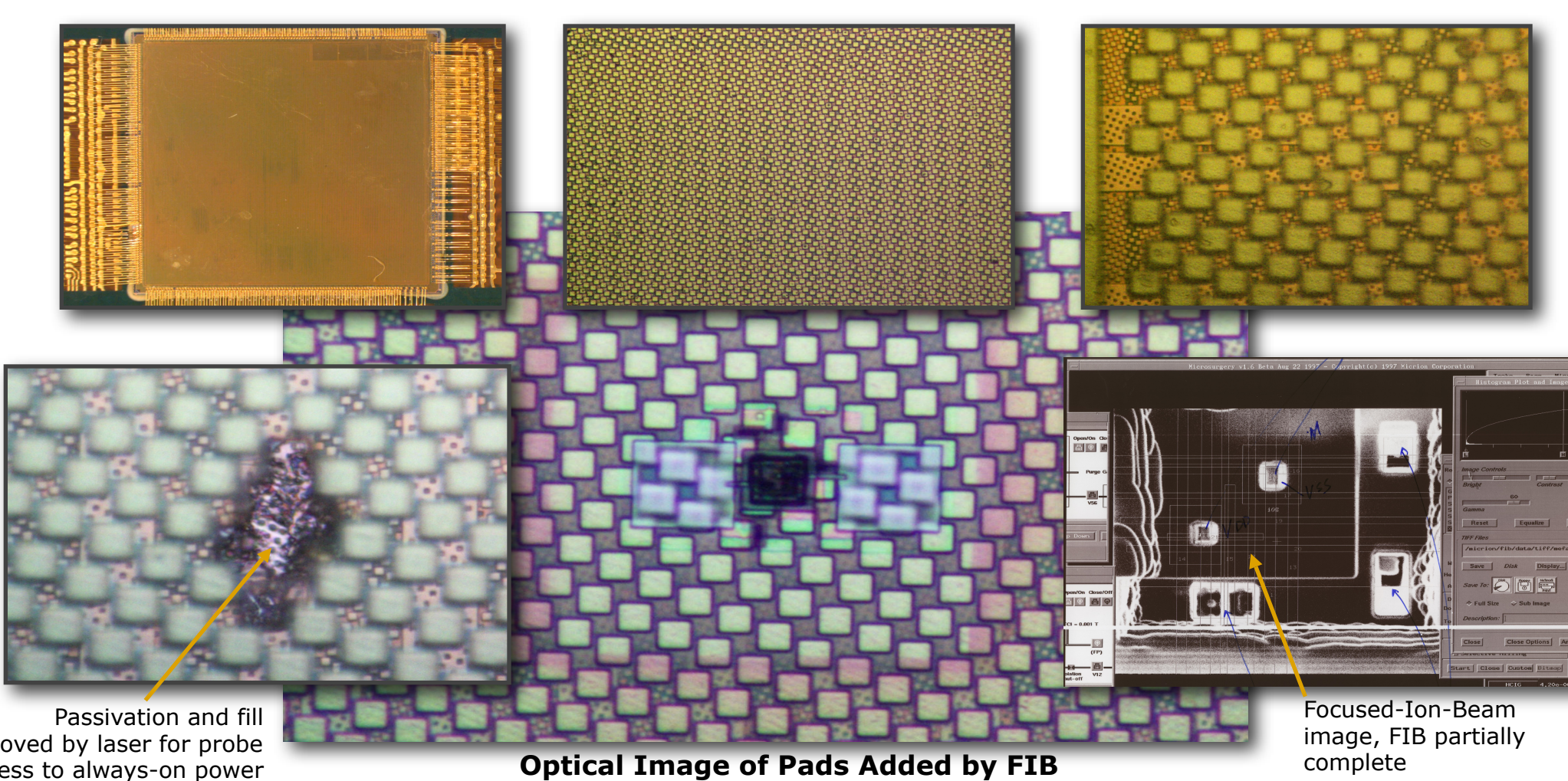
This FIB was planned but proved to be too difficult to implement without disturbing other logic due to overlying layers and density.



Switched DIGP_VDD node accessible on M4

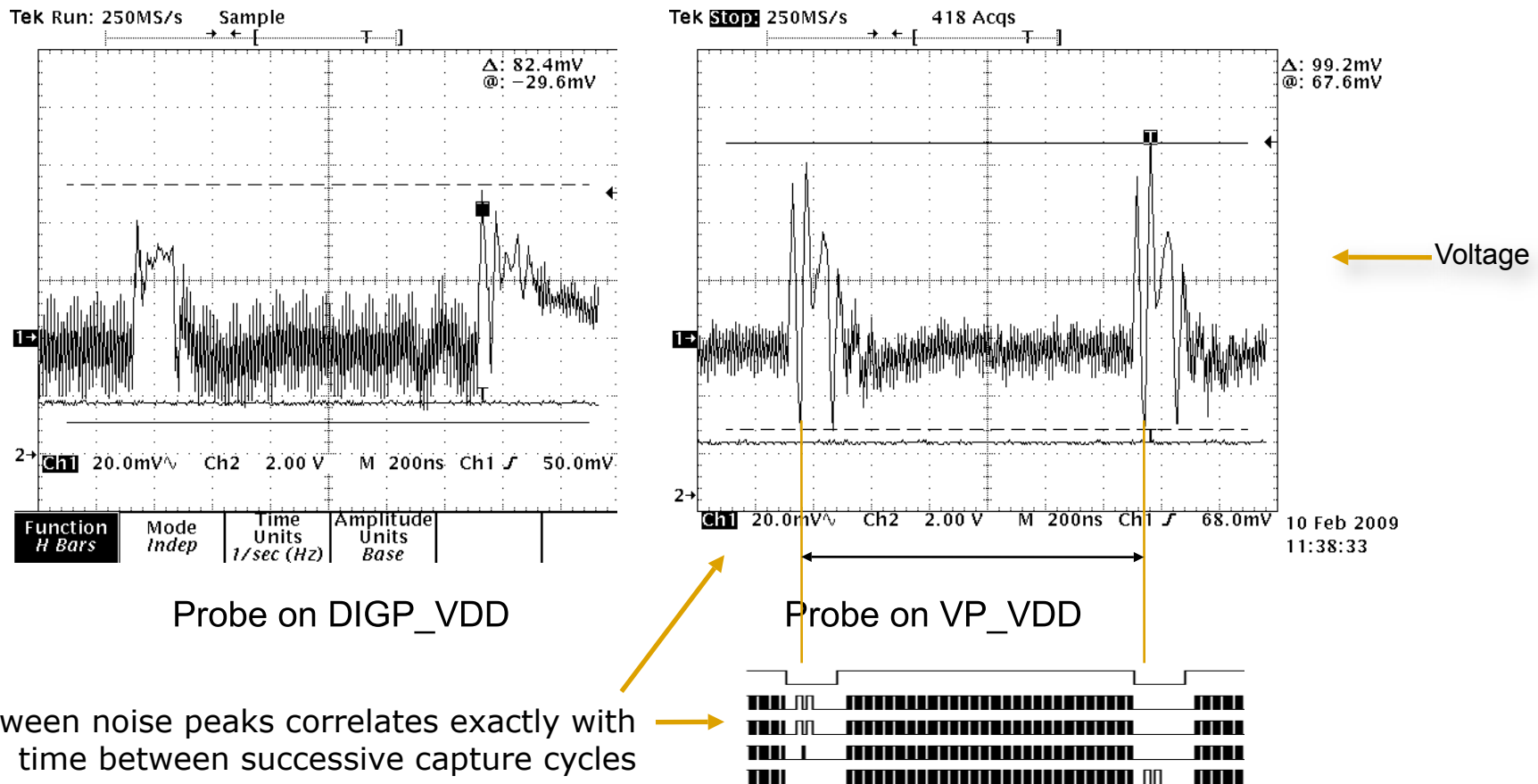
Entire area covered by Global VDD stripes on M8, M7, M6, M5 and M4

Die Photos



Measurements vs EDA Tool Predictions

Peak Supply Noise Measurements



Operational State	Scope - Peak-to-Peak Noise (mV)	
	VP_VDD	DIGP_VDD
DIGP LBIST (shift at 1/4 speed)	88.4	38.4
DIGP LBIST (shift at 1/2 speed)	82.4	46.4
DIGP LBIST (shift at full speed)	99.2	82.4

- Higher noise levels on global VDD (theory: probe is closer to noise source)
- Higher noise level at 1/4 speed shift than at 1/2 speed shift (theory: longer duration of zero activity between shift clocks and capture clocks)
- Unlikely that this represents the true peak noise at all locations

Average Supply Current Measurements

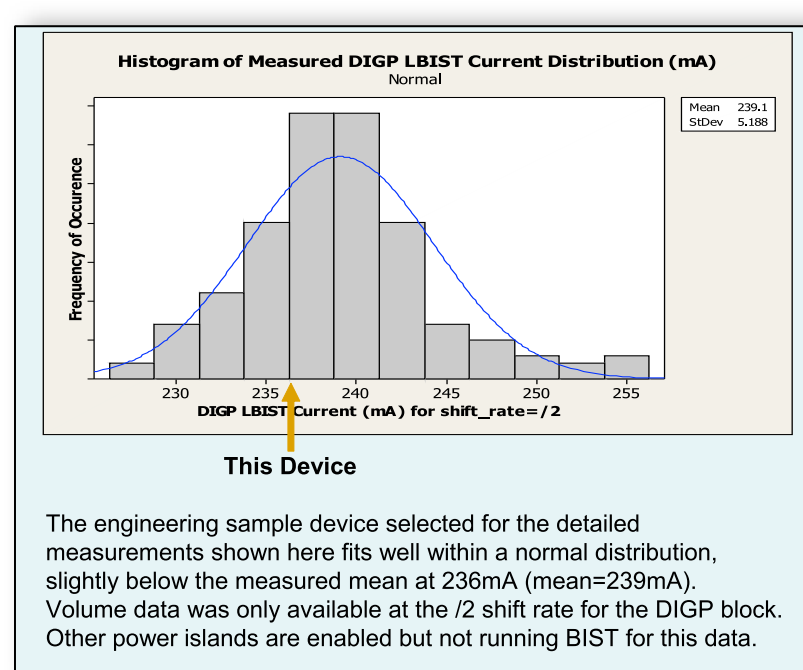
Measurement	Temperature:		Measured Core Supply Current (mA)									
	Core VDD % of Nominal (1.2V)		Ambient(25C)									
1) VP_RAIL on but internal DIGP_VDD off	90%	100%	90%	100%	110%	110%	110%	110%	110%	110%	110%	110%
2) DIGP_VDD on but DIGP clocks off	54.58	63.02	71.88	55.42	64.13	73.23	64.08	74.68	86.24	90.97	90.97	90.97
3) DIGP_VDD on, DIGP clocks on, but no other activity	99.83	113.30	127.30	100.80	114.80	129.30	112.40	129.00	147.00	147.00	147.00	147.00
4) DIGP running MBIST	111.40	126.20	142.40	111.00	127.60	142.30	123.40	140.70	160.10	160.10	160.10	160.10
5) DIGP running LBIST	122.50	138.80	155.80	123.60	140.40	157.90	135.60	154.90	175.70	175.70	175.70	175.70
a) Shift Rate /4	188.20	212.10	236.90	189.50	214.10	239.30	201.70	228.70	257.50	257.50	257.50	257.50
b) Shift Rate /2	318.50	357.60	396.20	319.20	359.10	400.00	330.60	373.20	417.60	417.60	417.60	417.60
c) Full Speed Shift Rate	67.92	75.78	83.94	68.18	76.27	84.67	71.51	80.24	89.46	89.46	89.46	89.46
Block-Level LBIST Current (1/4 speed shift) [5a-1]	133.62	149.08	165.04	134.08	149.97	166.07	137.61	154.04	171.28	171.28	171.28	171.28
Block-Level LBIST Current (1/2 speed shift) [5b-1]	263.92	294.58	326.34	263.78	294.97	326.77	266.51	298.54	331.36	331.36	331.36	331.36
Block-Level LBIST Current (full speed shift) [5c-1]	0.28	0.39	0.56	0.49	0.62	0.87	2.56	3.24	4.73	4.73	4.73	4.73

Since the block under test is itself a power island, the block-level supply current can be derived by separately measuring and subtracting the baseline chip core current with the island turned off [1] from the measured current with the island on and active (e.g. 5c) as long as all other activity is consistent. Leakage current can be determined (not accounting for sub-threshold leakage of the headbuf cells) by subtracting the baseline current [1] from the current measured when the power island is turned on but clocks are disabled [2].

Measured Power (Converted from Current Data)

Measurement	Temperature		Power (mW)	
	-55C	25C	105C	105C
Core VDD % of Nominal (1.2V)	110%	100%	100%	90%
Measured (Derived) Block-Level Total Power	430.8	354.0	287.8	287.8
Measured (Derived) Block-Level Leakage Power	0.74	0.74	3.20	3.20

A waveform excerpt from data generated by a PT-PX cycle-accurate power analysis run shows activity level variations that correspond with the timing of the measured peak noise.



PT-PX Power Estimates

Sources / Conditions		Power (mW)			
Total Power: Predicted Pre-Layout		Temperature			
Core VDD % of Nominal (1.2V)		-55C	25C	105C	105C
Process		110%	100%	100%	90%
PT-PX pre-layout, 100% annotated vcd, smallest wireload model		662.0	548.5	449.3	449.3
PT-PX pre-layout, 20% toggle, smallest wireload model		651.4	465.8	363.0	363.0

Sources / Conditions		Power (mW)			
Leakage Power: Predicted Post-Layout		Temperature			
Core VDD % of Nominal (1.2V)		-55C	25C	105C	105C
Process		110%	100%	100%	90%
PT-PX post-layout		0.16	0.30	2.15	2.15

Sources / Conditions		Power (mW)							
Total Power: Predicted Post-Layout		Temperature							
Core VDD % of Nominal (1.2V)		-55C		25C		105C		105C	
Process		110%		100%		100%		90%	
Predicted Block-Level LBIST Power (full speed shift) / spsf type		bc spsf	wc spsf	bc spsf	wc spsf	bc spsf	wc spsf	bc spsf	wc spsf
PT-PX post-layout, zero delay vcd, statistical average power		392.2	427.0	331.9	360.4	274.7	297.8	274.7	297.8
PT-PX post-layout, zero delay vcd, cycle-accurate average power		400.7	435.4	339.5	368.1	280.9	304.0	280.9	304.0
PT-PX post-layout, minisdf-annotated vcd, statistical average power		564.3	616.0	476.1	518.5	382.1	426.4	382.1	426.4
PT-PX post-layout, minisdf-annotated vcd, cycle-accurate average power		558.7	606.0	461.1	495.2	361.1	385.4	361.1	385.4
PT-PX post-layout, maxsdf-annotated vcd, statistical average power		552.7	603.1	466.3	507.7	384.0	417.5	384.0	417.5
PT-PX post-layout, maxsdf-annotated vcd, cycle-accurate average power		553.0	603.4	466.6	507.9	382.7	415.0	382.7	415.0

PT-PX Inputs and Settings:

- Parasitics 100% annotated from SPEF
- Activity 100% annotated from VCD
- Used 'create_power_waveforms' before 'report_power' to compute cycle-accurate average total power
- Estimates using SAIF as stimulus produced same result as the VCD-based statistical average power

Comparison of Back-End Tool Predictions (Cadence FE) vs. Measurements

fast_1.125C /wc_spef	VoltageStorm		21.3mV		Measured		25C/1.2V		19mV	
	Static IR Drop	Dynamic IR Drop	Static IR Drop	Dynamic IR Drop	Static IR Drop	Dynamic IR Drop	Static IR Drop	Dynamic IR Drop	Static IR Drop	Dynamic IR Drop
Island On Time	80ns	103.1mV	80ns	103.1mV	80ns	103.1mV	80ns	103.1mV	80ns	103.1mV
Average Power (toggle)	460mW	460mW	460mW	460mW	460mW	460mW	460mW	460mW	460mW	460mW